A Novel PPM Demodulator for Wireless Optical Transmission Systems

Rob Otte, L.P. de Jong and A.H.M. van Roermund

Delft University of Technology, Faculty of Electrical Engineering, Electronics Research Lab., Mekelweg 4, 2628CD Delft, The Netherlands
phone: +31 15 278 3679, fax: +31 15 278 5922, e-mail: r.otte@et.tudelft.nl

Abstract

Digital pulse position modulation (PPM) is a highly power efficient modulation scheme for use in wireless optical transmission systems. In this scheme, time is divided into frames, while each frame contains one pulse that is located at one of L possible slot positions. In our system a PPM method called 'half-pulse PPM' is used in order to simplify slot synchronization.

In this paper a novel half-pulse PPM demodulator is presented, based on a maximum likelihood principle. It detects the PPM slot containing the maximum amount of optical energy. The demodulator is extremely simple, since it consists of only an integrate-and-dump filter, an analogue memory, a comparator and some standard digital circuitry. Unlike conventional demodulators, the complexity hardly increases with L. This property is particularly attractive because in PPM systems the required transmission power decreases with increasing L.

A prototype, build with discrete components, was tested and its sensitivity was compared to its theoretically predicted value. For bit error rates in the order of 1E-3 the measured sensitivity approaches the calculated sensitivity quite close, while for smaller bit error rates, in the order of 1E-5, a deterioration of about 0.2dB (optical power level) occurs due to non-ideal circuit behaviour.

1 Introduction

In wireless optical communication systems digital pulse position modulation (PPM) is an attractive modulation scheme because of its power effi-

ciency [1]. In PPM transmission, time is divided into frames, which in turn are divided into L slots. One of the slots in every frame contains a pulse. If the width of the PPM pulses is chosen smaller than the slot duration, slot synchronization can simply be realized by means of a PLL [2], [3]. If the pulse duration is chosen equal to half the slot duration, the result is called 'half-pulse PPM'.

In this paper a novel PPM demodulator is presented for this type of signal. The complexity of the demodulator is very small because the memory function that is required in any PPM demodulator is realized as an appropriate mix of an analogue and a digital memory function. The demodulator is realized with discrete components to prove the feasibility.

Firstly the operation of the demodulator is discussed in section 2. Then in section 3 the circuit is presented and the measurement results are evaluated, and finally section 5 presents the conclusions.

2 PPM demodulation

In order to minimize the bit error rate, for every frame the demodulator assumes the PPM pulse to originate from the slot containing most optical energy (i.e. maximum likelihood demodulation). Thus a straightforward demodulator might consist of a series of L integrators, each integrating during one of the possible pulse intervals, accompanied by a series of comparators that mutually compare the L integration results, and a decoder that restores the originally transmitted bits. However, the number of integrators and comparators can be reduced to only one by storing only the largest integration result that was found until a particular moment, together with the number of the slot in which it was found. A block diagram of such system is shown in figure 1 together with an example of a PPM signal. The ratio of the pulse duration and the slot duration is denoted

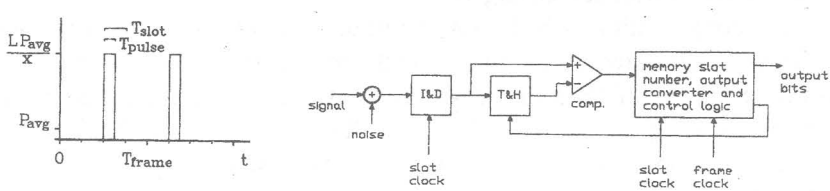

Figure 1: a) Half-pulse L-PPM signal b) Block diagram of the demodulator

as x; in the prototype $x = \frac{1}{2}$. The pulse height is chosen such that the

average signal level equals P_{avg}. In the block diagram the PPM pulses are integrated by an integrate and dump (I&D) filter. Storing the integration result is an analogue memory function, which in the block diagram appears as a track and hold (T&H) operation. Storing a slot number is performed most easily by means of some digital memory function. In the diagram this digital memory is incorporated in the output block.

The I&D filter is controlled directly by the slot clock. During a slot interval it passes three modes as indicated in the timing diagram shown in figure 2. During the pulse interval it is in the 'charge' (or integrate) mode,

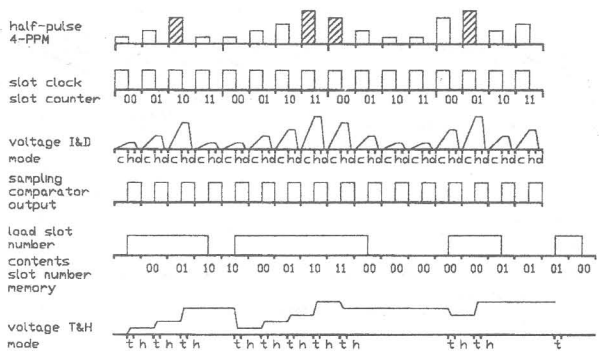

Figure 2: Timing diagram of the demodulator. The dashed pulses are the PPM pulses, the other pulses are dummy pulses that represent the influence of noise.

followed by the 'hold' and 'discharge' (or dump) mode. At the end of each charge interval the I&D filter contains an integration result corresponding to a pulse interval. The integration results can be stored in the track and hold circuit to facilitate their mutual comparison. Each frame starts with copying the first integration result into the track and hold circuit, so that it can be compared to the next integration result. This comparison is performed by sampling the comparator output at the positive edges of the signal shown in the timing diagram. When the value in the integrate and dump filter exceeds the value in the track and hold circuit, the actual contents of the I&D filter are copied into the track and hold circuit, while simultaneously the slot number corresponding to that integration result is stored. The signal that initiates these actions and the slot number that is stored are also shown in the timing diagram.

This procedure is repeated until the last slot has passed. At that time the track and hold circuit contains the largest integration result found in the frame, while the digital memory contains the corresponding slot number. By means of a parallel to serial converter this slot number is converted to a number of output bits. Meanwhile a new frame is being received.

3 Demodulator circuit

The demodulator circuit is shown in figure 3. The circuit is controlled by

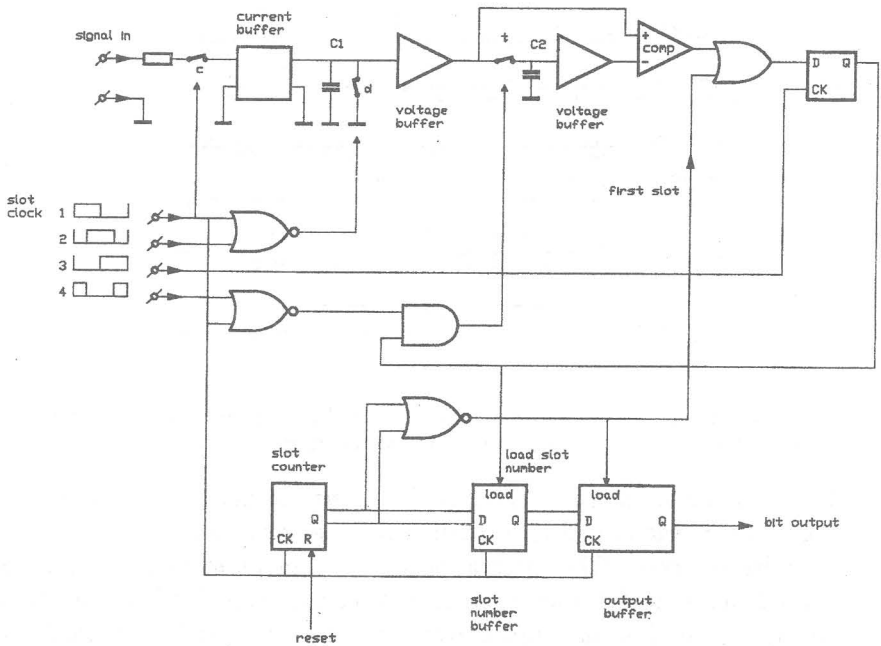

Figure 3: The demodulator circuit

three CMOS switches. The I&D filter consists of capacitor C1 and the switches 'c' and 'd' that are controlled directly by a four-phase slot clock. The track and hold circuit consists of capacitor C2 and switch 't', that is controlled indirectly by the comparator and the slot counter. In order to count the slot numbers correctly, the slot counter has to be synchronized

by some frame synchronization system. This is done using the reset input. The frame synchronization system will be discussed in a future paper.

4 Measurements

The bit error rate for Gaussian noise can be calculated as [3]:

$$\text{BER} = \frac{L}{2} Q\left(\sqrt{\frac{L\log_2 L}{2x}}\frac{P_{\text{avg}}}{\sqrt{N_0 R_b}}\right)$$
$$\text{with } Q(k) = \frac{1}{\sqrt{2\pi}}\int_k^\infty \exp -\frac{1}{2}\lambda^2 d\lambda \qquad (1)$$

in which P_{avg} is the average PPM signal level, N_0 is the double sided noise spectral density, R_b is the bit rate, and x is the ratio between the pulse duration and the slot duration. The BER was measured at a bit rate of 5kbps. The measurement results, together with eq. 1, are shown in figure 4. Because the BER is plotted as a function of the argument k of the Q-function, the results only indirectly depend on the bit rate. For large

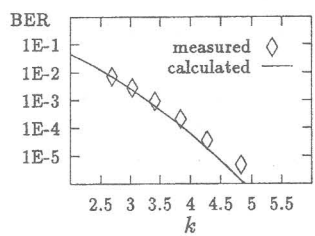

Figure 4: Calculated and measured BER versus k

noise levels, the measured results and the calculated results agree very well. For small noise levels, the sensitivity is about 0.2dB (optical power level) worse than expected. This is mainly caused by some offset in the current buffer that affects the integration result that is loaded into the track and hold circuit during the 'track' mode. Note that by shortening the duration of the 'track' mode, the sensitivity of the demodulator to additive errors in the current buffer can be decreased. During the other modes, the demodulator is insensitive to additive errors in the current buffer and the circuit that buffers the voltage across C1, due to 'self referencing'. Further it is insensitive to multiplicative errors in these circuits. The voltage buffer following C2 and the comparator have to be accurate, since their inaccuracies

directly deteriorate the sensitivity of the demodulator. No deterioration due to nonideal switch behaviour was observed.

Although the prototype operates at a speed of 5kbps, essentially the bit rate can be increased. The maximum possible bit rate follows from the maximum slot rate, that in turn depends on the available channel bandwidth and the chosen technology. In our application, indoor communications, the channel bandwidth is limited to 10MHz, due to multipath dispersion. This allows for slot rates as fast as 1MHz without significant sensitivity deterioration. This can be realized using the available LED and receiver technology. Thus, for L=4, bit rates up to 500kbps are feasible.

5 Conclusions and future work

The feasibility of the demodulator was proved by realizing a prototype and measuring the sensitivity. The sensitivity approaches the maximum possible sensitivity within 0.2dB (optical power level). This figure can be improved by further reducing the offset current of the current buffer at the input of the demodulator. Although the prototype is an L=4 PPM demodulator, larger values of L can be realized without seriously increasing the complexity. In our application, the maximum bit rate is limited to about 500kbps due to multipath dispersion. A 500kbps receiver with programmable L, containing the proposed demodulator, a slot synchronization circuit and a frame synchronization circuit, is currently being realized in CMOS technology.

References

[1] J.R. Barry, *Wireless Communication Using Non-Directed Infrared Radiation*, Ph. D. Thesis, University of California at Berkeley, 1992, or, same author, *Wireless Infrared Communications*, Kluwer Academic Publishers, Boston, 1994.

[2] V.A. Vilnrotter and E.R. Rodemich, *A Synchronization Technique for Optical PPM Signals*, Proc. IEEE Military Com. Conf. (MILCOM '86), Vol. 3, pp. 45.2.1-45.2.6, Montery, CA, Oct. 1986.

[3] R. Otte, *Power Efficiency, Bandwidth Efficiency and Slot Synchronization in Wireless Optical PPM Transmission Systems*, these proceedings, Electronics '96, Sozopol, Sept. 1996.