

Dependencies between Basic Timing Parameters in Image Processing System

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Abstract – This paper presents the dependencies between the basic timing parameters that define the processing of a pixel from image generated by a matrix image sensor. The ratio between pixel clock frequency and the time required for one pixel processing determine system parameters like frame rate, system clock frequency, the choice of processing algorithms, achievable accuracy. Here are presented several configurations of image processing system and opportunities through which it is possible to relax the timing requirements to the system and to make its design process more flexible.

Keywords – image processing system, frame rate, clock frequency, processing cycles, parallel processing.

I. INTRODUCTION

The main component of image processing system is the processing block. It contains a set of elements that implement different operations over the individual pixels, groups of them or over the entire frame. The type of these elements and the connections between them depend on the current application and the utilized hardware-software platform. The frames generated by the image sensor are transferred serially to the processing block. This fact allows implementation of conveyor processing of the pixel data flow (Fig.1). Each processing element (PE) executes one certain function over a portion of the input data and then sends the result to the next PE. All elements of the processing block are synchronized to the main system clock frequency F_{SYS} .

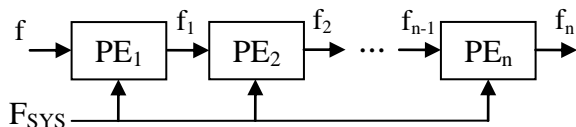


Fig.1. Data flow processed by conveyor

The conveyor type of data processing structure requires nonstop data execution and guaranteed lack of data loss. In order to satisfy this requirement, every PE should complete the processing of the current portion of data before the arrival of the next one. Duration of the time interval that every PE requires for execution of its specific function varies upon the different functions and it is in direct relation to the PE clock frequency.

In the following paper, several possible configurations of image processing system are presented and for every one of them the dependencies of the basic timing parameters are defined.

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II. TIMING PARAMETERS DEPENDENCIES

At fig.2 a single PE is presented with its main connections. The data that is to be processed (f) comes from the image sensor or from the previous PE. The result (f_{PE}) is transferred to the next PE when the function is completed. The clock frequency of the PE (F_{PE}) is derivative of the system clock frequency F_{SYS} , but it is not obligatory that all PE work with same F_{PE} – if it is possible to adjust the individual F_{PE} of every PE, the designer gets a great flexibility during the system design and configuration.

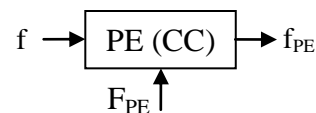


Fig.2. Processing element

Time duration for one pixel processing (T_{PP}) is proportional to the period of the PE clock signal and the total number of clock cycles (CC) needed for completion of the certain function:

$$T_{PP} = CC \times T_{PE} = \frac{CC}{F_{PE}} \quad (1)$$

Formula (1) is basic point that manifests the opportunities to gain additional flexibility during the design and the configuration of the image processing system. If one of the product components or both of them are changed, some main topics could be settled:

- Pixel processing duration T_{PP} could be reduced through decreasing of CC by implementing simpler and/or shorter algorithm with eventually less accurate final result;
 - In order to get certain required better precision, the implementation of more complex and/or more accurate algorithm will increase T_{PP} along with CC;
 - T_{PP} could be changed through increasing or decreasing of clock frequency (F_{PE}) of the PE. Due to the fact that F_{PE} is directly related to the energy consumption, T_{PP} value could be designed with taking this fact into consideration;
 - Certain amount of CC increase, caused by algorithm complexity or increased accuracy, could be compensated by proportional increase of F_{PE} and by this keeping T_{PP} constant;
 - If simpler and/or shorter algorithm is implemented, the reduced value of CC will allow corresponding reduction of F_{PE} and thus lower energy consumption.
- Parameter T_{PP} is in direct dependence on pixel clock signal and the chosen frame processing configuration. Three possible configurations are analyzed and parallel processing of data flow with multiple PE is presented as a fourth case.

A. One-Pixel processing configuration

At this configuration the pixels are processed at the time of their arrival. Duration of one pixel processing T_{PP} should be less or equal to the time of next pixel arrival, which is indeed the period of the clock signal that gets the pixel from the image sensor:

$$T_{PP}^P \leq T_p = \frac{1}{F_p} \quad (2)$$

From formulas (1) and (2) follows

$$T_{PE}^P \leq \frac{T_p}{CC} \quad (3.1)$$

$$F_{PE}^P \geq CC \times F_p \quad (3.2)$$

which means that the clock frequency of the processing element should be at least CC -times greater than the frequency pixel arrivals at that element. If this is not true, there have to be some buffering for the pixels that leads to the next configuration.

B. One-Row processing configuration

This configuration take advantage of the fact that at every transferred row there is additional time period (Horizontal Blanking, T_{HB}) after the last pixel of that row. The total amount of time needed for processing of all the pixels (M) from one row at certain PE should be no greater than T_{ROW} :

$$M \times T_{PP}^L \leq T_{ROW} = M \times T_p + T_{HB} = (M + P_{HB}) \times T_p \quad (4)$$

Time for one pixel processing in this configuration is

$$T_{PP}^L \leq \frac{T_{ROW}}{M} = \frac{M+P_{HB}}{M} * T_p = \frac{T_p}{\alpha} = \frac{1}{\alpha \times F_p} \quad (5)$$

$$\text{where } \alpha = \alpha_N = \frac{M}{P_R} = \frac{M}{M+P_{HB}} < 1 \quad (6)$$

The coefficient α represents that part of T_{ROW} during which the current row pixels are received at PE. It is analogue of the digital signal parameter "duty cycle".

From formulas (1) and (5) follows

$$T_{PE}^L \leq \frac{T_p}{\alpha \times CC} \quad (7.1)$$

$$F_{PE}^L \geq \alpha \times CC \times F_p \quad (7.2)$$

Formulas (7.1) and (7.2) show that due to the addition of the horizontal blanking period to the whole row processing duration ($\alpha < 1$) the requirements to the PE are relaxed in comparison to One-Pixel processing configuration. This is advantage that could be used in one of the following cases:

- Increasing CC (allows utilizing function that requires more clock cycle for completion) while keeping T_{PE} and T_p the same;
- Decreasing PE clock frequency F_{PE} ;
- Increasing pixel frequency F_p , hence increasing frame rate (if image sensor is capable of this);

- Some combination of previously mentioned actions on condition that (7.1) and (7.2) are not violated.

This configuration ($T_p < T_{PP} < T_{ROW}/N$) requires FIFO buffer to store the arriving row pixels while they are waiting their turn for processing (fig.3). Its volume should be large enough to prevent data loss, but adequate memory usage is also a factor that determines the size of the buffer. Having these into consideration, calculation of B_{ROW} is made in order to find the minimal value that is enough to hold the maximum possible number of row pixels.

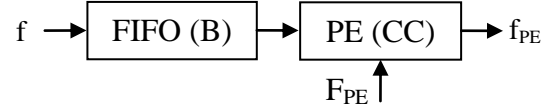


Fig.3. Processing element with FIFO buffer

The buffer should be emptied at the beginning of the next row and if this is not the case, there will be accumulation of waiting pixels that increases with every row. When the frame includes many rows the queue becomes enormous and requires buffer with significant size. This situation is described in the next system configuration. Pixel accumulation starts with the first pixel of the current row and continues until the last one from this row is received. At the same time goes extraction of elements in the head of the FIFO buffer and their processing by PE and by this freeing space for new pixels. The size of the buffer is determined by the number of pixels that could be processed during the horizontal blanking – time interval in which extraction from FIFO continuous and no new pixels are added. All the other elements should be processed before the start of T_{HB} . Total duration of processing the remaining pixels in the FIFO during horizontal blanking is

$$T_{BUF} = T_{PP}^L \times B_{ROW} \leq T_{HB} \quad (8)$$

From the limitation (8) and formula (5) follows

$$B_{ROW} \leq \frac{T_{HB}}{T_{PP}^L} = \frac{P_{HB} \times T_p}{\alpha} = \alpha \times P_{HB} \quad (9)$$

C. One-Frame processing configuration

When PE is not capable of processing the entire row during the T_{ROW} period, system configuration with larger FIFO buffer should be used. It uses the additional time slot in the frame (Vertical Blanking, T_{VB}) to deal with the remaining content of this buffer. All pixels from one frame of N rows and M columns (total number of $N \times M$ pixels) should be processed for the total time less than T_{FRAME} :

$$N \times M \times T_{PP}^F \leq T_{FRAME} = R_F \times T_{ROW} = R_F \times P_R \times T_p \quad (10)$$

where R_F (Rows-pr-Frame) is the duration of the frame in rows and P_R (Pixels-per-Row) is the duration of one row in pixels. Time duration of one pixel processing is

$$T_{PP}^F \leq \frac{T_{FRAME}}{N \times M} = \frac{R_F \times P_R}{N \times M} * T_p = \frac{T_p}{\alpha_N \times \alpha_M} = \frac{T_p}{\beta} = \frac{1}{\beta \times F_p} \quad (11)$$

$$\text{where } \alpha_N = \frac{N}{R_F} < 1 \quad (12)$$

$$\beta = \alpha_M \times \alpha_N < \alpha \quad (13)$$

The coefficient β is the frame “duty cycle”, i.e. it represents that part of T_{FRAME} during which the frame pixels are received. From formulas (1) and (11) follows

$$T_{PE}^F \leq \frac{T_p}{\beta \times CC} \quad (14.1)$$

$$F_{PE}^F \geq \beta \times CC \times F_p \quad (14.2)$$

Formulas (14.1) and (14.2) show that the time requirements to the PE are relaxed in comparison to the other two processing configurations, because $\beta < \alpha < 1$. Parameters CC, F_{PE} and F_p could be managed to the desired direction in a greater degree compared to the previous configuration.

The size of the FIFO buffer that contains the waiting frame pixels, is defined by the maximum number of pixels that could be processed during the time of frame blanking T_{FrB} (from the moment in which the last frame pixel is received in the FIFO to the arrival of the first pixel from the next frame). Time duration of processing the pixels remaining in the FIFO buffer should be

$$T_{BUF} = T_{PP}^F \times B_{FRAME} \leq T_{FrB} \quad (15)$$

From the limitation (15) and formula (11) follows

$$B_{FRAME} \leq \frac{T_{FrB}}{T_{PP}^F} = \frac{P_{FrB} \times T_p}{\beta} = \beta \times P_{FrB} \quad (16)$$

D. Parallel processing configuration

All the three configurations, described by now use single PE to deal with the entire data flow. If parallel processing structure with multiple (K) PE is implemented, the timing requirements will be significantly enhanced. Every PE will process $1/K$ part of the data flow and correspondingly the time slot granted to him will be K-times bigger and the required minimum PE clock frequency will be reduced also K-times:

$$T_{PE}^{PP} \leq \frac{K}{CC} \times T_p \quad (17.1)$$

$$F_{PE}^{PP} \geq \frac{CC}{K} \times F_p \quad (17.2)$$

$$T_{PE}^{PL} \leq \frac{K}{\alpha \times CC} \times T_p \quad (17.3)$$

$$F_{PE}^{PL} \geq \alpha \times \frac{CC}{K} \times F_p \quad (17.4)$$

$$T_{PE}^{PF} \leq \frac{K}{\beta \times CC} \times T_p \quad (17.5)$$

$$F_{PE}^{PF} \geq \beta \times \frac{CC}{K} \times F_p \quad (17.6)$$

In case of configuration with FIFO buffers, the total volume is equal to the value defined for a single PE (K=1) case. There could be two different implementations of the FIFO buffer. The first one is presented on fig.4 – one common buffer stores the row (frame) pixel and the distribution to the PE is done after the element extraction from the head of the buffer. The other case makes the separation of the data flow to the individual PE FIFO buffers and the size of each of them is

$$B_{ROW}^P \leq \frac{T_{HB}}{T_{PP}^L} = \frac{P_{HB} \times T_p}{\frac{K \times T_p}{\alpha}} = \frac{\alpha}{K} \times P_{HB} \quad (18.1)$$

$$B_{FRAME}^P \leq \frac{T_{FrB}}{T_{PP}^F} = \frac{P_{FrB} \times T_p}{\frac{K \times T_p}{\beta}} = \frac{\beta}{K} \times P_{FrB} \quad (18.2)$$

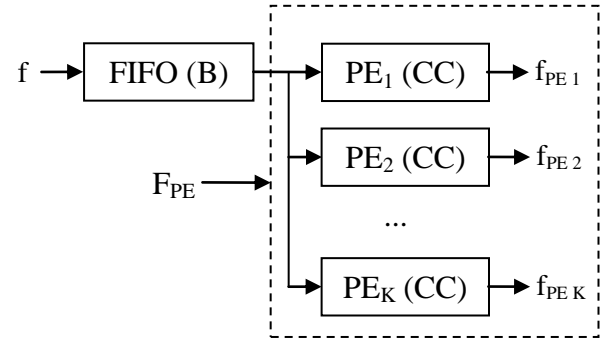


Fig.4. Parallel processing with common FIFO buffer

E. Example

As an example of described configurations an image sensor OV2640 of OmniVision Technologie is analyzed. Fig.5 presents timing diagram of one frame and Table1 includes the basic parameters of the image sensor frame and calculated values of coefficients and buffers sizes for different frame formats.

Table1. Basic parameters of a image sensor frame

Frame format	UXGA	SVGA	CIF	
Rows	N	1600	800	400
Columns	M	1200	600	300
T_{FRAME}	R_F * T_{ROW}	1248	672	336
T_{ROW}	P_R * T_p	1922	1190	595
T_{HB}	P_{HB} * T_p	322	390	195
T_{VB}	P_{VB} * T_p	84890	81310	14398
T_{FB}	P_{FB} * T_p	27193	7415	3707,5
T_{BB}	P_{BB} * T_p	57697	73895	17907,5
T_{FrB}	P_{FrB} * T_p	92578	86070	16778
α=α_M	M/P_R	0,8325	0,6723	0,6723
α_N	N/F_R	0,9615	0,8955	0,8955
β	α_N*α_N	0,8	0,6	0,6
B_{ROW}		269	263	132
B_{FRAME}		74063	51643	14398

III. DISCUSSION

From formulas (3.1), (7.1) and (14.1) it is possible to determine the ratios of the parameter T_{PE} (maximum acceptable time duration for processing one pixel in certain PE) for the different configurations:

$$T_{PE}^P : T_{PE}^L : T_{PE}^F = 1 : \frac{1}{\alpha} : \frac{1}{\beta} \quad (19)$$

Formula (19) shows that the available time for one pixel processing is increasing, but additional memory should be allocated for the FIFO buffers. In One-Row configuration their sizes are relatively small, but in One-Frame case they are significant. Despite of this, they are many times smaller than the memory required for a whole frame.

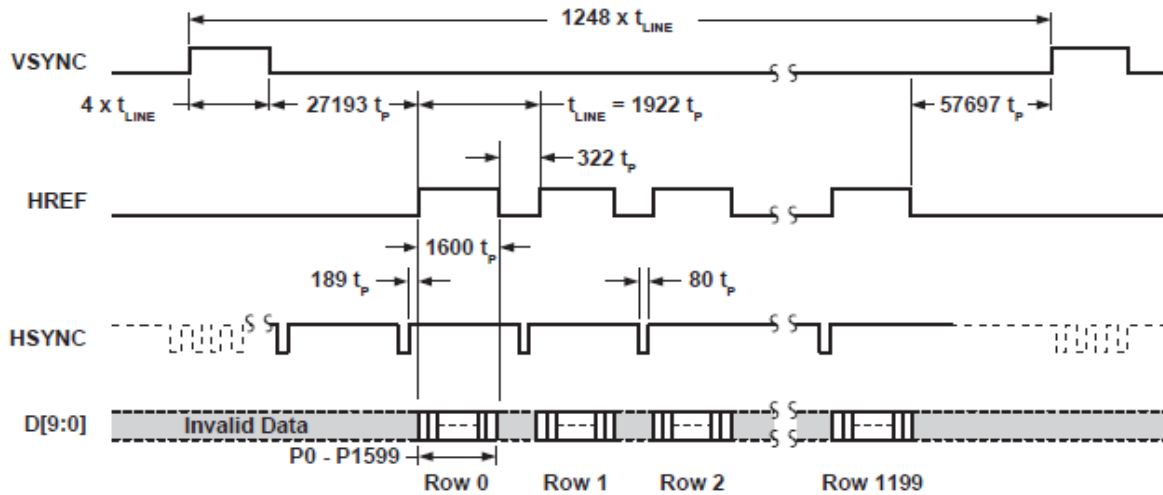


Fig.5 Timing diagram of one frame of OV2640 image sensor

From formulas (3.2), (7.2) and (14.2) it is possible to determine the ratios of the parameter F_{PE} (minimum acceptable clock frequency for a certain PE) for the different configurations:

$$F_{PE}^P : F_{PE}^L : F_{PE}^F = 1 : \alpha : \beta \quad (20)$$

Formula (19) shows that the required minimum PE clock frequency decreases. This is relaxation of the requirement to the image processing system. Other possible decision is to keep higher F_{PE} and to implement other version of the function that requires more clock cycles for execution, but produces better results.

If One-Frame configuration is implemented, the parameters should be calculated with some safety margin, because after the end of the frame processing, some of the following operations could take place:

- Evaluation of the result from the whole frame processing – some functions, for example statistical functions, consider the information from all frame pixels;
- Evaluation and/or additional processing of the information extracted from the frame
- Image sensor configuration adjustments for the next frames.

Presented analysis is build on the assumption that the PE can deal with only one pixel at any given time. If the processing function allows some form of decomposition and rearrangements toward conveyor-type structure that could handle more than one pixel at a time, than the calculations for this PE should be adjusted to the new structure.

Other important assumption was that the pixel data flow is transferred from the image sensor in TV standard frames. A possible example of different data transfer is the usage of the internal output buffer of the image sensor – in this case the pixels are outputted at regular intervals and there are not horizontal and vertical blanking periods. Another case is when data it transferred through some high speed serial interface. If the real image processing system does not work with TV-type frames, only One-Pixel configuration should be considered in single PE or multiple-parallel PE versions.

IV. CONCLUSION

Presented dependencies of the basic timing parameters allow quick and easy evaluation of the PE of a image processing system and detection of potential possibilities for system adjustment and enhancement. By individual configuration of the different PE it is possible to achieve a good balance between the system requirements – energy consumption, frame rate, result accuracy.

REFERENCES

- [1] А. Умбиталиев, А. Цыцулин. *Твердотелная Революция в Телевидении, Радио и связь*, Москва, 2006.
- [2] D. Gajski, *Embedded System Design*, Springer, 2009.
- [3] Пламенка Боровска, Милена Лазарова. *Паралелна информационна обработка: Системни архитектури, Паралелни алгоритми, Паралелно програмиране*. Сиела, София, 2007.
- [4] Георги Михов. *Цифрова схемотехника*. Технически Университет – София, 2008.
- [5] <http://www.ovt.com>
- [6] <http://www.aptna.com>