Investigation of Colpitts VCO Designed on 0.35 µm Technology

Tihomir Sashev Brusev

Abstract – **In this paper is presented Colpitts voltage controlled oscillator (VCO) designed with Cadence on AMS SiGe BiCMOS 0.35 µm technology. The frequency of oscillation f_o of VCO is equal to 2.5 GHz, while the supply voltage V_{DD} of the investigated circuits is equal to 2.5 V. The obtained result shows that phase noise of Colpitts VCO is -103 dBc/Hz at a 100kHz offset and -115.6 dBc/Hz at a 400kHz offset. The f_o of Colpitts VCO can be adjusted from 2.2 GHz to 2.5 GHz, when control voltage is changed in the range between 2.5 V and 0 V.**

Keywords – **Collpits VCO, Integrated circuits (IC), SiGe BiCMOS 0.35 µm technology, Cadence.**

I. Introduction

The wireless communication standard fourth generation Long-Term Evolution (4G LTE) allows transfer of large date packages in the real time, because orthogonal frequency division multiplexing (OFDM) modulation is used. The signal is transferred by several sub-carrier frequencies. Thus the spectrum is used very efficiently [1]. One of main requirements in 4G LTE standard is VCO to have low phase noise [2]. In Fig. 1 is presented the block diagram of wireless transceiver, where PA is power amplifier and LNA is low-noise amplifier [3].

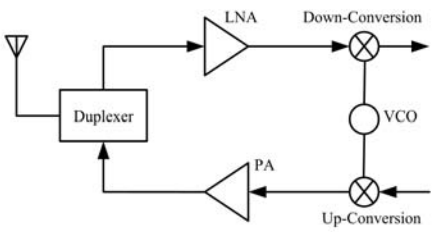

Fig. 1. Block circuit of the wireless transceiver.

The main goal of this paper is to be designed VCO with low phase noise. Cross-coupled LC VCO architectures are widely proposed in the literature as good choice for low phase noise oscillator circuits [4], [5]. The obtained results from this investigation show that Colpitts VCO is an alternative as oscillator with low phase noise performance [5]. Differential Colpitts VCO architecture should be used in the block diagram shown in Fig. 1, when up and down conversion is needed. In this paper is investigated single-ended Colpitts VCO architecture in order to evaluate the feasibility of this circuit.

In Section II*A* of this paper are presented the single-ended Colpitts VCO core and buffer designed on AMS process. For the purpose of this investigation from SiGe BiCMOS 0.35 µm technology are used MOS transistors, capacitors, varicaps and one of the available integrated inductors. The phase noise and frequency tuning characteristic of the Colpitts VCO are presented in Section II*B*.

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II. Investigation of Colpitts VCO

The block circuit of investigated Colpitts VCO is shown in Fig. 2. It consists of VCO and buffer. The load resistor R_L is equal to 50 Ω, while the supply voltage V_{DD} is 2.5 V.

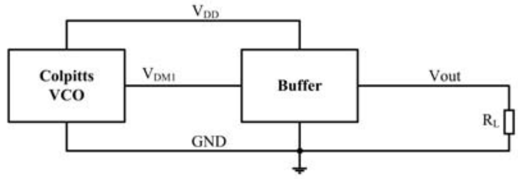

Fig. 2. Block circuit of Colpitts VCO.

A. Colpitts VCO core and buffer

The schematic of the designed Colpitts VCO core is presented in Fig. 3.

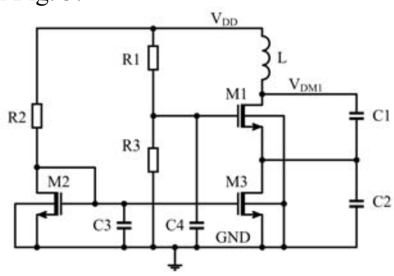

Fig. 3. Schematic of Colpitts VCO.

The frequency of oscillation of the VCO is determined by [6]:

$$f_o = \frac{1}{2\pi\sqrt{L_t C_t}}, \qquad (1)$$

where L_t is total tank inductance and C_t is the total tank capacitance. The spiral integrated inductor SP011S200T is chosen for *L*. Simulated characteristic of inductor's Q-factor as a function of frequency is shown in Fig. 4. The maximum Q-factor obtained at 5.01 GHz is equal to 11.56, while Q-factor at 2.5 GHz is equal to 9.5.

The values of: inductor *L*; feedback capacitors *C1* and *C2*; the sizes of core transistor *M1* of the Colpitts VCO are given in Table 1. The capacitance of *C1* and *C2* respectively is formed by: 18 and 16 "*cpolyrf*" capacitors with values of 330 fF, which are connected in parallel.

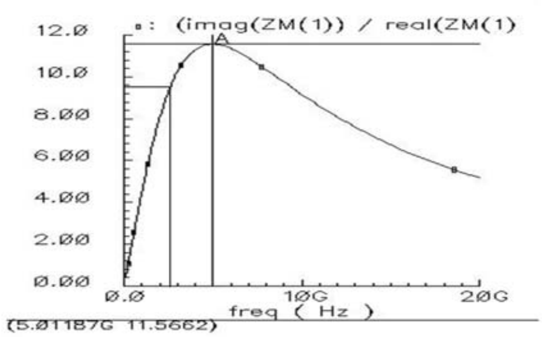

Fig. 4. Q factor as a function of frequency of inductor SP011S200T.

Colpitts VCO's core transistor *M1* is represented by 4 parallel connected "*modnrf*" NMOS transistors. The capacitance of *C3* and *C4* is formed by 16 parallel connected "*cpolyrf*" capacitors with values equal to 1 pF.

TABLE 1. THE VALUES OF INDUCTOR, FEEDBACK CAPACITORS, AND CORE TRANSISTOR SIZE OF COLPITTS VCO CORE

VCO core	L [nH]	C1 [fF]	C2 [fF]	C3=C4 [pF]	M1-W/L [μm]
	1.1	18x330	16x330	16x1	4x(200/0.35)

The schematic of buffer topology is shown in Fig. 5. The output of Colpitts VCO is the drain voltage of transistor *M1* (V_{DM1}), which is connected to input (*Buffer_in*) of the buffer stage. Block circuit of Colpitts VCO and buffer simulated with Cadence is shown in Fig. 6.

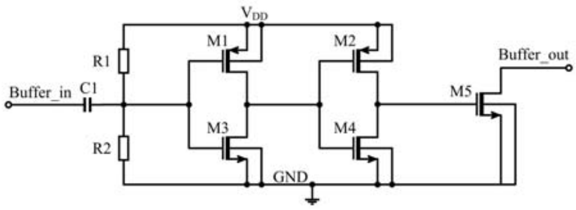

Fig. 5. Schematic of buffer.

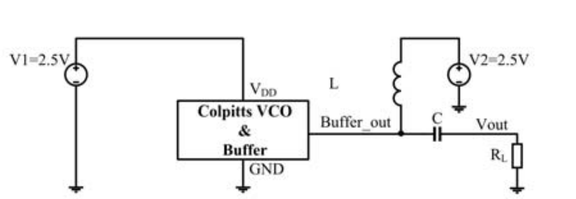

Fig. 6. Simulated Colpitts VCO and buffer block circuit.

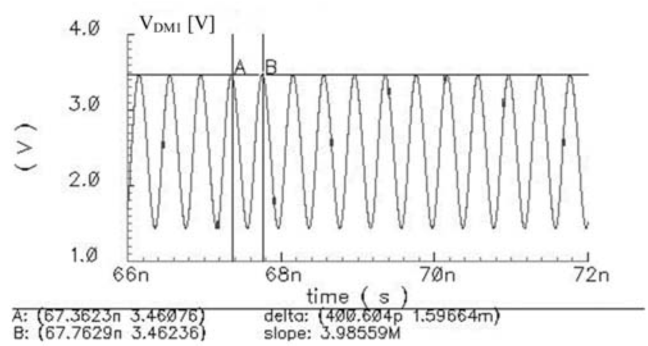

Fig. 7. Drain voltage waveform of transistor M1 V_{DM1}.

The value of load resistor R_L, of the block circuit shown in Fig. 6, is equal to 50 Ω. Simulated waveforms of output voltage of Colpitts VCO (V_{DM1}) are presented in Fig. 7 and Fig. 8.

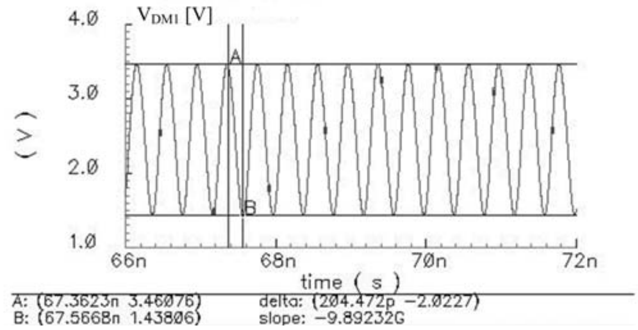

Fig. 8. The peak-to-peak voltage of V_{DM1}.

As can be seen from Fig. 7 the frequency of Colpitts VCO core's output voltage is equal 2.5 GHz. The peak-to-peak voltage of $V_{DM1(p-p)}$ equal to 2.02 V could be seen in Fig. 8. The simulated waveforms of output voltage V_{out} of designed Colpitts VCO and buffer block circuit, shown in Fig. 6, are presented in Fig. 9 and Fig. 10.

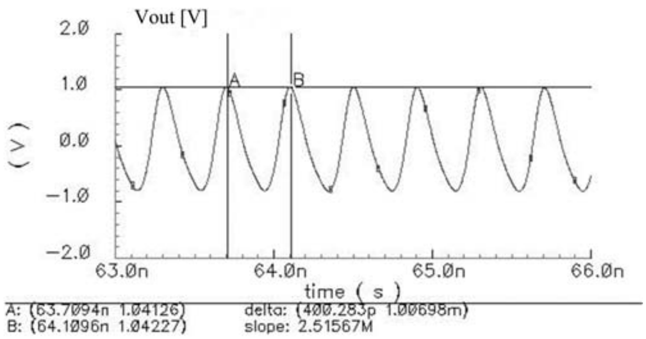

Fig. 9. The simulated waveform of output voltage V_{out}.

As can be seen respectively from Fig. 9 and Fig. 10 frequency of oscillation f_o of Colpitts VCO is equal to 2.5 GHz, while output peak-to-peak voltage $V_{out(p-p)}$ is equal to 1.83 V.

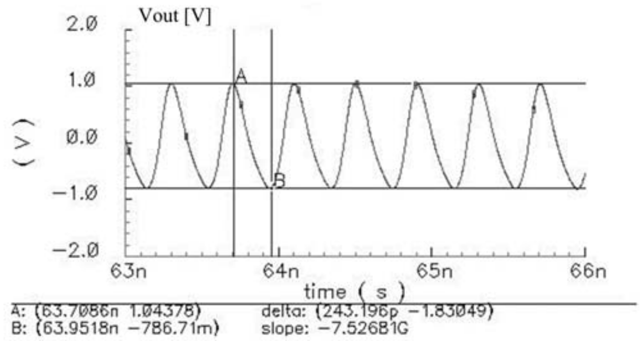

Fig. 10. The peak-to-peak voltage of V_{out}.

The drain current waveform of core transistor *M1* (I_{DM1}) is shown in Fig. 11.

TABLE 2. THE MAIN PARAMETERS OF COLPITTS VCO

Colpitts VCO	f_o [GHz]	$V_{DM1(p-p)}$ [V]	$V_{out(p-p)}$ [V]	$I_{DM1(p-p)}$ [mA]
	2.5	2.02	1.83	45.23

The value of peak-to-peak current $I_{DM1(p-p)}$ is equal to 45.23 mA. The main obtained parameters of the designed Colpitts VCO are summarized in Table. 2.

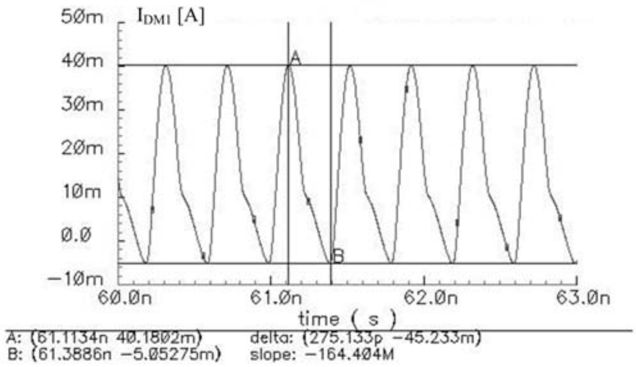

Fig. 11. The waveform of drain current of transistor M1 (I_{DM1}).

B. Phase noise and frequency tuning of designed Colpitts VCO

The phase noise of the oscillators degrades the dynamic range of the receivers [7]. If voltage controlled oscillators have low phase noise, the signal-to-noise ratio of the desired signal can be improved. According to the theory the phase noise can be expressed by [7]:

$$L_{total}\left\{\Delta\omega\right\} = 10.\log\left[\frac{P_{sideband}\left(\omega_0 + \Delta\omega, 1Hz\right)}{P_{carrier}}\right], \qquad (2)$$

where $P_{sidebanh}$ is the single sideband power at the frequency offset $\Delta\omega$ from the carrier with a measurement bandwidth of 1 Hz. $P_{carrier}$ is the total power under power spectrum. The obtained phase noise characteristic of the Colpitts VCO is shown in Fig. 12.

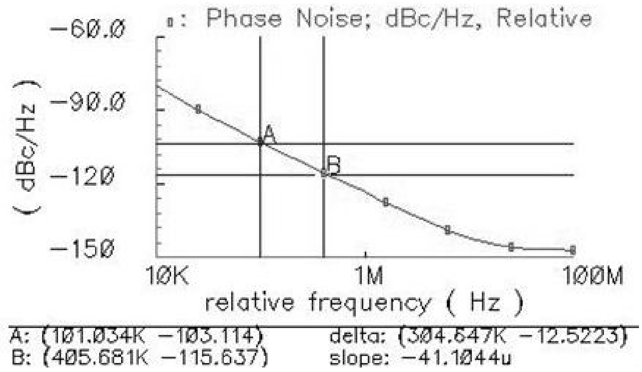

Fig. 12. Phase noise characteristic of designed Colpitts VCO.

The simulated phase noise is equal to -103 dBc/Hz at a 100 kHz offset from 2.5 GHz carrier when Colpitts VCO drawing 20 mA current from a 2.5 V power supply.

TABLE 3. PHASE NOISE OF COLPITTS VCO

Colpitts VCO	Phase Noise @ 100kHz [dBc/Hz]	Phase Noise @ 400kHz [dBc/Hz]
	-103	-115.6

The phase noise at a 400 kHz offset from 2.5 GHz carrier is equal to -115.6 dBc/Hz. The obtained phase noise results of the designed Colpitts VCO are summarized in Table. 3.

The frequency tuning of the investigated Colpitts VCO is performed using MOS varicap "*cvar*", available in the library *PRIMLIB* of the AMS 0.35 μm technology. This voltage controlled capacitance component is connected in parallel with capacitor *C1* of the VCO core shown in Fig. 3. The schematic of Colpitts VCO core with varicap is illustrated in Fig. 13.

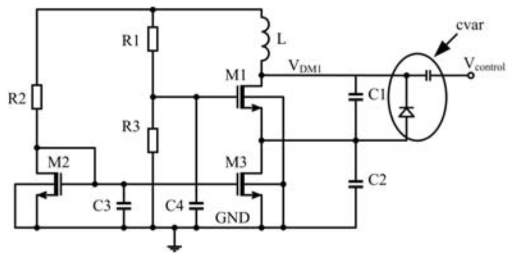

Fig. 13. Schematic of Colpitts VCO core with varicap.

The frequency of oscillation f_o of the investigated Colpitts VCO as function of control voltage $V_{control}$ applied to varicap "cvar" is investigated. The obtained results are presented in Table 4.

TABLE 4. FREQUENCY OF OSCILLATION OF COLPITTS VCO AS FUNCTION VCONTROL

$V_{control}$ [V]	Colpitts VCO f_o [GHz]
0	2.5
0.5	2.4
1	2.35
1.5	2.34
2	2.31
2.5	2.2

The dependence of f_o as function of control voltage $V_{control}$ is graphically presented in Fig. 14.

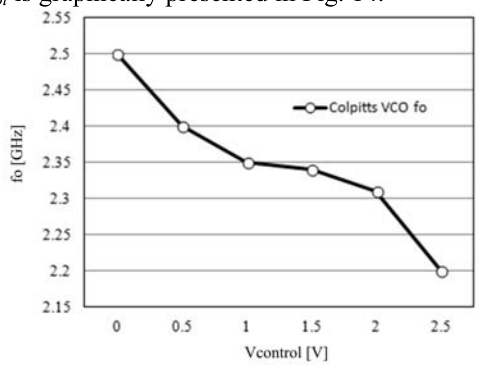

Fig. 14. Frequency of oscillation f_o of Colpitts VCO as function of control voltage $V_{control}$.

The received simulation results show that f_o of Colpitts VCO can be adjusted from 2.5 GHz to 2.2 GHz, when the control voltage $V_{control}$ is changed from 0 V to 2.5 V. The simulated waveform of the voltage V_{DM1}, when $V_{control}$ is equal to 2.5 V, is presented in Fig. 15. In this particular case frequency of oscillation f_o of Colpitts VCO is equal to 2.2 V.

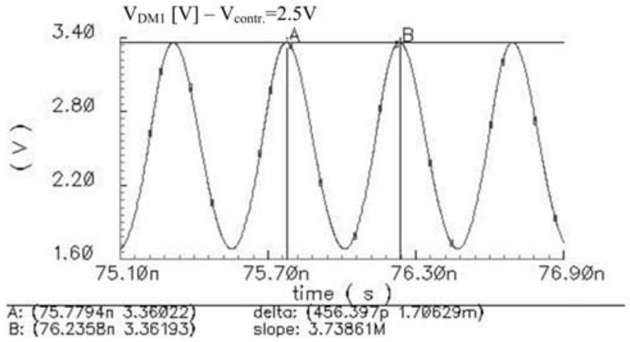

Fig. 15. The waveform of V_{DM1} when $V_{control}$ is equal to 2.5 V.

The layout of Colpitts VCO, designed on AMS SiGe BiCMOS 0.35 μm technology, is presented on Fig. 16.

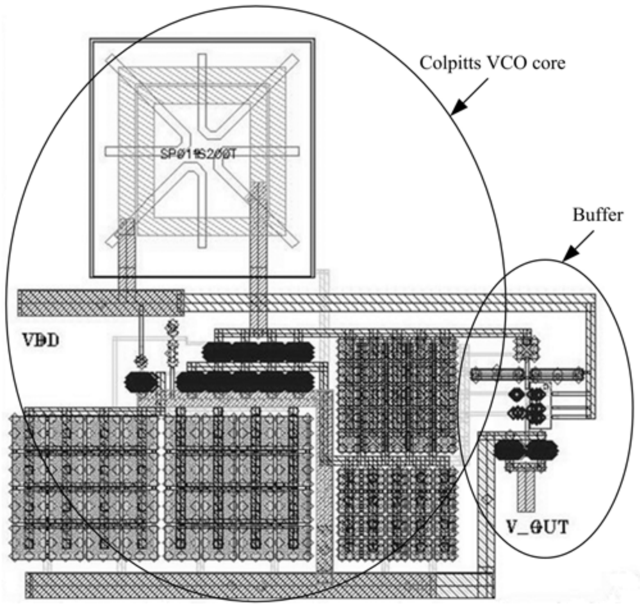

Fig. 16. The layout of Colpitts VCO designed on SiGe BiCMOS 0.35 μm technology.

The occupied silicon area of Colpitts VCO and buffer designed on AMS SiGe BiCMOS 0.35 μm technology is 0.73x0.69 mm^2.

III. CONCLUSION

In this paper is presented Colpiits VCO designed on 0.35 μm technology. The phase noise of the investigated circuit is equal to -103 dBc/Hz at a 100 kHz offset and -115.6 dBc/Hz at a 400 kHz offset from 2.5 GHz carrier frequency. The frequency of oscillation f_o of Colpitts VCO can be adjusted from 2.2 GHz to 2.5 GHz, when the control voltage $V_{control}$ is changed in the range between 2.5 V and 0 V. The obtained results show that Colpitts VCO can be used for wireless communication applications.

ACKNOWLEDGEMENT

The research described in this paper was carried out within the framework of Project 151ПР0011 – 07 – 03.2015.

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