Mains Frequency Deviation Measurement by Using Elements of the Subtraction Procedure Based on Xilinx FPGA

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Abstract -**The subject of the article is an application of a programmable logic devices from the FPGA XILINX family and elements of the subtraction procedurefor the power-line frequency deviation measurement. The synthesized structural diagram includes programmable input attenuator, input stage, analog-to-digital converter, SPI interface unit, CPU core and LCD display. The mains frequency deviation measurement is performed by the soft CPU core implemented in the FPGA. Software algorithms for 'two point' averaging digital filtering and calculation of the mains frequency deviation are developed which minimizes the usage of FPGA resources.**

Keywords– **Frequency Measurement,Mains Frequency, FPGA, Deviation Measurement, Two Point Averaging, FIR Filter, Subtraction Procedure.**

I. INTRODUCTION

The frequency of the utility grid is maintained in tight interval by precisely balancing the amounts of generated and consumed power. For this purpose a high precision measurement of the mains frequency is needed.Typically this is done by direct measurement of the period of the mains voltage and calculating its frequency [1]. The method requires 'direct' signal from the mains. Sometimes in data acquisition systems we need to know the deviation of the mains frequency from its nominal value but cannot use 'direct' mains signal [2]. For this purpose the frequency deviation measurement using the 'two point' FIR digital filter is developed. It offers significant advantages over the classical direct period measurement method:

– does not need a 'direct' signal from the mains

– low sampling rate (200*Hz*) is enough for fast, high accuracy measurement

– does not need dedicated input for the frequency deviation measurement (the 'parasitically' induced hum can be used)

The frequency deviation measurement is implemented on a FPGA (Field-Programmable Gate Array) integrated circuit of Xilinx Spartan-3E family.

The FPGA logic devices are used to implement any logical function.

A Hardware Description Language (HDL) or logical diagrams are used for configuring of the FPGA.

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II. STRUCTURE OF THE MAINS FREQUENCY DEVIATION METER

The structural diagram of the mains frequency deviation meteris represented on Fig. 1. The mains signal is first fed to the input of the programmable attenuator. The right attenuation is chosen so that the signal always remains within the dynamic range of the following stages [5]. Then the signal is fed to the amplifier-limiter where it is buffered and level shifted to the half of the input dynamic range of the ADC (Analog to Digital Converter). Then the signal is fed to the input of the 12-bit ADC. The digital information from the ADC is transferred to the FPGA via SPI interface. All further signal processing is carried by the microprocessor core implemented into the FPGA [6].There is 12-bit RAM (Random Access Memory) implemented into the FPGA [6]. The data from the ADC is stored into the RAM memory during the processing. The results from the calculations are visualized on the LCD display.

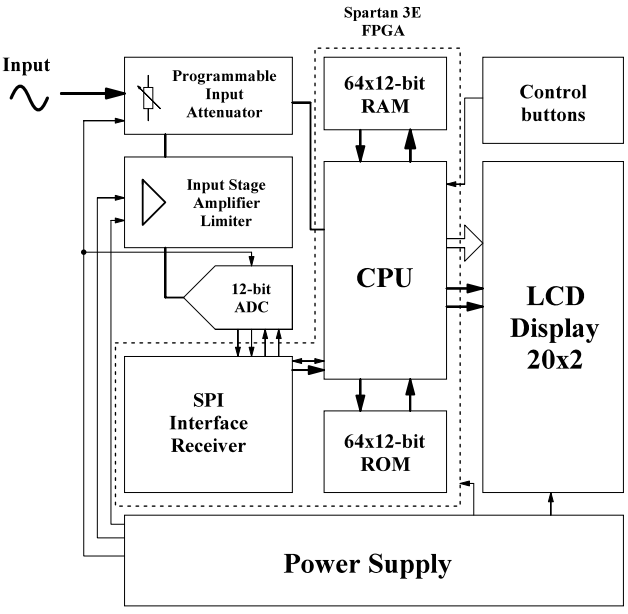

Fig. 1. Multifunctional analyser structural diagram

III. INPUT STAGE

The circuit diagram of the input stage is represented on Fig. 2. The first stage is the input attenuator which is a resistive voltage divider. The attenuation is programmed by switching the resistance to ground by reed relays. There are three different attenuations possible: 1:1; 10:1 and 100:1. The next stage is a non-inverting voltage follower built with the Texas Instruments operational amplifier NE5534.

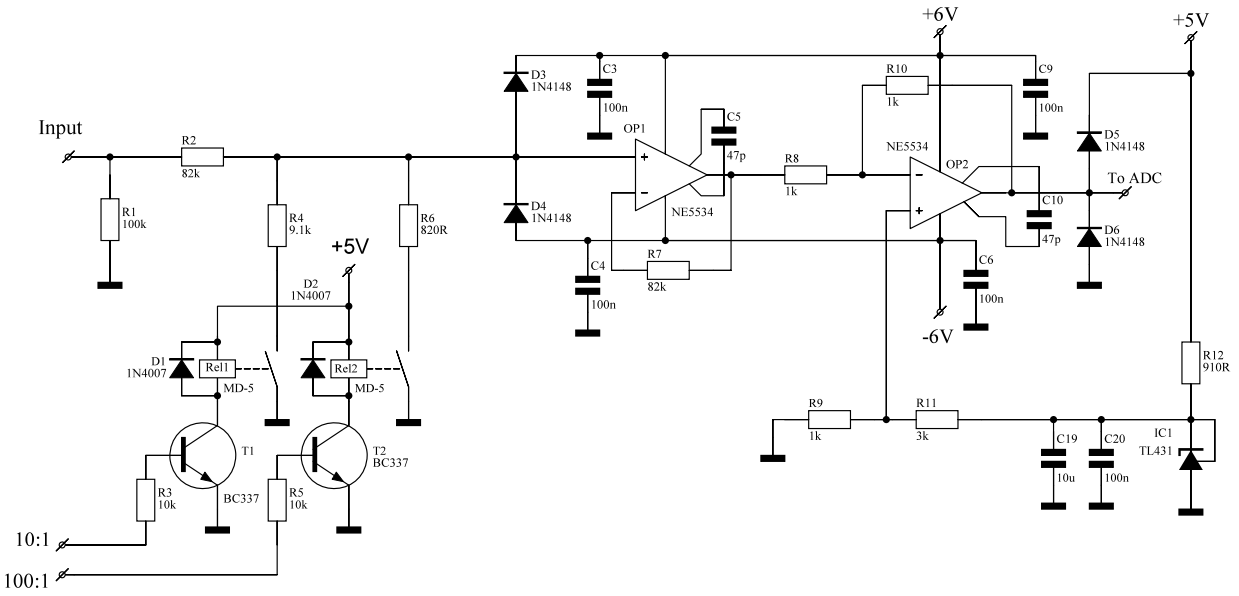

Fig. 2. Input stage schematic diagram

This stage matches the relatively high output impedance of the attenuator with the lower impedance of the next stage. There is a diode limiter at the input of the amplifier for overvoltage protection. The next stage is an inverting amplifier and level shifter. It's function is to shift the level of the signal to the half of the dynamic range of the ADC. This is needed because of the single polarity input range of the ADC. D5 and D6 are overvoltage protection for the ADC input. The bipolar power supply for the operational amplifiers is built with the AIMTEC AM1D-0512DZ DC-DC converter.

IV. Frequency Deviation Measurement Algorithm

The signal samples from the ADC are sent to the FPGA where the microprocessor is performing the software processing. For the purposes of the frequency deviation measurement a 'two point' FIR filter is implemented [3][7]. This is a truncated filter which is performing averaging over two data points in the measured signal period [4]. Its working principle is given by the Eq. (1):

$$Y_i = \frac{X_{i-n/4} + X_{i+n/4}}{2}, \qquad (1)$$

where X_i stands for input samples, Y_i stands for filtered samples, n is the ratio between the sampling rate Φ and the mains frequency F ($n = \Phi/F$).

The value of $n/4$ must be an integer number. That is why a $\Phi = 200$ *Hz* sampling rate is chosen. This is the lowest frequency which is exact multiple of $F = 50$ *Hz* and satisfies the upper condition with its minimal integer value of 1.

The frequency response of the filter is a cosine function with coefficient of 1 for the frequencies $f = 0$ and 0 for the mains frequency $f = F$ (see Eq. 2)

$$K(f) = \cos\frac{\pi n f}{2\Phi}. \qquad (2)$$

The impulse response with the frequency and phase responses of the 'two point' filter are represented on Fig. 3.

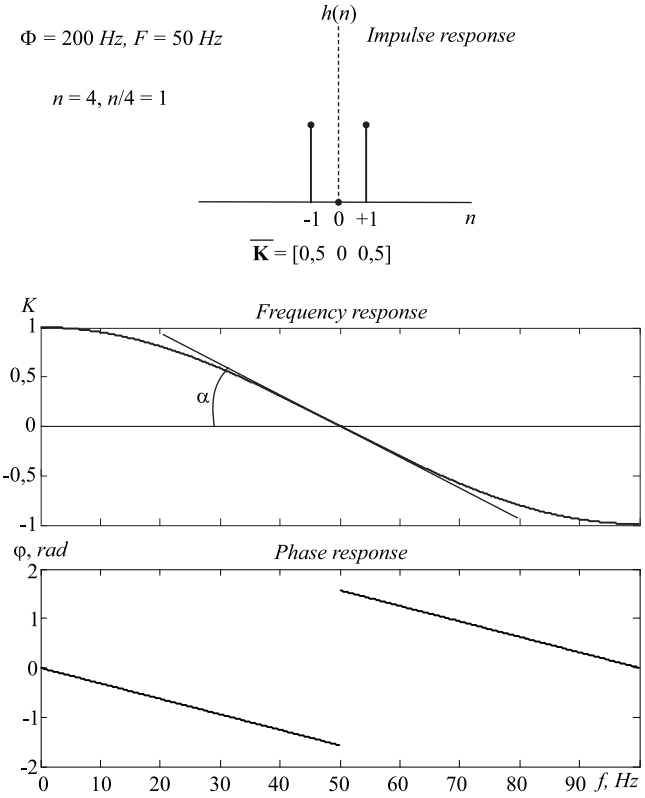

Fig. 3. Filter impulse, frequency and phase responses

For small frequency deviations the transfer function can be approximated according to the formula

$$\frac{\Delta K}{\Delta f} = \tan\alpha. \qquad (3)$$

The usage of 'two point' filter for mains frequency deviation measurement has several major advantages over the rest of the filters:

– simplified calculations are reducing the processor speed needed for real time operation;
– the transfer function of the filter crosses steeply the *x* axis at 50 *Hz* this leads to better sensitivity of the frequency deviation measurement;
– the transfer function crosses the *x* axis symmetrically which reduces the measurement error and it is equivalent for positive and negative frequency deviations.

For the chosen sampling rate Φ = 200 *Hz* the equations are significantly simplified.The current output sample is calculated by

$$Y_i = \frac{X_{i-1} + X_{i+1}}{2}. \quad (4)$$

The difference between the current output sample and the corresponding input sample represent samples B_i of the power-line signal. It is calculated by

$$B_i = X_i - Y_i, \quad (5)$$

and stored into a temporary buffer.
The frequency deviation is calculated using the formula

$$\Delta f \approx -K(f)\frac{\Phi}{2\pi}, \quad (6)$$

where$K(f)$ is given by

$$K(f) = \frac{B_i - B_{i-4}}{2(B_{i-1} - B_{i-3})}. \quad (7)$$

Using these equations the deviation of the mains frequency can be calculated fast and easily.

V. Experimental Results

The input stage testing is performed with PC with a 16-bit 192kHz sampling rate sound card and installed Right Mark Audio Analyzer software. The software performs automatic measurement of various parameters of an audio system. It generates testing signals which are fed from the Line-out of the sound card to the tested circuitry. Then the signal from the output of the tested circuitry is fed back to the sound card Line-in input.

The following parameters are tested: frequency response, noise level, dynamic range, THD + noise, intermodulation distortion and crosstalk between channels.

The testing shows a frequency response from DC to 40 kHz ±0.25 dB (Fig. 4), noise level below -70 dB, THD lower than 0.04% (Fig. 5), inter modulation distortion lower than 0.2 % in the whole spectrum from 1 kHz to 50 kHz and inter-channel crosstalk about -42 dB.

The measurement of the mains frequency deviation using the ‘two point’ FIR filter is showing good results with high accuracy. The required processing speed for a real time operation is small. The algorithm is tested in MATLAB and the results are represented on figure 6, 7 and 9. The real frequency of the test signal is represented by the red graph, and the measured frequency with the ‘two point’ filter method is represented by the black graph. The two graphs are closely matching and for that reason for better visibility they are slightly misaligned.

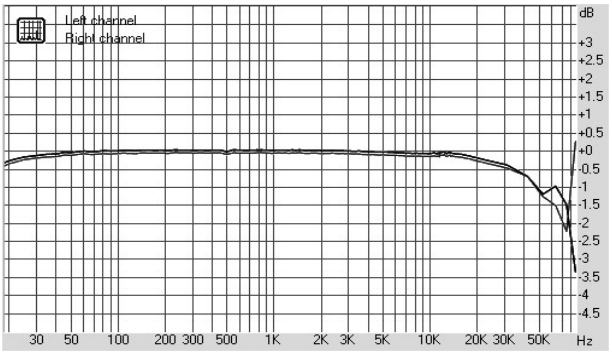

Fig. 4.Input stage frequency response

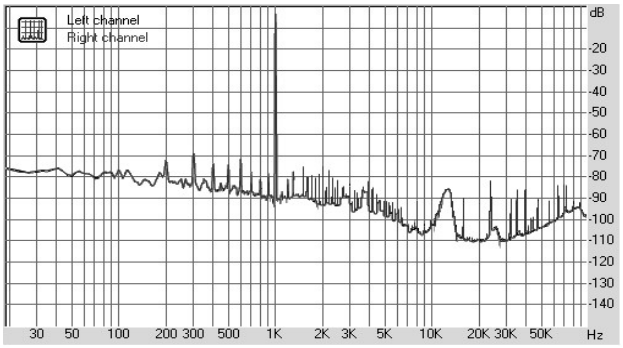

Fig. 5.Input stage spectrum of the output signal with 1 kHz sine wave test signal

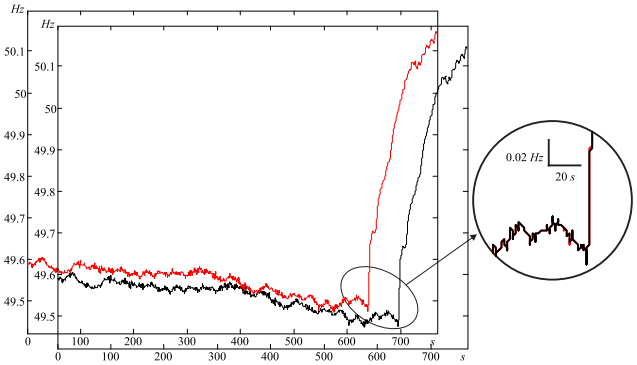

Fig. 6.The actual mains frequency and the measured frequency

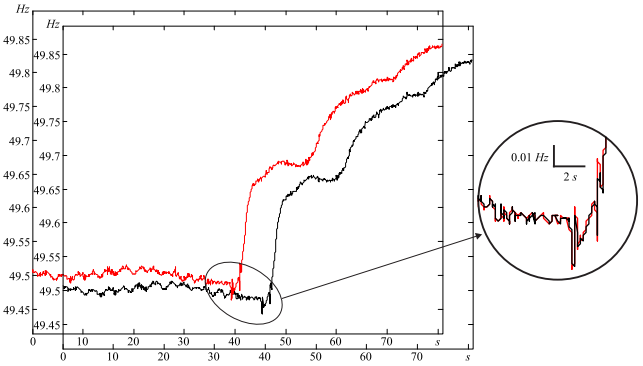

Fig. 7. The actual mains frequency and the measured frequency

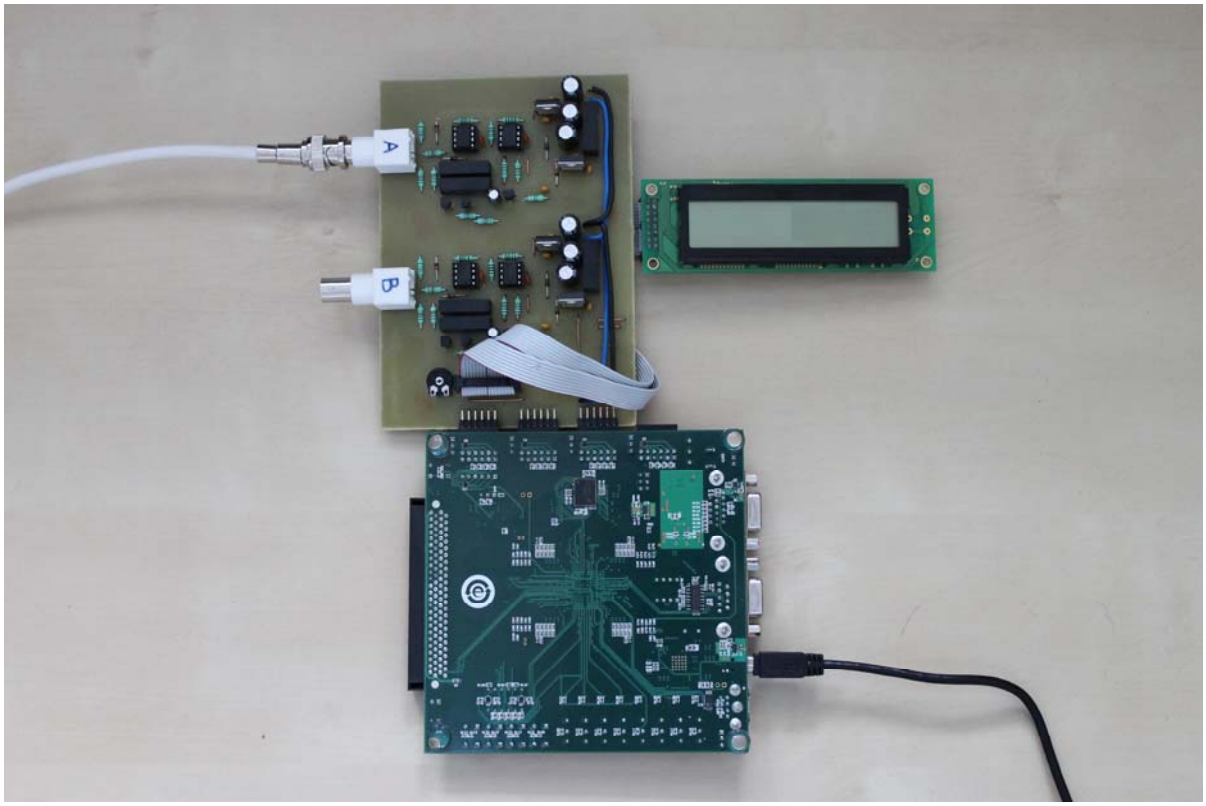

Fig. 8.Developed board with input attenuators, input stages, power supply, ADC and LCD display

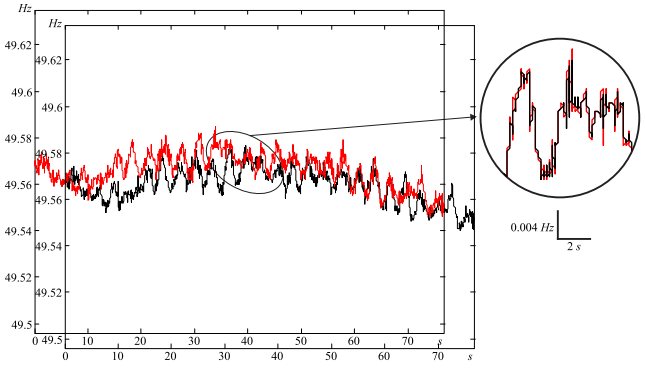

Fig. 9. The actual mains frequency and the measured frequency

VI. Conclusion

The results from the input stage testing are showing good flat frequency response.

The noise level of -70 dB is low enough to prove the concept but a good point for development is lowering the noise floor up to at least a –100 dB. This can be achieved by using resonant DC-DC converters for power supply, as well as using a lower noise operational amplifiers.

The 'two point'filter method for mains frequency deviation is showing good accuracy over a wide range of mains interference amplitudes. This makes it possible to implement the method in different embedded systems where the exact mains frequency is important to be known. It can be used in further signal processing for mains interference suppression.

References

[1] Ст. Овчаров, Н. Тюлиев, П. Якимов. *Система за следенечестотата на електрическата мрежа*, Трета национална научно-приложна конференция с международно участие Електронна Техника ЕТ'94. Септември 28-30, Созопол, т. I, стр. 98-103, 1994.

[2] I. Dotsinsky, T.Stoyanov. *Cancellation of the power-line interference: effect of amplitude and frequency variations on the ECG signal*, Proceedings of the 11-th International Conference ELECTRONICS – ET'2000, September 25–27, Sozopol, book 2, pp. 65-70, 2000.

[3] C.Levkov, G.Mihov, R.Ivanov, I. Daskalov, I.Christov, I.Dotsinsky. *Subtraction Method for Powerline Interference Removing from ECG,* The Thirteenth International Scientific and Applied Science Conference ELECTRONICS ET'2004, b. 1, September 22-24, Sozopol, pp. 3-14, 2004.

[4] G.Mihov, R. Ivanov, C.Levkov, *Subtraction Method for Removing Powerline Interference from ECG in Case of Frequency Deviation*. Proceedings of the Technical University – Sofia, Vol. 56, b. 2, pp. 212-217, 2006.

[5] *Cygnal Improving ADC Resolution By Oversampling and Averaging*, Application Note, May 2001, pp. 1-21.

[6] *Xilinx Spartan-3E Libraries Guide for Schematic Designs*, UG618, September 16, 2009.

[7] G.Mihov, *Измерване на честота и на амплитуда на мрежови смущения чрез субтракционната процедура*. Годишник на Технически университет – София, Том. 62, книга. 4, стр. 189-198, 2012.