Graphical Representations for Analog IC Design in Deep and Ultra-Deep Submicron CMOS

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Abstract – The paper presents a set of simulation experiments for characterization and graphical representation of the performance of deep and ultra-deep submicron CMOS transistors. The aim is to propose a general approach for illustration of the basic capabilities and limitations of tested CMOS technologies. The results are used to determine the bias conditions and the sizes of the transistors in analog integrated circuit design.

To this goal the key figures of merit for characterizing of CMOS technologies are discussed and test circuits for their examination by simulation are presented. The test circuits are applied for study of 45nm ultra-deep submicron CMOS technology. The obtained results are analyzed and recommendations and simple rules of thumb for application of the presented approach in practice are given.

Keywords – submicron CMOS, figure of merit, intrinsic gain, unity gain frequency

I. INTRODUCTION

Reducing the channel length of the transistors is the leading trend in modern CMOS technologies. Table 1 shows the evolution of submicron CMOS technologies over the past 30 years [1, 2].

<table>
<thead>
<tr>
<th>Type</th>
<th>Period</th>
<th>Channel length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Submicron</td>
<td>1985 - 1995</td>
<td>1µm&gt;L_min&gt;0.35µm</td>
</tr>
<tr>
<td>Deep submicron</td>
<td>1995 - 2003</td>
<td>0.35µm&gt;L_min&gt;0.1µm</td>
</tr>
<tr>
<td>Ultra-deep</td>
<td>2003 - 2015</td>
<td>0.1µm &gt;L_min&gt;0.01µm</td>
</tr>
</tbody>
</table>

II. BASIC PERFORMANCE INDICATORS FOR CMOS TECHNOLOGIES CHARACTERIZATION

The selection of optimal channel length of the transistors is the key decision in initial phase of the design of analog integrated circuits. The channel length is an important factor that determines the operating area, unity-gain frequency and intrinsic (open loop) gain. The next step in the design procedure is determination of bias conditions and sizing of transistor’s width.

Fig. 1 presents the transconductance of 45nm nMOS transistor in saturation (L=2L_min=90nm, W=1µm, U_DDS=U_DDS=1V) versus gate source voltage U_GS.

The plot can be divided in three regions of operation [6, 7]: subthreshold or weak inversion (wi) – U_GS < U_DDS; square-law or strong inversion (si) – U_GS between 450 mV and 620 mV and g_m between 230 µA/V and 925 µA/V; velocity saturation (vs) – U_GS above 620 mV and g_m from 925 µA/V up to 1.3 mA/V.

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The weak inversion is characterized with small currents. The operation in this region is appropriate for very low-power analog applications [8]. The main disadvantage is the low-speed.

Velocity saturation occurs at high gate-source voltages. It can be modeled by adding a source degeneration resistor towards the transistor [1, 9]. The operation in this region is used only when very high speed is required. Then the transistors have to be with low sizes in order to ensure minimal parasitic capacitances.

The classical analog design is performed in central area of strong inversion [7, 10], where the drain current is directly proportional to the square of the effective voltage $U_{\text{eff}}=U_G-U_T$ and the transconductance $g_m$ versus $U_{\text{eff}}=U_G-U_T$ is linear. In modern short channel technologies this sector is very narrow (reduced overdrive voltage), which complicates the design. One of the purposes of our study will be the examination of how the use of a channel, which is larger than the minimum allowed lengths $L_{\text{min}}$, helps to minimize the velocity saturation and enlarges square-law region.

Another key indicator is the unity-gain frequency [7, 9, 10]. Generally it is well known that unity-gain frequency is directly proportional to the gate overdrive voltage and inversely proportional to the square of the channel length, but in the design it is important to know the specific nature of these features for the particular technology used.

The intrinsic gain presents the maximum possible small-signal low frequency gain of the transistor [7, 9, 10]. It is a function of the overdrive voltage and the channel length.

The above discussed characteristics and indicators lead to the conclusion that the channel length and the gate-source biasing voltage $U_{GS}$ are the basic parameters, which determine the performance of the designed circuits. Our goal is to give a procedure for creation of appropriate charts which illustrate the described relations and are a basis for successful electrical design and sizing of analog integrated circuits.

III. EXAMINATION AND VISUALIZATION OF BASIC PERFORMANCE INDICATORS

A. Transconductance $g_m$ versus channel length $L$ and gate-source voltage $U_{GS}$

Fig. 2 presents the test circuit for study transconductance $g_m$ vs. channel length $L$ and gate-source voltage $U_{GS}$.

The simulations are carried out by using LTspice [11]. W/L ratio at all simulations remains 1. The obtained results are shown on Fig. 3. It can be concluded that increasing the channel length of the transistor leads to widening of the field of strong inversion. For example, increasing the channel length from $2\cdot L_{\text{min}}$ to $10\cdot L_{\text{min}}$ expands the strong inversion region by more than 200 mV. Unfortunately, as we shall see later, this possibility is limited due to reduced bandwidth and increased surface area of the chip.

B. Unity gain frequency $f_u$ versus channel length $L$ and gate-source voltage $U_{GS}$

Fig. 4 shows the test circuit for examination of unity-gain frequency $f_u$ versus channel length $L$ and gate-source voltage $U_{GS}$. For this purpose, series of simulations were carried out with an argument $L$ at different values of the parameter $U_{GS}$ and $W/L=1$.

Fig. 5 presents the results of the simulations. The highest values of the unity-gain frequency are obtained at short channel ($L=2\cdot L_{\text{min}}$) for values of $U_{GS}$ in velocity saturation. In strong inversion the frequency $f_u$ depends almost linearly on the bias point (gate-source voltage $U_{GS}$), while in the velocity saturation $f_u$ practically does not change. In strong inversion the frequency $f_u$ is inversely proportional of the square of the channel length $L$, while in the velocity saturation this relation is weaker.
C. Intrinsic gain $A_u$ versus channel length $L$ and gate-source voltage $U_{GS}$

The proposed test circuit for simulation of the intrinsic gain of the transistor is shown on Fig. 6. The parameter $S$ is set of 1, so $W / L$ is 1 again. To provide an open AC circuit, an ideal current source $F_1$ is used as a load. To obtain an adequate result, the currents through examined transistor $M$ and the load $F_1$ have to be equal. To this aim an additional transistor $M_1$, identical with $M$, is used. Because of the same $U_{GS}$ voltage of both transistors, the current through $M_1$ is equal to the current through $M$. The input of current controlled current source $V-F_1$ is a load to the $M_1$. Hence, because the current transfer coefficient is 1, the current through $F_1$ is equal to the current through $V$ and consequently to currents through $M_1$ and $M$.

The results from simulations are generalized on Fig. 7. As long as the channel length $L$ is larger, the intrinsic gain $A_u$ is greater. The maximum gain is obtained with a voltage between 0.45 V and 0.55 V, i.e. when the transistor is in strong inversion (see Fig. 1). The values of maximum are from 60 (when $L=2\cdot L_{\text{min}}$), up to 440 (when $L=15\cdot L_{\text{min}}$).

D. Gain product versus channel length $L$ and gate-source voltage $U_{GS}$

The presented Fig. 5 and Fig. 7 show one of the big trade-off in the analog circuit design – for high unity-gain frequency $f_u$ the channel length $L$ have to be smaller, while for a big intrinsic gain $A_u$ the channel length $L$ have to be larger. Therefore, we can never achieve both maximum gain and bandwidth of an amplifier – if the frequency increases, the gain decreases and vice versa.

Another figure of merit that is useful to evaluate practically different amplifier circuits is the gain-to-unity-gain frequency product $A_u\cdot f_u$ [10]. This quantity is presented on Fig. 8, where gate-source voltage $U_{GS}$ is argument and channel length $L$ is parameter. It is obtained...
through multiplication of the results of simulation of unity-gain frequency \( f_u \) and intrinsic gain \( A_u \) for different values of channel length \( L \) and gate-source voltage \( U_{GS} \). As long as the channel length \( L \) is larger, the gain-to-unity-gain frequency product \( A_u f_u \) is smaller.

Using the provided graphs, designers can choose better values of the channel length and bias condition \( U_{GS} \) for every transistor in the circuit.

IV. CONCLUSION

The paper presents a set of simulation experiments for characterization and graphical representation of the performance of deep and ultra-deep submicron CMOS transistors in dependence of channel length \( L \) and bias conditions \( U_{GS} \).

To this aim the key performance indicators as transconductance \( g_m \), unity-gain frequency \( f_u \), intrinsic gain \( A_u \) and gain-to-unity-gain frequency product \( A_u f_u \) are discussed. Test circuits for evaluation of these indicators by simulation are presented.

The proposed approach is applied to the nMOS transistor from 45nm CMOS technology. The obtained results give detailed and demonstrative illustration of the characteristics of the transistor for different values of channel length \( L \) and bias conditions \( U_{GS} \).

The results can be used to determine the operating point and the sizes of the transistors in analog integrated circuit design.

REFERENCES