Graphical Representations for Analog IC Design in Deep and Ultra-Deep Submicron CMOS

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Abstract – **The paper presents a set of simulation experiments for characterization and graphical representation of the performance of deep and ultra-deep submicron CMOS transistors. The aim is to propose a general approach for illustration of the basic capabilities and limitations of tested CMOS technologies. The results are used to determine the bias conditions and the sizes of the transistors in analog integrated circuit design.**

To this goal the key figures of merit for characterizing of CMOS technologies are discussed and test circuits for their examination by simulation are presented. The test circuits are applied for study of 45nm ultra-deep submicron CMOS technology. The obtained results are analyzed and recommendations and simple rules of thumbs for application of the presented approach in practice are given.

Keywords – **submicron CMOS, figure of merit, intrinsic gain, unity gain frequency**

I. Introduction

Reducing the channel length of the transistors is the leading trend in modern CMOS technologies. Table 1 shows the evolution of submicron CMOS technologies over the past 30 years [1, 2].

TABLE 1. EVOLUTION OF SUBMICRON CMOS TECHNOLOGIES

Type	Period	Channel length
Submicron	1985 - 1995	1µm>L_{min}>0.35µm
Deep submicron	1995 - 2003	0.35µm>L_{min}>0.1µm
Ultra-deep submicron	2003 - 2015	0.1µm >L_{min}>0.01µm

The reduction of the channel length of the transistors complicates the hand calculation models and hence the procedures of analog circuits design. The designer has to comply with a number of emerging effects and dependencies. They are studied in detail in the literature and as a result are described by complex expressions, which usually serve as guidelines in initial design [3, 4, 5]. Increasingly the designer's experience becomes a decisive factor in the design. Currently, the design of analog circuits combines the requirements for thorough knowledge of the physical phenomena and processes in semiconductors, the opportunity to work with abstract patterns and creativity to balance between the requirements and the limitations of performance. Analog design becomes a symbiosis between cutting-edge science and art.

In this situation, the task of teaching design of analog integrated circuits becomes extremely complex and responsible. Inexperienced trial-and-errors approach leads to longer design times and usually ends with redesign. Hence beginner designers should be directed consistently and with small steps towards mastering successful strategies and approaches to design.

In most analog applications, MOS transistor is used as an amplifier. To this end, it works in the field of saturation, where U_{GS}-U_T <U_{DS}. The first task that must be solved in the design of analog integrated circuits is to choose two main design parameters – gate-source voltage U_{GS} and channel length L. This is done intuitively by skilled designers, based on their experience, gained in development of many projects with different technologies. Students and beginners, however, require additional information to summarize and visualize in a compact form characteristics, capabilities and limitations of each particular used technology. Examples of such information are graphical represented figures of merit.

The paper presents a set of simulation experiments for characterization and graphical representation of the performance of deep and ultra-deep submicron CMOS transistors. The aim is to propose general approach for illustration of the basic capabilities and limitations of tested CMOS technologies. The results can be used to determine the bias conditions and the sizes of the transistors in analog integrated circuit design.

To this goal, key figures of merit for characterizing of CMOS technologies are discussed and test circuits for their examination by simulation are presented. The test circuits are applied for study of 45nm ultra-deep submicron CMOS technology, presented in [2] with BSIM4 model card for bulk CMOS. The obtained results are analyzed and recommendations and simple rules of thumbs for application of the presented approach in practice are given.

II. Basic Performance Indicators for CMOS Technologies Characterization

The selection of optimal channel length of the transistors is the key decision in initial phase of the design of analog integrated circuits. The channel length is an important factor that determines the operating area, unity-gain frequency and intrinsic (open loop) gain. The next step in the design procedure is determination of bias conditions and sizing of transistor's width.

Fig. 1 presents the transconductance of 45nm nMOS transistor in saturation ($L=2L_{min}$=90nm, W=1µm, $U_{DS}=U_{DD}$=1V) versus gate source voltage U_{GS}.

The plot can be divided in three regions of operation [6, 7]: subthreshold or weak inversion (wi) – U_{GS} from 0 V up to 450 mV and g_m from 0 µA/V up to 230 µA/V; square-law or strong inversion (si) – U_{GS} between 450 mV and 620 mV and g_m between 230 µA/V and 925 µA/V; velocity saturation (vs) – U_{GS} above 620 mV and g_m from 925 µA/V up to 1.3 mA/V.

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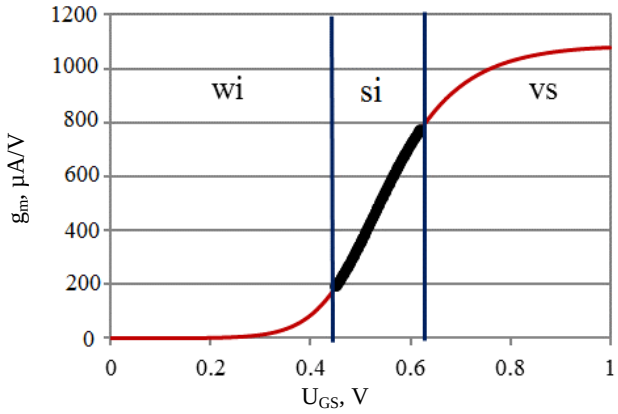

Fig. 1. Transconductance g_m, µA/V vs. gate-source voltage U_{GS},V.

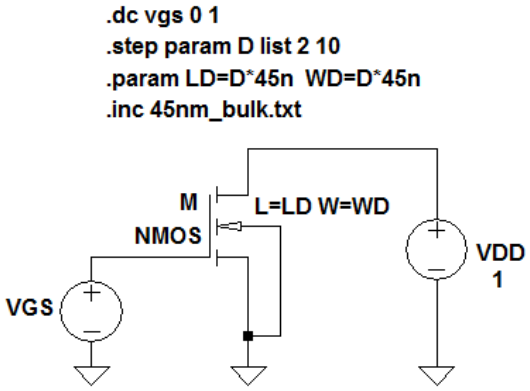

Fig. 2. Test circuit for study g_m vs. L and U_{GS}.

The weak inversion is characterized with small currents. The operation in this region is appropriate for very low-power analog applications [8]. The main disadvantage is the low-speed.

Velocity saturation occurs at high gate-source voltages. It can be modeled by adding a source degeneration resistor towards the transistor [1, 9]. The operation in this region is used only when very high speed is required. Then the transistors have to be with low sizes in order to ensure minimal parasitic capacitances.

The classical analog design is performed in central area of strong inversion [7, 10], where the drain current is directly proportional to the square of the effective voltage $U_{eff}=U_G-U_T$ and the transconductance g_m versus $U_{eff}=U_G-U_T$ is linear. In modern short channel technologies this sector is very narrow (reduced overdrive voltage), which complicates the design. One of the purposes of our study will be the examination of how the use of a channel, which is larger than the minimum allowed lengths Lmin, helps to minimize the velocity saturation and enlarges square-law region.

Another key indicator is the unity-gain frequency [7, 9, 10]. Generally it is well known that unity-gain frequency is directly proportional to the gate overdrive voltage and inversely proportional to the square of the channel length, but in the design it is important to know the specific nature of these features for the particular technology used.

The intrinsic gain presents the maximum possible small-signal low frequency gain of the transistor [7, 9, 10]. It is a function of the overdrive voltage and the channel length.

The above discussed characteristics and indicators lead to the conclusion that the channel length and the gate-source biasing voltage U_{GS} are the basic parameters, which determine the performance of the designed circuits. Our goal is to give a procedure for creation of appropriate charts which illustrate the described relations and are a basis for successful electrical design and sizing of analog integrated circuits.

III. Examination and Visualization of Basic Performance Indicators

A. Transconductance g_m versus channel length L and gate-source voltage U_{GS}

Fig. 2 presents the test circuit for study transconductance g_m vs. channel length L and gate-source voltage U_{GS}.

The simulations are carried out by using LTspice [11]. W/L ratio at all simulations remains 1. The obtained results are shown on Fig. 3. It can be concluded that increasing the channel length of the transistor leads to widening of the field of strong inversion. For example, increasing the channel length from 2·Lmin to 10·Lmin expands the strong inversion region by more than 200 mV. Unfortunately, as we shall see later, this possibility is limited due to reduced bandwidth and increased surface area of the chip.

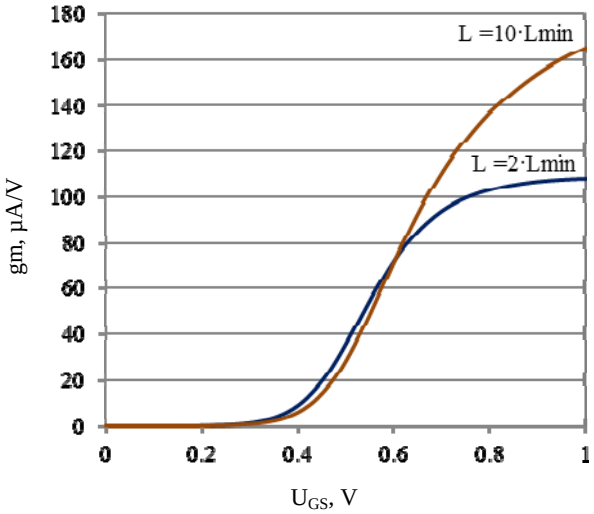

Fig. 3. Transconductance g_m vs. L and U_{GS}.

B. Unity gain frequency f_u versus channel length L and gate-source voltage U_{GS}

Fig. 4 shows the test circuit for examination of unity-gain frequency f_u versus channel length L and gate-source voltage U_{GS}. For this purpose, series of simulations were carried out with an argument L at different values of the parameter U_{GS} and W/L=1.

Fig. 5 presents the results of the simulations. The highest values of the unity-gain frequency are obtained at short channel (L=2·Lmin) for values of U_{GS} in velocity saturation. In strong inversion the frequency f_u depends almost linearly on the bias point (gate-source voltage U_{GS}), while in the velocity saturation f_u practically does not change. In strong inversion the frequency f_u is inversely proportional of the square of the channel length L, while in the velocity saturation this relation is weaker.

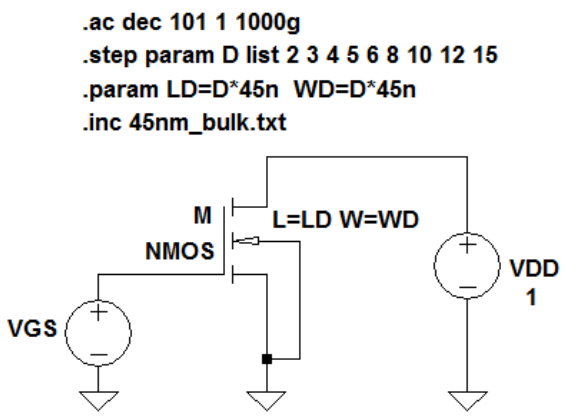

Fig. 4. Test circuit for study f_u vs. L and U_{GS}.

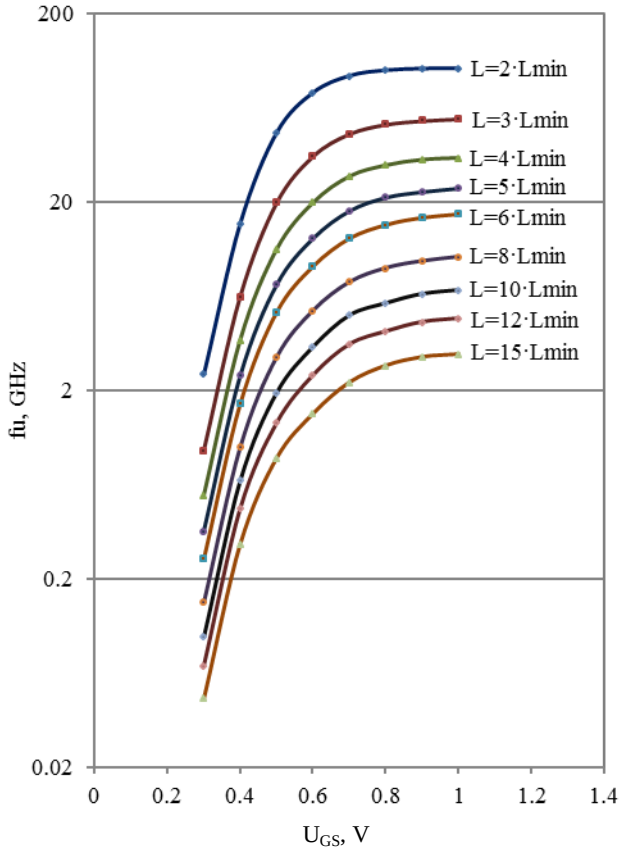

Fig. 5. Unity gain frequency f_u vs. L and U_{GS}.

C. Intrinsic gain A_u versus channel length L and gate-source voltage U_{GS}

The proposed test circuit for simulation of the intrinsic gain of the transistor is shown on Fig. 6. The parameter S is set of 1, so W / L is 1 again. To provide an open AC circuit, an ideal current source F1 is used as a load. To obtain an adequate result, the currents through examined transistor M and the load F1 have to be equal. To this aim an additional transistor M1, identical with M, is used. Because of the same U_{GS} voltage of both transistors, the current through M1 is equal to the current through M. The input of current controlled current source V-F1 is a load to the M1. Hence, because the current transfer coefficient is 1, the current through F1 is equal to the current through V and consequently to currents through M1 and M.

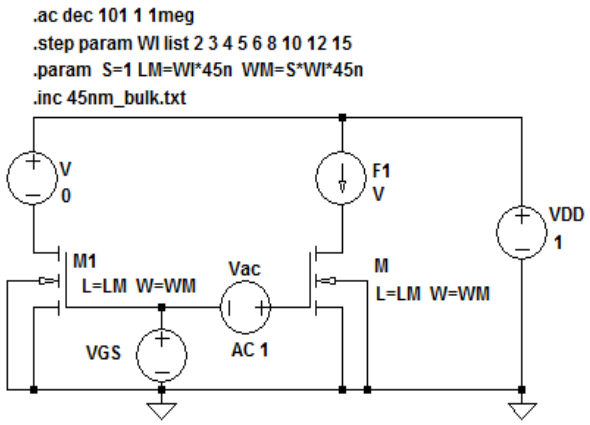

Fig. 6. Test circuits for study A_u vs. L and U_{GS}.

The results from simulations are generalized on Fig. 7. As long as the channel length L is larger, the intrinsic gain A_u is greater. The maximum gain is obtained with a voltage between 0.45 V and 0.55 V, i.e. when the transistor is in strong inversion (see Fig. 1). The values of maximum are from 60 (when L=2·Lmin), up to 440 (when L=15·Lmin).

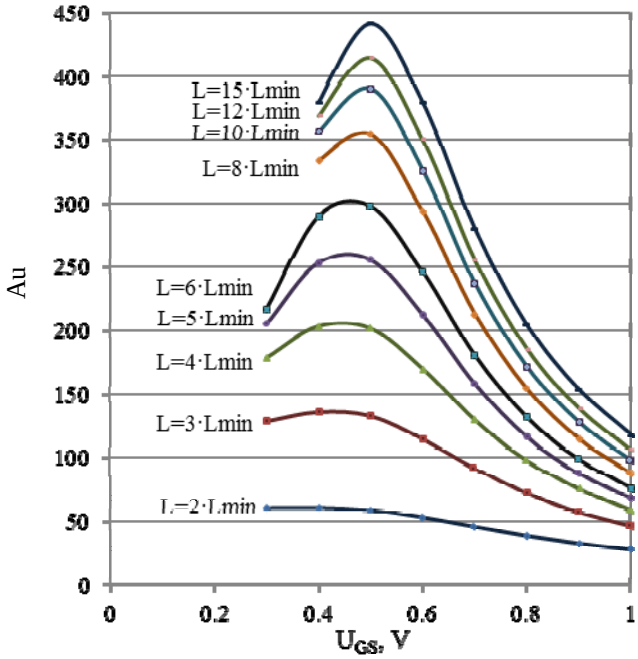

Fig. 7. Intrinsic gain A_u vs. L and U_{GS}.

D. Gain product versus channel length L and gate-source voltage U_{GS}

The presented Fig. 5 and Fig. 7 show one of the big trade-off in the analog circuit design – for high unity-gain frequency f_u the channel length L have to be smaller, while for a big intrinsic gain A_u the channel length L have to be larger. Therefore, we can never achieve both maximum gain and bandwidth of an amplifier – if the frequency increases, the gain decreases and vice versa.

Another figure of merit that is useful to evaluate practically different amplifier circuits is the gain-to-unity-gain frequency product $A_u \cdot f_u$ [10]. This quantity is presented on Fig. 8, where gate-source voltage U_{GS} is argument and channel length L is parameter. It is obtained

through multiplication of the results of simulation of unity-gain frequency f_u and intrinsic gain A_u for different values of channel length L and gate-source voltage U_{GS}. As long as the channel length L is larger, the gain-to-unity-gain frequency product $A_u \cdot f_u$ is smaller.

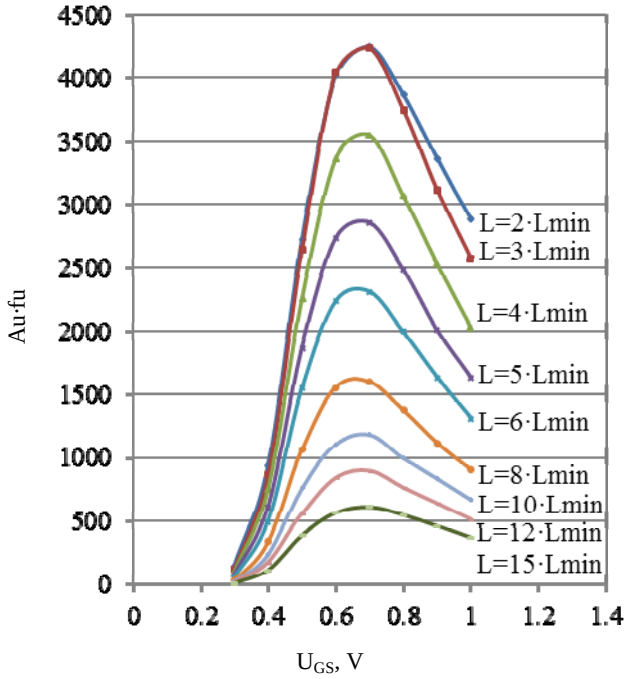

Fig. 8. Gain-to-unity-gain frequency product $A_u \cdot f_u$ vs. L and U_{GS}.

Fig. 9 gives another 3-D view of the gain-to-unity-gain frequency product $A_u \cdot f_u$, in which the channel length L and gate-source voltage are arguments together. The maximum of the product $A_u \cdot f_u$ is for L=2·Lmin and U_{GS}=0.7 V (around the border between strong inversion and velocity saturation regions). The value is up to $4200 \cdot 10^9$.

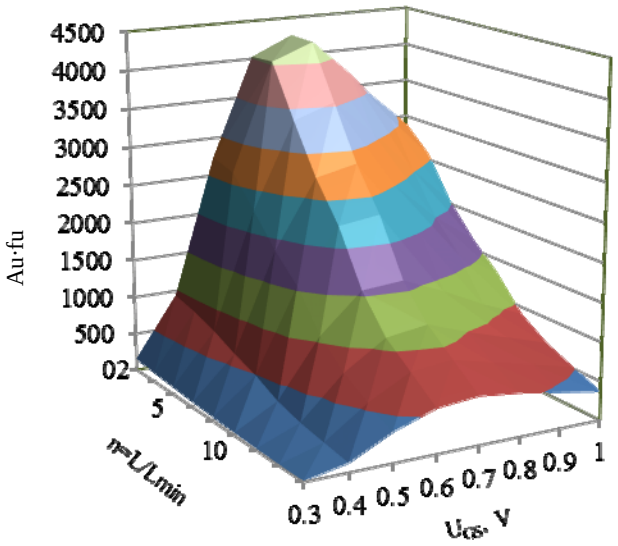

Fig. 9. 3-D view of the gain-to-unity-gain frequency product $A_u \cdot f_u$ vs. L and U_{GS}.

Using the provided graphs, designers can choose better values of the channel length and bias condition U_{GS} for every transistor in the circuit.

IV. Conclusion

The paper presents a set of simulation experiments for characterization and graphical representation of the performance of deep and ultra-deep submicron CMOS transistors in dependence of channel length L and bias conditions U_{GS}.

To this aim the key performance indicators as transconductance gm, unity-gain frequency fu, intrinsic gain Au and gain-to-unity-gain frequency product Au·fu are discussed. Test circuits for evaluation of these indicators by simulation are presented.

The proposed approach is applied to the nMOS transistor from 45nm CMOS technology. The obtained results give detailed and demonstrative illustration of the characteristics of the transistor for different values of channel length L and bias conditions U_{GS}.

The results can be used to determine the operating point and the sizes of the transistors in analog integrated circuit design.

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