

Three-Phase Soft-Switched Quasi Resonant DC Link Inverter for AC Motor Drives with Different Clamps

Dimitar Stoilov Spirov and Nikolay Georgiev Komitov

Abstract – A soft-switched inverter is derived from the passively clamped quasi-resonant link circuit with three different clamps: coupled inductor, diode clamp and coupled inductor and capacitor. The proposed soft-switching inverter is formed from the traditional pulse-width modulated (PWM) inverter by simply augmenting with auxiliary resonant circuits, and the soft switching is achieved through applying PWM switching control signals with suitable delays for the switches. Only one auxiliary switch is used to generate zero-voltage instants for the inverter switching devices. The designed soft-switching inverter is used for powering an induction motor drive to test its effectiveness. The proposed drive system is modeled and its performance is simulated in PSpice. Several results are presented to illustrate the performance of the proposed inverter topology with three different clamps.

Keywords – Induction motor drive, Soft-switching inverter, Clamp circuit.

I. INTRODUCTION

Inverters have many applications in power electronic devices. The performance of a pulse-width modulated inverter-fed system can be much improved by increasing the switching frequency. In hard switching inverters, a higher switching frequency leads to increased switching losses which consequently increases the size of the snubber circuits [1, 2]. This will suffer by giving large switching stresses of the power devices. In addition, electromagnetic interference increases and efficiency decreases. To overcome these problems, the application of soft switching techniques is essential [1-5].

The resonant DC-link inverter is the most commonly used one for induction motor drives, owing to its simplicity, but it possesses the disadvantage of having a high resonant link voltage, which is equal to or greater than twice the supply voltage [1].

Quasi-resonant (QR) inverters offer several advantages compared with resonant DC-link inverters with regard to resonant link design and control, device rating requirements and use of pulse width modulation (PWM) [6]. The QR inverter schemes generate zero-voltage instants in the DC link at controllable instants that can be synchronised with any PWM transition command, thus

Dimitar Spirov is with the Department of Electrical Engineering, University of Food Technologies - Plovdiv, 26, Maritza Blvd., 4002 Plovdiv, Bulgaria, e-mail: dimitar_spirov@abv.bg

Nikolai Komitov is with the Department of Electrical Engineering, University of Food Technologies - Plovdiv, 26, Maritza Blvd., 4002 Plovdiv, Bulgaria, e-mail: nikkomitov@abv.bg

ensuring a zero-voltage switching condition of inverter devices. As a result, these inverters can be operated at high switching frequencies with high efficiency [6].

The passively clamped QR inverter is reported in [7]. This topology satisfying most of the essential requirements, such as low clamp factor, simple resonance control, guaranteed zero-link voltage condition, PWM capability, use of only one auxiliary switch and recycling of resonant energy. The only drawback of this scheme was the high reverse voltage requirement of the clamp diode. This problem can be solved by use of a separate, low-voltage DC source [5, 6]. Another possible solution could be to use a simple R-C parallel circuit to maintain low voltage [6].

One of the main QR inverter research goals is to achieve soft switching conditions with a minimum number of auxiliary circuit elements [2]. Reducing the number of auxiliary switches simplifies the control circuit and decreases the inverter cost.

The object of this work is to develop and simulated in PSpice a three-phase induction motor drive fed by a PWM voltage source soft-switching inverter – the passively clamped quasi-resonant link inverter with three different clamps. It is necessary to investigate a performance of proposed drive system for the dynamic and steady-state modes.

II. SIMULATION MODEL

One of the passively clamped quasi-resonant dc link inverter topology falling into this category is inverter with coupled inductive feedback (Fig. 1) [5].

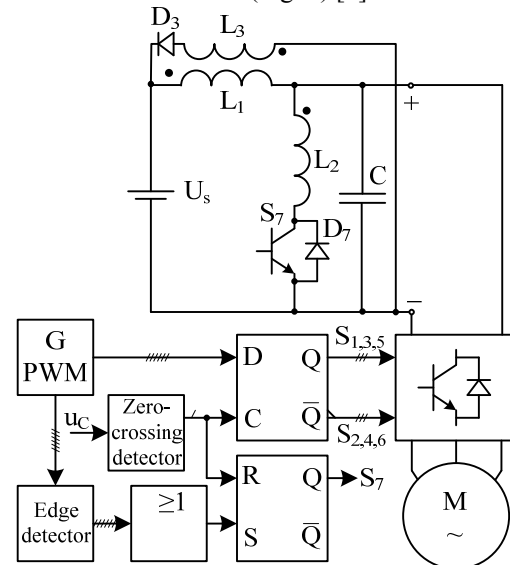


Fig. 1. Passively clamped quasi-resonant dc link inverter with coupled inductor

Through the introduction of magnetic coupling between three resonant inductors (L_1 , L_2 and L_3), the zero-voltage instants for the inverter can be generated by one auxiliary switch S_7 and antiparallel diode D_7 . The dc-link resonant capacitor is C . The main inverter is composed of S_1 to S_6 .

The circuit operates by setting up a resonating dc link that periodically returns the dc bus voltage to zero. During the interval that the diodes in antiparallel with the main inverter devices are conducting, all inverter devices may be turned off, if desired, with minimal turn-off losses. At the same time, all incoming devices may be turned on with zero turn-on losses.

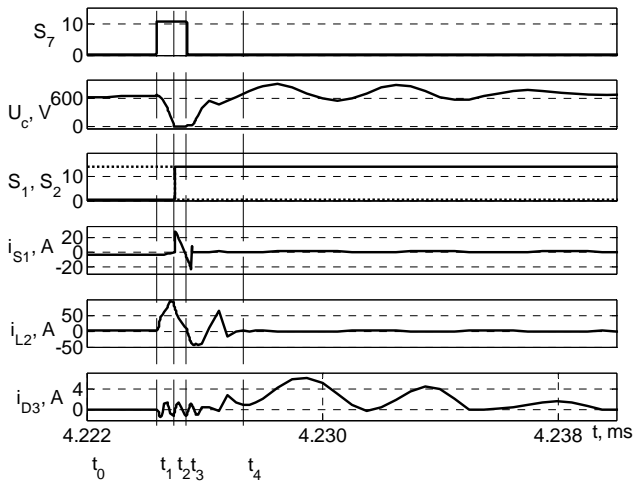


Fig. 2. Resonant link waveforms for the inverter with coupled inductor

Initially, the auxiliary switch S_7 is off and the auxiliary circuit is disconnected from the inverter main power circuit. This regime corresponds to the pseudo steady state conditions with link voltage equal to $U_s - (t_0 \div t_1$ in Fig. 2). Whenever a change in the state of the inverter main switches is desired, S_7 is turned on (t_1). The resonance between inductor L_1 and capacitor C drives the capacitor voltage up toward $2U_s$ until it is clamped at KU_s [5]. Since the clamp factor is less than 2, the resonance between L_1 and C will limit the capacitor voltage U_c between $(2-K)U_s$ and KU_s [5]. With S_7 on, the resonance between L_1 , L_2 and C causes the capacitor to discharge and pulls down the link voltage toward a negative value (t_2). When capacitor voltage reaches zero, the antiparallel diodes in the inverter legs conduct and the link voltage is clamped at zero-voltage conduction [5]. The inverter poles can then perform the commanded switching at zero-voltage conduction. In the mean time, the magnetic coupling between inductors L_1 and L_2 cause the current in the antiparallel diodes to decrease (Fig. 2). Once the current in the antiparallel diodes becomes zero, the zero-voltage conduction is removed, and the link resonance between L_1 , L_2 and C regains control and automatically charges up the capacitor voltage [5]. Inductor current i_{L2} will reverse its direction and diode D_7 becomes conducting (t_3). The switch S_7 is then turned off in a zero-voltage switching manner. When current i_{L2} decreases to zero, the diode D_7 turns off. The auxiliary circuit is automatically disconnected from the main power circuit. The resonance between L_1 and C keeps driving the link voltage up to the clamp voltage KU_s [5]. Clamp period starts to feedback excessive resonant energy

to the dc source through the clamp diode D_3 . After this interval, the link returns to the pseudo steady state and the cycle repeats for the next switching command.

The problem with the high reverse voltage requirement of the clamp diode can be solved by use of a separate, low-voltage DC source. The clamp circuit can be simplified as shown in Fig. 3 [5, 6].

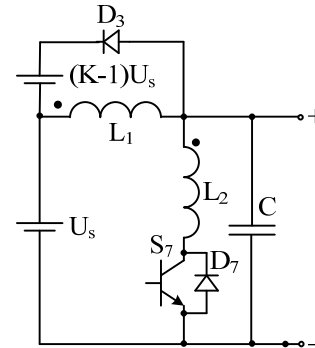


Fig. 3. Passively clamped quasi-resonant dc link inverter with diode clamp

The secondary of the passive clamp transformer is replaced by a low voltage dc source with a voltage equal to $(K-1)U_s$ and clamp diode. The resonant link waveforms are shown in Fig. 4.

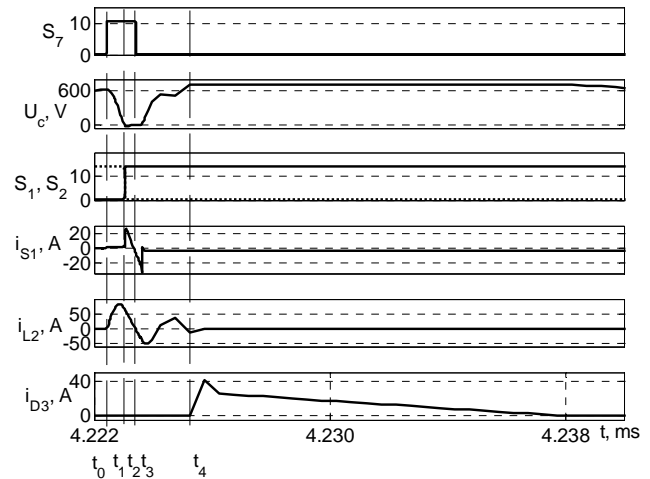


Fig. 4. Resonant link waveforms for the inverter with diode clamp

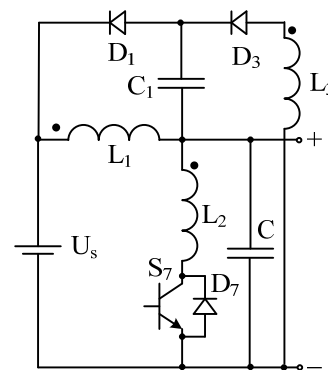


Fig. 5. Passively clamped quasi-resonant dc link inverter with coupled inductor and capacitor

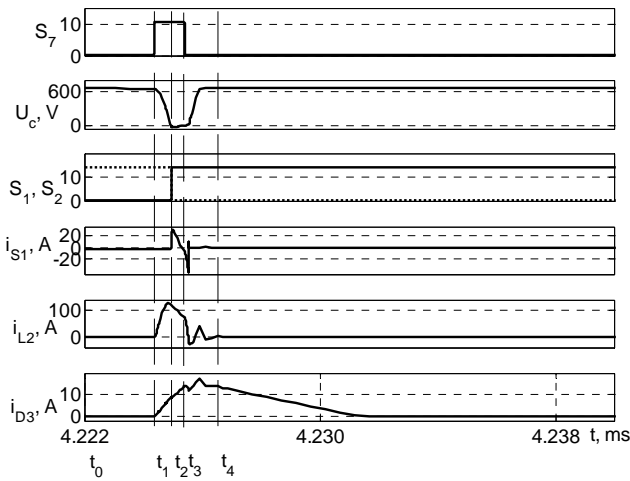


Fig. 6. Resonant link waveforms for the inverter with coupled inductor and capacitor

A soft-switched topology in which three mutually coupled inductors at a time are involved in the resonance process is proposed in Fig. 5 [6]. Clamping is provided by a large filter capacitor C_f , which acts as a low-voltage dc source whose average current in steady state is zero [6]. The entire resonant energy associated with the clamping circuit is recycled. The voltage U_f across C_f attains a value equal to $(K-1)U_s$ and lies in the range of 1.1–1.3. This dc voltage across C_f is analogous to a separate low voltage dc source. Operation of this inverter can be explained by reference to Fig. 6.

III. RECEIVED RESULTS

Simulation is done on a three phase induction motor fed by a PWM inverter developed in PSpice. The basic circuit of the proposed scheme consists of a three phase induction motor type AO-90S-4 having ratings as 1,kW, 380V, 50 Hz which is connected to drive the constant nominal load. The PSpice model of three phase induction motor inverter drive has been developed in [7]. The technical data of the electric motor are given in Appendix.

The design of the proposed inverter involves the selection of parameters C , L_1 , L_2 , L_3 to satisfy the desired link waveform specifications such as du/dt , di/dt and peak currents [6]. The design expressions are derived from the differential equations of each mode of the resonant cycle [1-7]. A set of parameters has been chosen as $L_1=30\mu\text{H}$, $L_2=10\mu\text{H}$, $L_3=1000\mu\text{H}$, $C=80\text{nF}$. The magnetic coupling between L_1 , L_2 , L_3 is designed as 0.9.

A three-phase sine-triangle PWM command generator (GPWM) was implemented to control the six inverter switches (Fig. 1). The frequency of the carrier wave is maintained at 2 kHz.

Inverter control is implemented based on the link operation requirements, whenever a switching signal is generate, the auxiliary circuit must first be turned on to initiate a resonant transient. The inverter switches, when the link voltage reaches zero. A block diagram for a control scheme is shown in Fig. 1. The edge detector locates the desired state change before the switching command is passed to the inverter switches. The detected edges are used as an input of a RS-flip flop to turn on of the auxiliary

circuit. When the link voltage reaches zero, the zero-voltage detector outputs a signal used as an input of a RS-flip flop to turn off of the auxiliary switch.

To synchronize the change in the conducting state of the inverter devices with the zero link voltage instant, D-type flip-flop is used. The switching signals generated by GPWM drive the D-input pins of the flip-flop, and the output pins drive the corresponding top (S_1 , S_3 , S_5) and bottom (S_2 , S_4 , S_6) switches of the PWM inverter. When the link voltage reaches zero, the zero-voltage detector outputs a signal that is used to clock the D-type flip-flop. Thus the conducting state is changed only at zero-voltage condition.

From the basic waveforms shown, it is seen that some limitations still exist. The control circuit must drive the auxiliary switch at the proper time. It can be observed, that the state of the inverter switches can be changed Δt_s after turning S_7 on. The fall time for the link voltage is Δt_f . The zero link voltage condition maintained for Δt_z . The rise time for the link voltage is Δt_r . The delay values for the three different clamps were summarized in Table 1.

TABLE 1. THE DELAY VALUES FOR THE THREE DIFFERENT CLAMPS

Parameter	Clamping circuit		
	Coupled inductor	Diode clamp	Coupled inductor and capacitor
$\Delta t_s, ns$	586.4	590.8	572.4
$\Delta t_f, ns$	558.9	522.6	528.7
$\Delta t_z, ns$	617.9	615.4	634.2
$\Delta t_r, \mu s$	3.27	2.07	0.48

From Table 1 it can be seen that the rise time of the link voltage for the third clamping circuit is 0.48, i.e. about 5 times less than the rise time of the other two schemes.

Amplitude value of the capacitor voltage $U_{c,max}$, diode D_7 voltage $U_{D7,max}$, current through the transistor S_1 ($i_{S1,max}$), current through the inductance L_2 ($i_{L1,max}$) and current through the diode D_3 ($i_{D3,max}$) respectably with coupled inductor, diode clamp and coupled inductor and capacitor are summarized in Table 2.

TABLE 2. AMPLITUDE VALUES FOR THE THREE DIFFERENT CLAMPS

Parameter	Clamping circuit		
	Coupled inductor	Diode clamp	Coupled inductor and capacitor
$U_{c,max}, V$	878,6	705,9	668,2
$U_{D7,max}, V$	974,1	949,6	1325,5
$i_{S1,max}, A$	29,9	29,4	31,9
$i_{L2,max}, A$	92,0	83,4	131,3
$i_{D3,max}, A$	4,8	24,3	17,1

From Table 2 it can be seen that the clamping circuit with coupled inductor and capacitor has an amplitude value of the capacitor voltage 668,2V, i.e. clamp factor is 1.04, while for the coupled inductor and the diode clamp is 1.37 and 1.1 respectably. Amplitude value of the diode D_7 voltage is $(1.48 \div 2.07)U_s$.

Fig. 7 shows the shapes of the current, voltage and power losses in the switches of the test circuit with coupled inductor and capacitor.

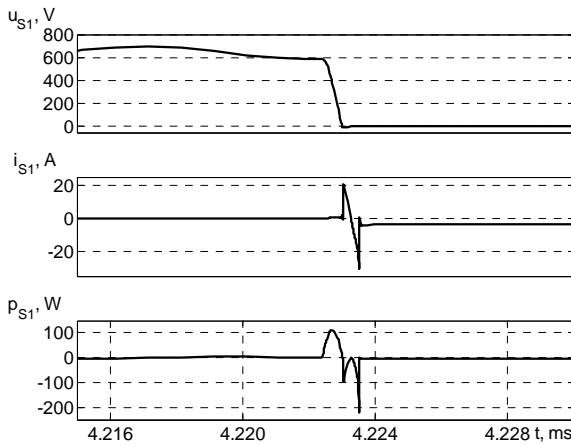


Fig. 7. Dependences $u_{S1}, i_{S1}, p_{S1}=f(t)$

Fig. 8 shows the link voltage u_{DC} , inverter line-line voltage u_{AB} and phase current i_B for the passively clamped quasi-resonant dc link inverter with coupled inductor and capacitor.

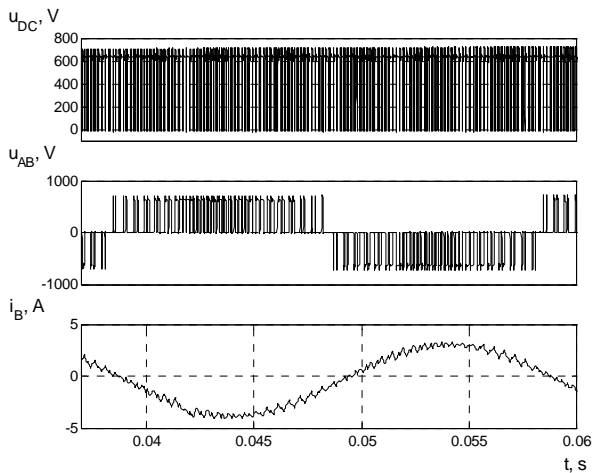


Fig. 8. Dependences $u_{DC}, u_{AB}, i_B=f(t)$

It is seen that there is some distortion in the motor current. The value of the THD for phase current and power losses average value in the switches of the test circuit for the three different clamps were summarized in Table 3.

TABLE 3. THE THD FOR PHASE CURRENT FOR THE THREE DIFFERENT CLAMPS

Parameter	Clamping circuit		
	Coupled inductor	Diode clamp	Coupled inductor and capacitor
THD, %	8.59	7.59	8.63
P_{S1}, W	24.78	20.94	20.95

From Table 3 is seen that the current through transistor S_1 begins to flow in the reset voltage on it. This led to a significant reduction in switching losses - in the case of coupled inductor and capacitor of 20.95 W.

The value of the THD for phase current i_B is 8.59% for the coupled inductor and it is 7.59% and 8.63% for the

diode clamp and coupled inductor and capacitor respectively.

IV. CONCLUSION

A three-phase induction motor drive fed by a PWM voltage source soft-switching QR inverter is presented. A soft-switched inverter is derived from the passively clamped quasi-resonant link circuit with three different clamps: coupled inductor, diode clamp and coupled inductor and capacitor.

The proposed drive system is modeled and its performance is simulated in PSpice. From the basic waveforms, it is seen that some limitations still exist. The operation principles and link resonance control for the three different clamps are investigated. Link waveforms and operation modes are analyzed to reveal various soft switching characteristics.

REFERENCES

- [1] K. H. Chao, C. M. Liaw. *Three-phase soft-switching inverter for induction motor drives*, IEE Proc-Electr. Power Appl, vol 148, no. 1, pp. 8-20, 2001.
- [2] M. R. Amini, H. Farzanehfar. *Quasi Resonant DC Link Inverter with a Simple Auxiliary Circuit*, Journal of Power Electronics, vol. 11, no. 1, pp. 10-15, 2011.
- [3] W. Yi, H. L. Liu, Y. C. Jung, J. G. Cho, and G. H. Cho. *Program-Controlled Soft Switching PRDCL Inverter with New Space Vector PWM Algorithm*, IEEE, pp. 313-319, 1992.
- [4] S. Chen, B. J. C. Filho and T. Lipo. *Design and Implementation of a Passively Clamped Quasi Resonant DC Link Inverter*, IEEE, pp. 2387-2392, 1995.
- [5] S. Chen and T. Lipo. *A Novel Soft-Switched PWM Inverter for AC Motor Drives*, IEEE Trans. On Power Electr, vol. 11, no. 4, pp. 653-659, 1996.
- [6] J. Shukla and B.G. Fernandes. *Three-phase soft-switched PWM inverter for motor drive application*, IET Electr. Power Appl., vol. 1, no. 1, pp. 93-104, 2007.
- [7] D. Spirov, N. Komitov and N. Bozukov. *PSpice Modeling of Inverter Induction Machine Drive*, TECHSYS'13, pp. 73-76, 2013.

APPENDIX

Induction motor type AO-90S-4
 $P_N=1,1kW; U_N=380V; I_N=2,8A; f=50Hz; p_p=2;$
 $n_N=1410min^{-1}; M_N=7,45Nm; \cos\varphi=0,8; J_m=0,001kgm^2.$
 Parameters for $s=s_N$
 $R_s=7.45\Omega; R_r=5\Omega; L_{\sigma s}=0.01839H; L_{\sigma r}=0.01839H;$
 $L_m=0.33475H.$