Stability Investigation using SPICE of BUCK DC-DC Converter

Georgi Tzvetanov Kunov, Elissaveta Dimitrova Gadjeva, Maria Petkova Petkova and Tihomir Sachev Brusev

Abstract – **A stability investigation of the BUCK DC-DC converter with Average Current Mode Control is considered in the present paper. A *Spice* stability investigation equivalent circuit is composed. Using parametric analysis, zeros and poles of the current regulator transfer function are investigated. The optimal values of the compensation network elements for the current regulator are obtained. The stability of the converter operation is validated by *Nyquist* plot and transient analysis.**

Keywords – **Power Electronics, BUCK DC-DC Converters, Average Current Mode Control, Stability, Spice Simulation**

I. Introduction

The basic methods of control used in the BUCK DC-DC converters are voltage mode control (VMC), peak current mode control (CMC) and average current mode control (ACMC). Their advantages and disadvantages are systematically summarized in [1,2,3]:

Voltage Mode Control:

The advantages are: stable modulation – less sensitive to noise, single feedback path, it can work over a wide range of duty cycles. The disadvantages are: loop gain proportional to V_{in}, LC double pole often drives type PID compensation, continuous current mode (CCM) and discontinuous current mode (DCM) differences – a compensation challenge, slow response to input voltage changes, current limiting must be done separately.

Current Mode Control:

The advantages are: power plant gain offers a single-pole roll-off, line rejection, cycle-by-cycle current limiting protection, current sharing. The disadvantages are: noise, minimum on-time, current probe (Rsense, current transformers).

Peak versus Average Current Mode Control:

The disadvantages of Peak CMC are: poor noise immunity (at switching on), slope compensation required when $D > 0.5$, peak to average current error, topology problem when inductor current is other than output current. The advantages of ACMC are: average current tracks well the current program in CCM or DCM, noise immunity is excellent even at low set point, ACMC is working whatever the topology, slope compensation is not required but loop gain at F_{sw} is limited to achieve stability.

In the present paper the stability of work of BUCK DC-DC converter with Average Current Mode Control is investigated. It is performed using the program *Cadence PSpice*. The simplified circuit of the converter is shown in Fig. 1.

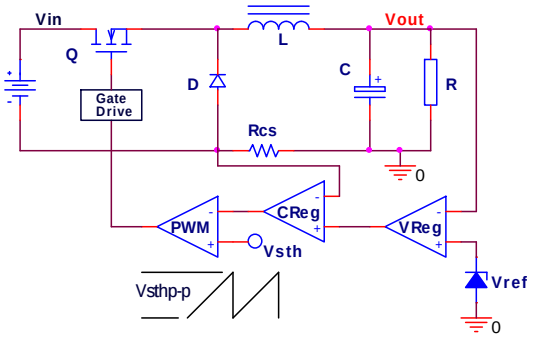


Fig.1. Simplified circuit of BUCK DC-DC with ACMC

In the classical theory of automated control, a closed loop system is represented by its mathematical description [4]. This approach, applied to BUCK DC-DC converter with ACMC, is illustrated in Fig. 2.

The designations for the separate blocks are: W_{Mod} – transfer function of the BUCK DC-DC converter, W_{LCR} – transfer function of the output filter, W_{CR} – transfer function of the current regulator (a PI regulator is used), W_{VR} – transfer function of the voltage regulator (a PID regulator is used). Applying the rules for the equivalent transformations, (Fig.2a, Fig.2b and Fig.2c), the system is reduced to a single block with equivalent transfer function *We*.

The mathematical description of the transfer functions of the separate blocks is shown as follows [5,6]:

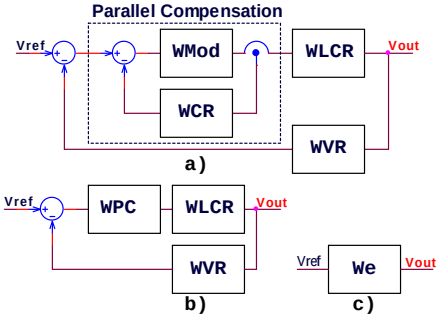


Fig.2. Equivalent transformations of the system

G. Kunov is with the Department of Power Electronics, Faculty of Electronic Engineering and Technologies, Technical University of Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: gkunov@tu-sofia.bg

E. Gadjeva is with the Department of Electronics and Electronics Technologies, Faculty of Electronic Engineering and Technologies, Technical University of Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: egadjeva@tu-sofia.bg

M. Petkova is with the Department of Power Electronics, Faculty of Electronic Engineering and Technologies, Technical University of Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: mariya_petkova@tu-sofia.bg

T. Brusev is with the Department of Technology and Management of Communication Systems, Technical University of Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: brusev@ecad.tu-sofia.bg

The transfer function of the Modulator:

$$W_{Mod}(s)=\frac{V_{in}}{V_{sthp-p}} \quad (1)$$

The transfer function of the output filter:

$$W_{LCR}=\frac{1+sR_C C}{1+s\left(R_L+R_C\right)C+s^2LC} \quad (2)$$

where:
R_L – direct-current resistance (DCR) of the filter inductor, R_C – electrical series resistance (ESR) of the filter capacitor.

The transfer function of the PI current regulator:

$$W_{CR}(s)=\frac{1}{R_{C1}.C_{C1}}\cdot\frac{s+\frac{1}{R_{C2}.C_{C2}}}{s.\left(s+\frac{C_{C1}+C_{C2}}{R_{C2}.C_{C1}.C_{C2}}\right)} \quad (3)$$

The transfer function of the PID voltage regulator:

$$W_{VR}(s)=\frac{R_{V1}+R_{V3}}{R_{V1}R_{V3}C_{V1}}\frac{\left(s+\frac{1}{R_{V2}C_{V2}}\right)\left(s+\frac{1}{(R_{V1}+R_{V3})C_{V3}}\right)}{s\left(s+\frac{C_{V1}+C_{V2}}{R_{V2}C_{V1}C_{V2}}\right)\left(s+\frac{1}{R_{V3}C_{V3}}\right)} \quad (4)$$

The transfer function of the Parallel Compensation:

$$W_{PC}(s)=\frac{W_{Mod}(s)}{1+W_{Mod}(s).W_{CR}(s)} \quad (5)$$

The equivalent transfer function:

$$W_e(s)=\frac{W_{Mod}(s)W_{LCR}(s)}{1+W_{PC}(s)W_{LCR}(s)W_{VR}(s)}=$$

$$=\frac{W_{Mod}(s)W_{LCR}(s)}{1+sW_{Mod}(s)+W_{Mod}(s)W_{LCR}(s)W_{VR}(s)} \quad (6)$$

In [7], the mathematical description of the transfer functions of the output filter and the regulators is replaced by their real circuits. This approach, combined with the SPICE simulation, simplifies the stability investigation of the system. It is applied in the present paper.

II. Stability Investigation of BUCK DC-DC Converter

A. Calculation of the LC filter parameters

In order to perform stability investigation of the BUCK DC-DC regulator system, it is necessary to have the parameters of the mode in which it will work. The mode of operation includes the following parameters [6]:

- switching frequency: F_{sw}=250 kHz;
- input voltage: V_{in}=15V;
- output voltage: V_{out} = 5V;
- maximum output current: $I_{Load\text{-}max}$ = 5A;
- inductor current ripple: ΔI_L=0.5A;
- output voltage ripple: ΔV_{out} = 0.25V;
- maximum change in load current: $\Delta I_{Load\text{-}max}$=4A.

First, the smoothing filter is designed by the following equations[6]:

$$L\geq\frac{V_{in}-V_{out}}{\Delta I_L}.\frac{V_{out}}{V_{in}}.\frac{1}{F_{sw}}=26.6\ \mu H \quad (7)$$

We choose L=33μH.

$$C\geq\frac{L\Delta I^2_{Load-max}}{2.V_{out}\Delta V_{out}}=267\mu F$$

We choose C=330 μF with ESR=25 mΩ.

The calculated L and C values define the cutoff frequency:

$$F_{LC}=\frac{1}{2\pi\sqrt{LC}}=1.5\text{kHz}$$

and ESR zero frequency:

$$F_{ESR}=\frac{1}{2\pi C.ESR}=19.3\text{kHz}$$

B. Compensator calculation of the PI current regulator

A *PI* type compensator as a current regulator is shown in Fig. 3a. The location of its zero crossover frequencies is shown in Fig. 3b. The recommended values are [6]:

F_{ZI}=0.75×F_{LC}=1.125 kHz and F_{P2}=0.5×F_{sw}=125 kHz.

The desired bandwidth of the system (F_0=25 kHz) is chosen bigger than F_{ESR}.

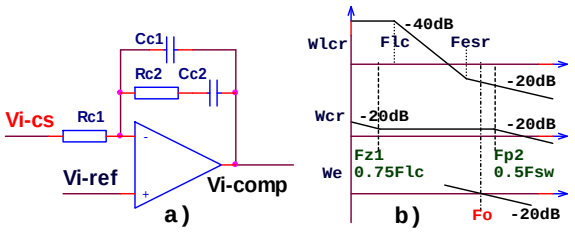


Fig.3. PI type compensator as a current regulator

The recommended parameter value [6] of the resistor R_{C1} is between 1 kΩ and 5 kΩ. It is chosen R_{C1}=3.9 kΩ.

The parameter value of the resistor R_{C2} is calculated by the equation:

$$R_{C2}=\frac{F_{ESR}F_0}{(F_{LC})^2}\cdot\frac{V_{sthp-p}}{V_{in}}R_{C1}=278\text{k}\Omega \quad (8)$$

We choose R_{C2}=270 kΩ.

The relationship between the parameter values of the passive components of the regulator and the poles of the compensator is given by equations [6]:

$$F_{z1}=\frac{1}{2\pi R_{C2}C_{C2}} \quad (9)$$

$$F_{P2} = \frac{1}{2\pi R_{C2} C_{C1}} \tag{10}$$

By the above equations standard values are calculated and chosen: C_{C2}=4.7 pF and C_{C1}=680 pF.

C. Compensator calculation of the PID voltage regulator

A PID type compensator as voltage regulator is shown in Fig. 4a. The location of its zero crossover frequencies is shown in Fig. 4b. The recommended values are [6]:

F_{Z1}=0.75×F_{LC}=1.125 kHz; F_{Z2}=F_{LC}=1.5 kHz;
F_{P2}=F_{ESR}=19.3 kHz and F_{P3}=0.5×F_{sw}=125 kHz.

The desired bandwidth of the system (F_0=15 kHz) is chosen less than F_{ESR}.

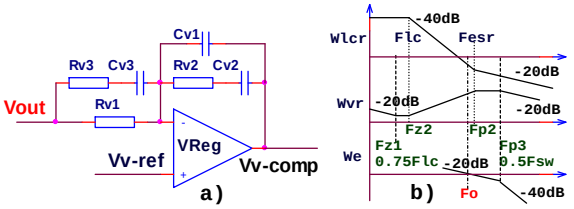


Fig.4. PID type compensator as a voltage regulator

The recommended parameter value of the resistor R_{V1} is between 1 kΩ and 5 kΩ. We choose R_{V1}=3.9 kΩ.

The parameter value of the resistor R_{V2} is calculated by the equation:

$$R_{V2} = \frac{F_0}{F_{LC}} \cdot \frac{V_{sthp-p}}{V_{in}} R_{V1} = 13\text{k}\Omega \tag{11}$$

We choose R_{V2}=13 kΩ.

The relationship between the parameter values of the passive components of the regulator and the poles of the compensator is given by equations:

$$F_{Z1} = \frac{1}{2\pi R_{V1} C_{V1}} \tag{12}$$

$$F_{Z2} = \frac{1}{2\pi C_{V3}\left(R_{V1} + R_{V3}\right)} \tag{13}$$

$$F_{P2} = \frac{1}{2\pi C_{V3} R_{V3}} \tag{14}$$

$$F_{P3} = \frac{1}{2\pi R_{V1} C_{V2}} . \tag{15}$$

By the equations (11) to (15) standard value are calculated and chosen for C_{V1}=100 pF; C_{V2}=10 nF; C_{V3}=27 nF; R_{V3}=47 Ω.

D. Stability investigation equivalent circuit

The equivalent circuit for stability investigation is shown in Fig. 5. The *Nyquist* plot is shown in Fig. 6a with calculated parameters in correspondence with the conditions in Chapter *II.A* and *II.B*. It is seen that the system is unstable (Fig. 6a). Using *Parametric Analysis* (Fig. 5), the values of the frequency F_{Z1} and F_{P2} are obtained, which ensure the system stability.

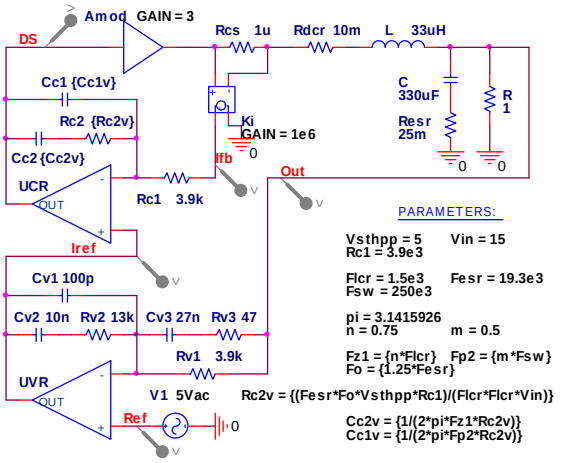
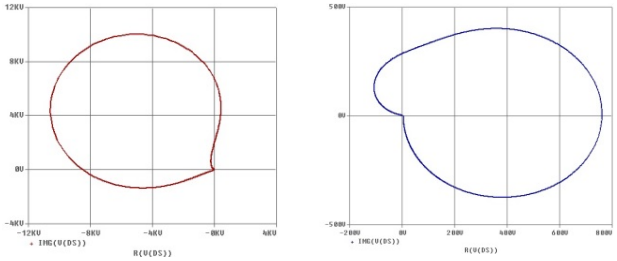


Fig. 5. Equivalent circuit for stability investigation

A recalculation of the capacitor values C_{C2} and C_{C1} is performed in the compensation network of the PI regulator and standard values are chosen: (C_{C2} = 390 nF and C_{C1} = 2.7 nF). It is seen from the *Nyquist* plot in Fig. 6b that the system is stable.



a) F_{Z1}=0.75F_{LC}; F_{P1}=0.5F_{SW} b) F_{Z1}=0.001F_{LC}; F_{P1}=0.001F_{SW}

Fig.6. *Nyquist* plot of the system

E. Magnitude vs. frequency responses of the basic blocks of the converter

The Magnitude-vs. frequency responses of the building blocks of the BUCK DC-DC converter with Average Current Mode Control are obtained using the simulation circuit shown in Fig. 7.

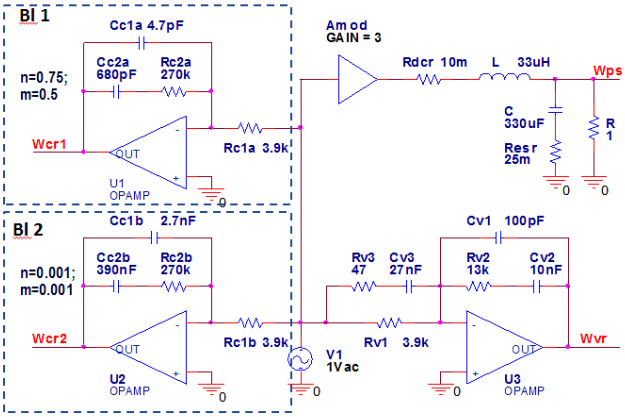


Fig.7. Simulation circuit for obtaining the magnitude-vs. frequency responses of the building blocks

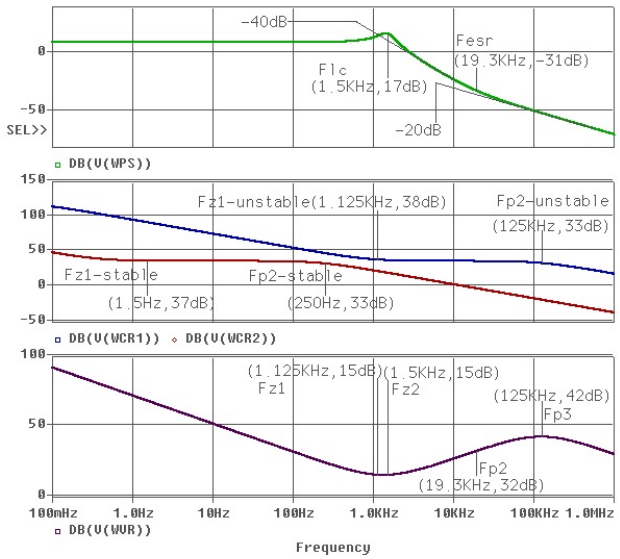


Fig.8. Simulation results for the magnitude-vs. frequency responses

The circuit of the PI regulator, corresponding to unstable mode of operation, is simulated by $Bl_1(n = 0.75$ and $m = 0.5)$.

The circuit of the PI regulator, corresponding to stable mode of operation, is simulated by $Bl_2(n = 0.001$ and $m = 0.001)$.

The simulation results are shown in Fig. 8. It is seen that a stable mode of operation is achieved, placing the zero and the pole of the PI regulator (F_{Z1} and F_{P2}) in the low frequency range.

III. Transient Stability Investigation of BUCK DC-DC Converter

The full electrical circuit of the BUCK DC-DC converter with Average Current Mode Control is shown in Fig. 9, using the obtained parameter values of the PI regulator, which ensure a stable mode of operation.

The simulation results in the time domain are shown in Fig. 10. The circuit is simulated for two stepping variations of the load current (from 1.5A to 5A and from 5A to 1.5A). The simulation results for the transient responses confirm the system stability.

IV. Conclusion

Stability of the BUCK DC-DC converter with Average Current Mode Control has been investigated. The optimal values of the compensation network elements for the current regulator are obtained corresponding to a stable system. A parametric analysis in the frequency domain using *Cadence PSpice* simulator is applied for this purpose. Stability investigation is performed using frequency criterion (*Nyquist* plot), as well as using simulation in the time domain. The obtained simulation results confirm the validity of the proposed procedure for optimal value determination of the compensation network elements for the current regulator.

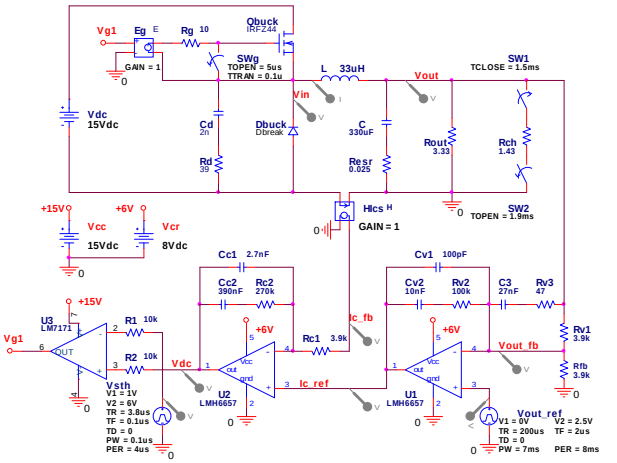


Fig. 9. The full electrical circuit of the BUCK DC-DC converter with Average CMC, corresponding to a stable mode of operation

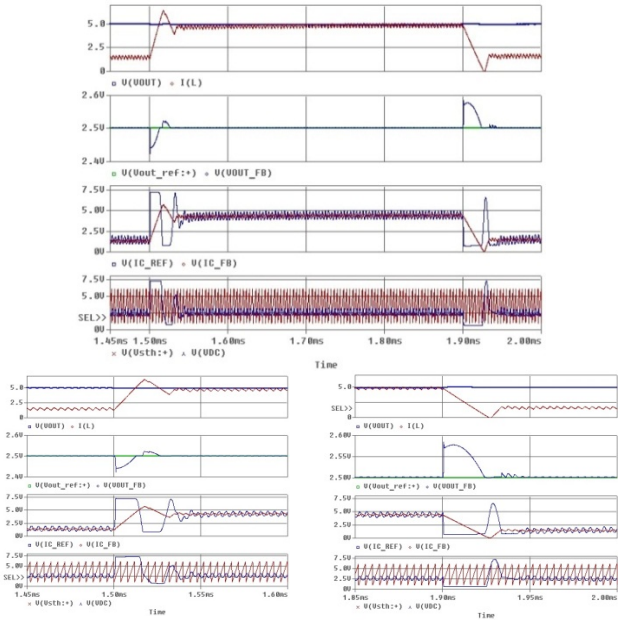


Fig.10. Simulation results in the time domain

References

[1] http://www.montefiore.ulg.ac.be/~geuzaine/ELEC0055/

[2] P.Cooke. *Modeling average current control*, Proc. APEC, New Orleans, 2000, Vol.1, pp. 256-262

[3] L. Dixon. *Average Current Mode Control of Switching Power Supplies*, www.ti.com/lit/an/slua079/slua079.pdf

[4] K. Ishtev. *Theory of automatic control*, Technical University of Sofia, 2007.
www.ti.com/lit/an/slva274a/slva274a.pdf

[5] D. Mattingly. *Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators*, Intersil, Technical Brief, December 2003, TD 417.1
www.intersil.com/data/tb/tb417.pdf

[6] A. M. Rahimi, P. Parto, P. Asadi. *Compensator Design Procedure for Buck Converter with Voltage-Mode Error-Amplifier, International Rectifier*, Application Note AN-1162
www.irf.com/technical-info/.../an-1162.pdf

[7] R. Sheehan, *Understanding and Applying Current Mode Theory*, Power Electronics Technology Exhibition and Conference, October 30 – November 1, 2007, Dallas
http://www.ti.com/lit/an/snva555/snva555.pdf