Multifunctional Analyzer for Audio Signals Based on Xilinx FPGA

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Abstract – **The subject of the article is an application of programmable logic devices from the FPGA XILINX family in the building of multifunctional signal analyzing structures. The synthesized structural diagram includes programmable input attenuator, input stages, analog to digital converters, SPI interface unit, CPU core, 64 cells by 12 bit RAM and ROM memories and LCD display. The RMS calculation and Fourier analysis are performed by the soft CPU core implemented in the FPGA. Software algorithms for discrete Fourier analysis are developed which minimizes the usage of FPGA resources.**

Keywords – **Multifunctional Analyzer, Audio Signals, FPGA, RMS measurement, Distortion Measurement, Discrete Fourier Transform**

I. INTRODUCTION

The multifunctional analyzer for audio signals is a digital electronic device accomplishing different time and frequency domain and amplitude measurements of the audio signals [1]. Some of them are:
– Root Mean Square (RMS) voltage measurement;
– Amplitude measurement;
– Frequency and period measurements;
– Total Harmonic Distortion (THD) measurement.

The multifunctional analyzer is built on a Field-Programmable Gate Array (FPGA) integrated circuit of Xilinx Spartan-3E family.

The FPGA logic devices are used to implement any logical function. They have significant advantages before Application-Specific Integrated Circuits (ASIC's). The most important of them is the ability to change the configuration after the integrated circuit is manufactured [2].

A Hardware Description Language (HDL) or logical diagram is used for configuring of the FPGA.

Some dynamic parameters as slew rate and logic levels of the output signals can also be configured.

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II. STRUCTURE OF THE MULTIFUNCTIONAL ANALYZER

The structural diagram of the multifunctional analyzer for Audio signals is represented on Fig. 1. The analyzed audio signal is first fed to the input of the programmable attenuator. The right attenuation is chosen so that the signal always remains within the dynamic range of the following stages [3]. Then the signal is fed to the amplifier - limiter where it is buffered and level shifted to the half of the input dynamic range of the Analog to Digital Converter (ADC). Then the signal is fed to the input of the 12-bit ADC. The digital information from the ADC is transferred to the FPGA via SPI interface [4]. All further signal processing is carried by the microprocessor core implemented into the FPGA [5]. There are 12-bit Random Access Memory (RAM) and Read Only Memory (ROM) memories implemented into the FPGA. The data from the ADC is stored into the RAM memory during the processing. The ROM memory stores 64 pre-calculated values for one period of the sine function which are used in the process of discrete Fourier transform [3]. The results from the calculations are visualized on the LCD display.
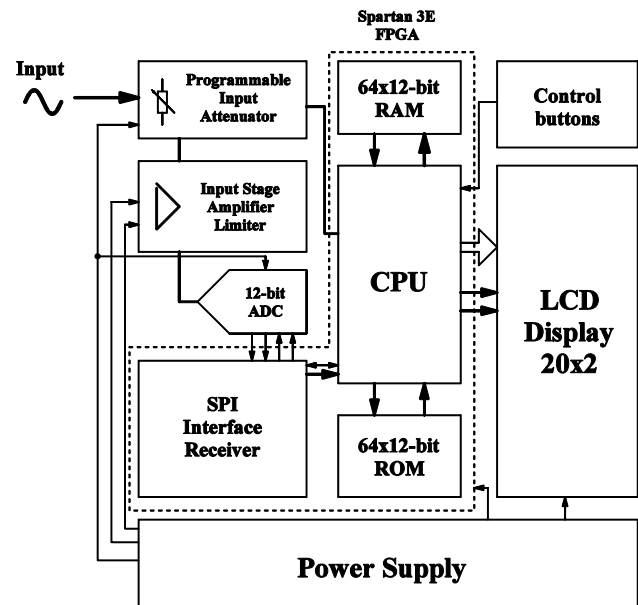

Fig. 1. Multifunctional analyzer structural diagram

III. INPUT STAGE

The circuit diagram of the input stage is represented on Fig. 2. The first stage is the input attenuator which is a resistive voltage divider. The attenuation is programmed by switching the resistance to ground by reed relays. There are three different attenuations possible: 1:1, 10:1 and 100:1. The next stage is a non-inverting voltage follower built with the Texas Instruments operational amplifier NE5534. This stage matches the relatively high output impedance of the attenuator with the lower impedance of the next stage [1]. There is a diode limiter at the input of the amplifier for overvoltage protection. The next stage is an inverting
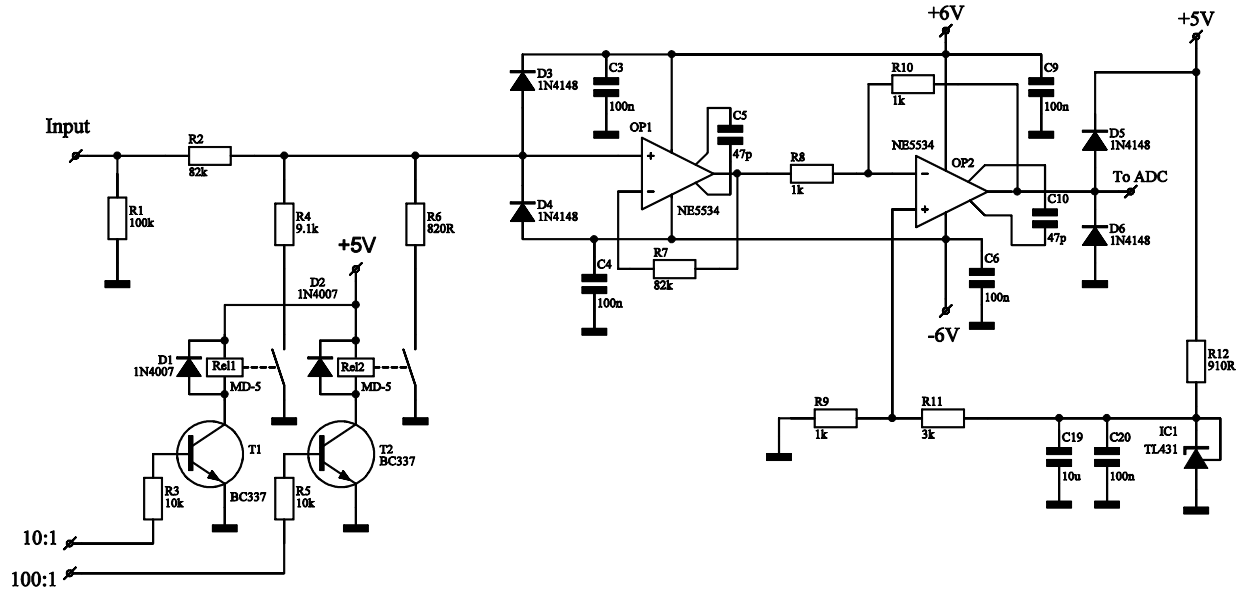
Fig. 2. Input stage schematic diagram

amplifier and level shifter. Its function is to shift the level of the signal to the half of the dynamic range of the ADC. This is needed because of the single polarity input range of the ADC. D5 and D6 are overvoltage protection for the ADC input. The bipolar power supply for the operational amplifiers is built with the AIMTEC AM1D-0512DZ DC-DC converter.

IV. DISCRETE FOURIER TRANSFORM ALGORITHM

The signal samples from the ADC are sent to the FPGA where the microprocessor is performing the software processing [5]. The most important parameter which is used in all other calculations is the period of the signal.

TABLE 1. IMPLEMENTATION OF THE MULTIFUNCTIONAL ANALYZER INTO THE FPGA

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	197	9,312	2%	
Number used as Flip Flops	181			
Number used as Latches	16			
Number of 4 input LUTs	339	9,312	3%	
Number of occupied Slices	225	4,656	4%	
Number of Slices containing only related logic	225	225	100%	
Number of Slices containing unrelated logic	0	225	0%	
Total Number of 4 input LUTs	341	9,312	3%	
Number used as logic	223			
Number used as a route-thru	2			
Number used for Dual Port RAMs	16			
Number used for 32x1 RAMs	100			
Number of bonded IOBs	33	232	14%	
Number of RAMB16s	1	20	5%	
Number of BUFGMUXs	2	24	8%	
Number of RPM macros	15			
Average Fanout of Non-Clock Nets	3.64			

There is developed a zero crossing detection algorithm [6]. When two zero crossings in the positive direction are detected, the number of samples between them gives the period of the signal. For measuring distortion, a Discrete Fourier Transform (DFT) is performed. The DFT algorithm is represented on Fig. 5. The sine and cosine components of every harmonic are calculated by multiplying the input signal with the sine or cosine function. The period of the function is the same as the period of the harmonic which is being calculated. Calculating sine and cosine functions is a slow process for a simple Central Processing Unit (CPU). For that reason a 12-bit ROM memory with 64 pre-calculated sine values for one period is implemented into the FPGA.

The multiplication of the input signal with the sine or cosine function is done sample by sample. First the CPU reads the current sample from the RAM memory and writes it into a dedicated register. Then using the number of the current sample and the number of the current harmonic component, the ROM address is calculated. If a cosine component is measured, the number 16 is added to the calculated address. Then the address value is divided by 64 and the remainder is sent to the ROM address lines. The CPU reads the ROM value and multiplies it with the current signal sample. The result from the multiplication is added to the sum register. This process is repeated for the remaining samples of the signal period. Then the content of the sum register is divided by the number of the processed samples. This gives us the relative amplitude of the sine or cosine component of the measured harmonic [7]. The relative amplitude of the measured harmonic is calculated by the equation (1).

$$A_n = \sqrt{A\,sin_n{}^2 + A\,cos_n{}^2}. \qquad (1)$$

When the relative amplitudes of the all 9 harmonics are calculated the THD value in percent is calculated by the equation (2).

$$THD.\,100 = \frac{10^4.\sqrt{\sum n(A_n)^2}}{A_1},\% \qquad (2)$$
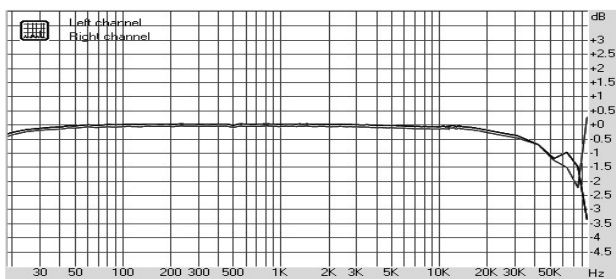

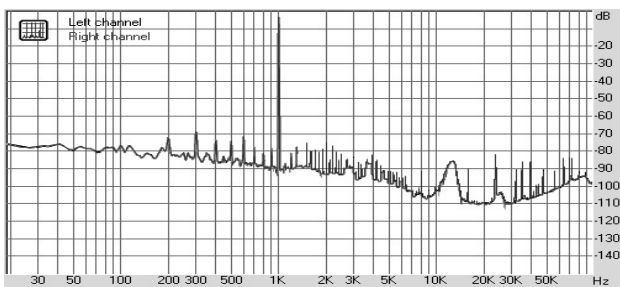Fig. 3. Input stage frequency response

Fig. 4. Input stage spectrum of the output signal with 1 kHz sine wave test signal
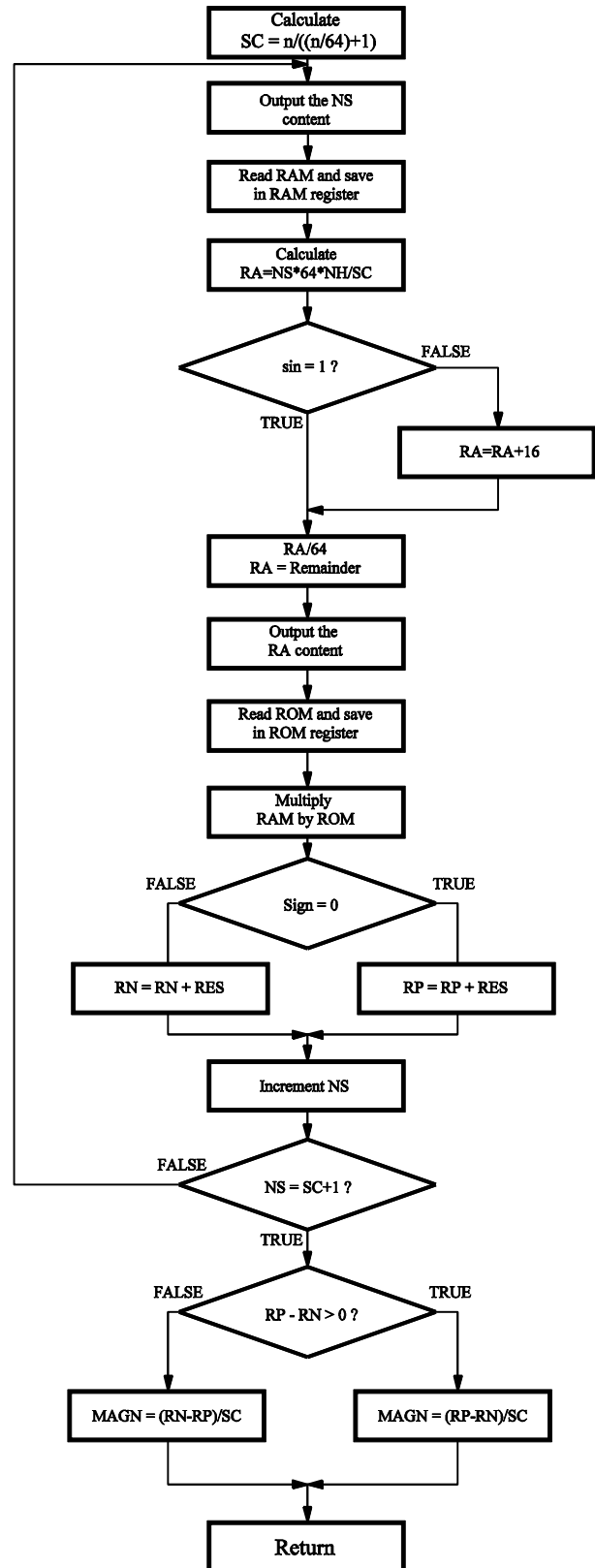

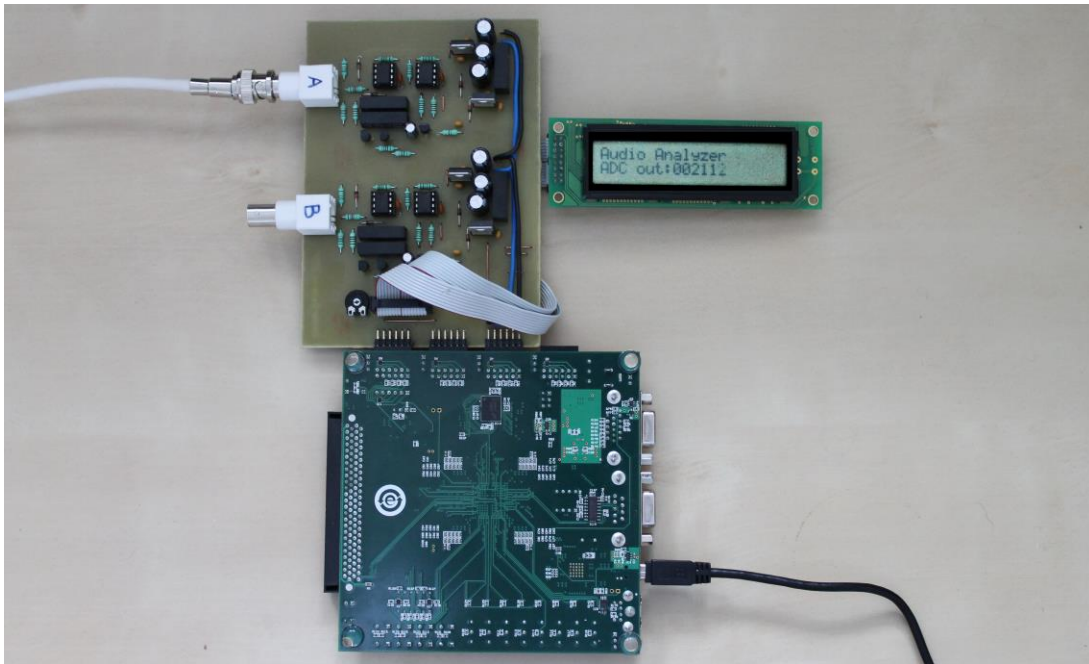Fig. 5. Algorithm of the discrete Fourier transformation subroutine

Fig. 6. Developed board with input attenuators, input stages, power supply, ADC and LCD display

V. EXPERIMENTAL RESULTS

The input stage testing is performed with PC with a 16-bit 192 kHz sampling rate sound card and installed Right Mark Audio Analyzer software. The software performs automatic measurement of various parameters of an audio system. It generates testing signals which are fed from the Line-out of the sound card to the tested circuitry. Then the signal from the output of the tested circuitry is fed back to the sound card Line-in input.

The following parameters are tested: frequency response, noise level, dynamic range, THD + noise, intermodulation distortion and crosstalk between channels.

The testing shows a frequency response from DC to 40 kHz ±0.25 dB (Fig. 3), noise level below -70 dB, THD lower than 0.04% (Fig. 4), inter modulation distortion lower than 0.2 % in the whole spectrum from 1 kHz to 50 kHz and inter-channel crosstalk about -42 dB.

VI. CONCLUSION

The results from the testing of the input stage are showing good flat frequency response which is adequate for audio signals testing.

The noise level of -70 dB is low enough to prove the concept but a good point for development is lowering the noise floor up to at least a -100 dB. This can be achieved by using resonant DC-DC converters for power supply, as well as using lower noise operational amplifiers.

The input stage is showing low enough distortion of 0.04% but this distortion is directly affecting the lowest possible measured THD. That is why it has to be improved in future developments.

The relatively high inter-channel crosstalk is due to the test setup wiring not to the input stage itself.

The results from the implementation of the analyzer into the FPGA chip are shown in Table 1. The data shows a compact structure with less than 10 percent occupation of the Spartan-3E FPGA. This proves the concept that software algorithms for Fourier transformation are more efficient with respect to the occupied resources on the chip. They can be efficiently used in non-time critical applications such as measuring THD.

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