Current Driven Automatic Electrode Impedance Balance for Ground-free Biosignal Acquisition

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Abstract – **Power-line interference (PLI) is a common disturbing factor in almost all two-electrode biosignal acquisition applications. The main cause of interference is the body to amplifier Wheatstone bridge imbalance. The bridge is formed from electrode impedances and the amplifier common mode input impedances. Because the electrode impedances vary with time, the Wheatstone bridge tends to be imbalanced and produces differential PL interference which is amplified together with the useful signal. The interference can be canceled only when the bridge is kept continuously in balanced conditions. This paper describes a powerful concept for PLI cancellation wherein by two Voltage-Controlled-Current-Sources (VCCS) enclosed in two control loops, the active and reactive components of the amplifier input impedances are synthesized and automatically adjusted to maintain balanced conditions. The main advantage of the presented approach is that the interference is canceled on a hardware level where it is generated, without influencing the spectrum of the useful signal. The method is applicable in all ground-free applications, such as Holter monitors, external defibrillators, ECG monitors and other heart beat sensing biomedical devices.**

Keywords – **Wheatstone Bridge, Lock-in Demodulator, Frequency Mixer, Power-line Interference**

I. INTRODUCTION

In ground-free biosignal amplifications (e. g. two-electrode) the common mode interference current must flow via the same electrodes used for the signal sensing. The electrode impedances Z_e and the amplifier common mode impedances Z_{cm} form a Wheatstone bridge, see *Fig. 1* [1].
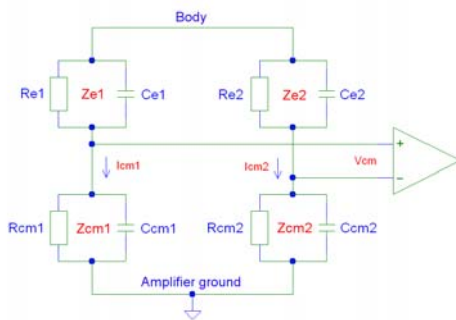

Fig. 1. Body-amplifier interface

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Only when the two shoulders Z_{e1}, Z_{cm1} and Z_{e2}, Z_{cm2} of the formed Wheatstone bridge are balanced, the Power-Line (PL) interference is not converted into a differential voltage. The Wheatstone bridge is balanced when:

$$\frac{Z_{e_1}}{Z_{cm_1}} = \frac{Z_{e_2}}{Z_{cm_2}} \tag{1}$$

The amplifier input common mode impedances Z_{cm1} and Z_{cm2} can be synthesized by common mode voltage controlled current sources [2, 3] according the Ohm's low relationship.

$$Z_{cm1} = \frac{V_{cm}}{I_{cm_1}}, \qquad Z_{cm2} = \frac{V_{cm}}{I_{cm2}} \tag{2}$$

Replacing Eq. (2) in Eq. (1) V_{cm} drops and the condition for Wheatstone bridge impedance balance becomes:

$$Z_{e_1} I_{cm_1} = Z_{e_2} I_{cm_2} \tag{3}$$

The electrode-skin impedances Z_{e1}, and Z_{e2}, by their nature, are not set at a precise value and will change from individual to individual, with electrode location and with time on the same person. If the electrode impedance variation is ΔZ, Eq. (3) can be expressed as:

$$(Z_{e_1} + \Delta Z) I_{cm_1} = (Z_{e_2} - \Delta Z) I_{cm_2} \tag{4}$$

It is clear that the two products shown in Eq. (4) can be equal only when I_{cm1} and I_{cm2} can have a corresponding ΔI change:

$$(Z_{e_1} + \Delta Z)(I_{cm_1} - \Delta I) = (Z_{e_2} - \Delta Z)(I_{cm_2} + \Delta I) \tag{5}$$

So, the matching is possible only when the common mode input currents I_{cm1} and I_{cm2} are continuously adjusted to track the electrode impedance variations with time.

Recently a method for automatic Wheatstone bridge balance was published [4, 5].The approach uses two controlled impedance multipliers: one for resistive control and the other for capacitive control of the amplifier common mode input impedance. By two orthogonal phase-sensitive detectors enclosed in two control loops the active and reactive components of the Wheatstone bridge are automatically adjusted to maintain balanced conditions.

Now, a powerful current driven concept for Wheatstone bridge automatic balance is described, wherein voltage controlled current sources are used instead impedance multipliers.

II. ELECTRODE IMPEDANCE BALANCE

A. Electrode impedance model

The electrode-skin impedance can be modeled by one parallel RC network or by a parallel RC network with serial resistor, as is shown in *Fig. 2*.
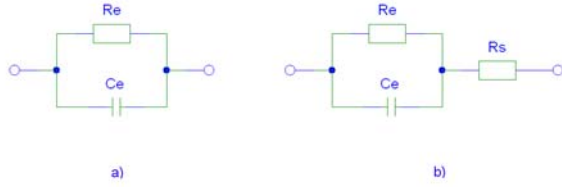

Fig. 2. Electrode impedance model:
a) parallel RC network, *b*) parallel RC network with serial resistor

The impedance shown in *Fig. 2a* has the following Laplace representation:

$$Z_e = \frac{R_e}{1 + sR_eC_e} = \frac{R_e}{1 + s\tau_p} \qquad (6)$$

It has a pole for frequency $\omega_p = 1/\tau_p$. If additional serial resistor is added, Eq. (6) is changed to:

$$Z_e = \frac{R_e}{1 + sR_eC_e} + R_s = (R_e + R_s)\frac{1 + s\tau_z}{1 + s\tau_p} \qquad (7)$$

Where $\tau_z = (R_e\|R_s)C_e$. Eq. (7) has a zero for frequency $\omega_z = 1/\tau_z$. Looking at Eq. (6) and Eq. (7) the conclusion is that the serial resistor R_s or any additional serial resistor inserted in electrode leads, e. g. protection resistors, will tend to equalize electrode impedances, because the pole will be canceled by a zero, i. e. when $R_s \gg R_e$, $\tau_z \approx \tau_p$, and Z_e approaches R_s. From the other side, higher values of R_s will decrease the useful signal, due to voltage divider with the amplifier input differential impedance, and will introduce additional noise. So, additional augmentation of R_s is possible, but should be kept as low as possible.

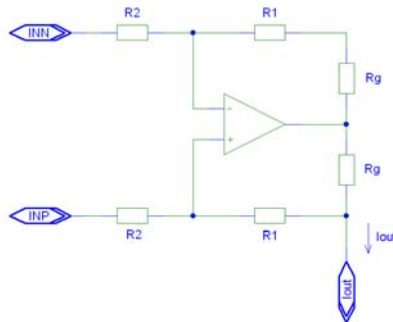### B. Bidirectional Howland current source

Fig. 3. Bidirectional Howland VCCS

The most appropriate transconductance amplifier to drive electrode impedances is the Howland bidirectional VCCS circuit. It is shown in *Fig. 3*.

The transconductance gain *g* is [2]:

$$g = \frac{R_1 + R_g}{R_2}\frac{1}{R_g} \qquad (8)$$

When $R_1 = R_2$, Eq. (8) becomes:

$$g = \frac{1}{R_1 \| R_g} \qquad (9)$$

The worst case output resistance R_{out} can be expressed as [2]:

$$R_{out\_wc} = \frac{1}{4\delta\,g} \qquad (10)$$

where δ is the resistor mismatch. The typical R_{out} can be approximated as:

$$R_{out} \approx \frac{1}{\delta\,g} \qquad (11)$$

For 0.2% resistor relative mismatch, $\delta = 0.002$ and $g = 1/100k$, $R_{out} \approx 50M\Omega$. Note that resistor absolute tolerances are specified, and resistors from one lot have much better relative tolerances.

C. Operating principle

The simplified impedance balance circuit concept is shown in *Fig. 4*. Z_{e1}, Z_{e2} are the electrode impedances, while Z_{cm1} and Z_{cm2} are synthesized by VCCS's G_1 and G_2, generating the input common mode currents I_{cm1} and I_{cm2}. Differential signal is amplified 200 times at node V_{ecg}, common mode signal 2 times at node $2V_{cm}$. If G_1 and G_2 transconductance is *g*, the synthesized common mode resistance per input is, when *Error* signal is zero:

$$R_{cm} = \frac{1}{2g} \qquad (12)$$

Let's assume that the common mode signal $2V_{cm}$ consists of only the fundamental harmonic of the PL interference, i. e. it is a pure 50Hz sine wave. The first mixer *M1* detects the presence of in-phase PLI in the V_{ecg}. The second mixer *M2* is controlled by 5ms ($\pi/2$ for PLI) delayed reference and detects the presence of quadrature-phase PLI in the V_{ecg}. The outputs of the two mixers are integrated, and are enclosed in two negative control loops. The control loops are used to generate real *Re_error* and imaginary *Im_error* error signals. The error signals are added at G_2 input, and subtracted at G_1, input from the common mode voltage $2V_{cm}$ controlled the VCCSs. It should be noted that the two VCVS's are controlled from the common mode voltage, thus the differential input impedance is uninfluenced, and
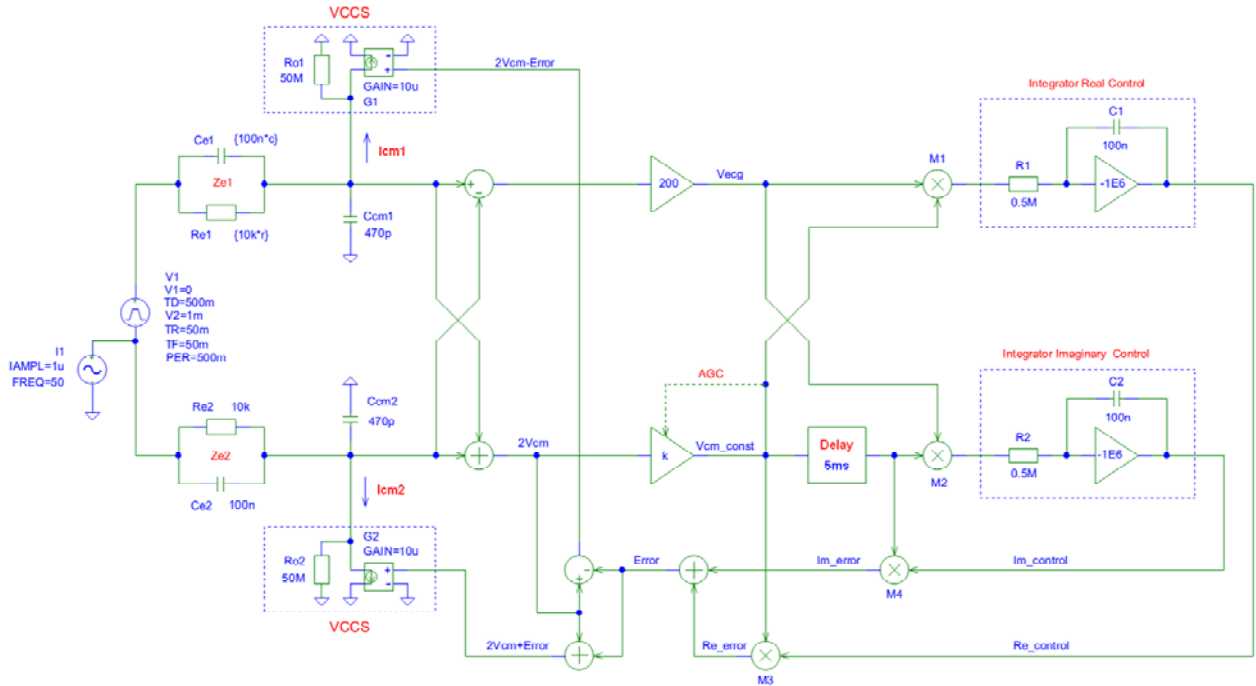
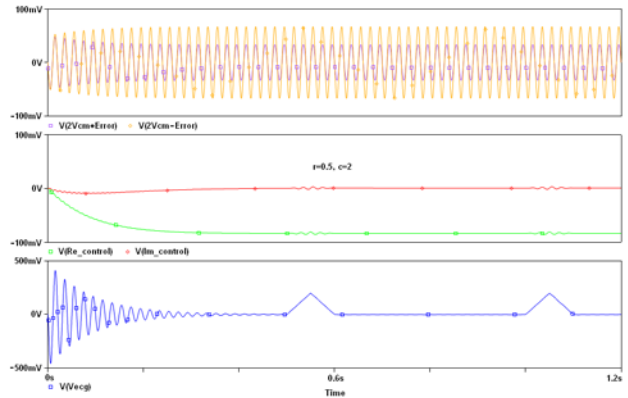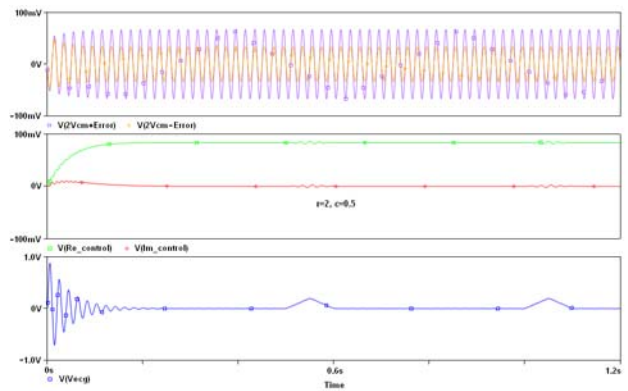Fig. 4. Simplified automatic electrode impedance balance circuit concept

only the common mode input impedance is changed due to circuit operation. In steady-state conditions the integrator outputs *Re_control* and *Im_control* settles at voltages, at which the mixers M_1 and M_2 will detect the absence of in-phase and quadrature-phase PLI in the ECG signal. The two negative feedback control loops automatically equalize the electrode voltage drops, due to flowing common mode PLI current, and cancel the PL interference.

III. PSPICE SIMULATIONS

PSpice simulations of the behavior of the circuit from *Fig. 4* are shown in *Fig. 5*. The electrode imbalance is simulated by varying parameters *r* and *c*. The delay of 5ms is simulated by Laplace VCVS. Instead of ECG signal, a triangle pulse with 100ms pulse width, 1mV amplitude and 0.5s period is used in the simulation.

Five cases of electrode imbalance are simulated by parameters *r* and *c*. The shown signals are as follows. The control voltages $2V_{cm}$-*Error* for G_1 and $2V_{cm}$+*Error* for G_2 are shown on the first trace. The second trace shows control signals *Re_control* and *Im_control*. The third trace shows V_{ecg}. It is clear that the electrode impedances automatically goes in balanced condition, and the PLI is canceled. A case when *Re_control* and *Im_control* are grounded is shown in *Fig. 5f* for comparison.

The gain coefficient *k* is equal to 4 for the all plots. It can be seen that the impedance settling time is different, e. g. in *Fig. 5 a)* and *c)* it is longer than in *Fig. 5 b)* and *d)* due to lower V_{cm} amplitude. For a constant settling time, the amplitude of the signal *Vcm_const* should be kept constant. An automatic gain control, by varying the coefficient *k*, could be added in addition, as is shown in *Fig. 4*.

A) $r = 0.5, c = 2$

B) $r = 2, c = 0.5$

C) $r = 0.5$, $c = 0.5$

D) $r = 2$, $c = 2$

E) $r = 1$, $c = 1$

f) $r = 2$, $c = 0.5$, $Re\_control = Im\_control = 0$V

Fig. 5. PSpice simulation result with six cases of different electrode imbalance.
I trace: $2V_{cm}+Error$, $2V_{cm}-Error$;
II trace: $Re\_control$, $Im\_control$; III trace: V_{ecg}

IV. CONCLUSION

The presented electrode impedance balancing approach breaks the gap between two and three-electrode amplification techniques in regards the quality of achieved signals. The PL interference is cancelled on a hardware level - wherein it is generated, without affecting the spectrum of the useful signal.

The presented approach can be built in digital domain, for example mixers M_1 and M_2 can be implemented as lock-in square wave demodulators, M_3 and M_4 can be realized by digital potentiometers or floating point multipliers [5]. Moreover, flexible algorithms could make the impedance balancing process faster and insensitive to the level of interference, e. g. adding Automatic Gain Control (AGC), changing the loop filter bandwidth during operation, etc.

Finally, it should be noted that due to the first order impedance synthesis in some cases the impedance balance will not be perfect. A popular PL interference removing algorithms could be used in addition, such as subtraction procedure [6, 7], lock-in techniques [8] and high-Q comb filters [9, 10].

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[10] D. Dobrev, T. Neycheva, V. Krasteva, I. Iliev. *High-Q Comb FIR Filter for Mains Interference Elimination*, Annual Journa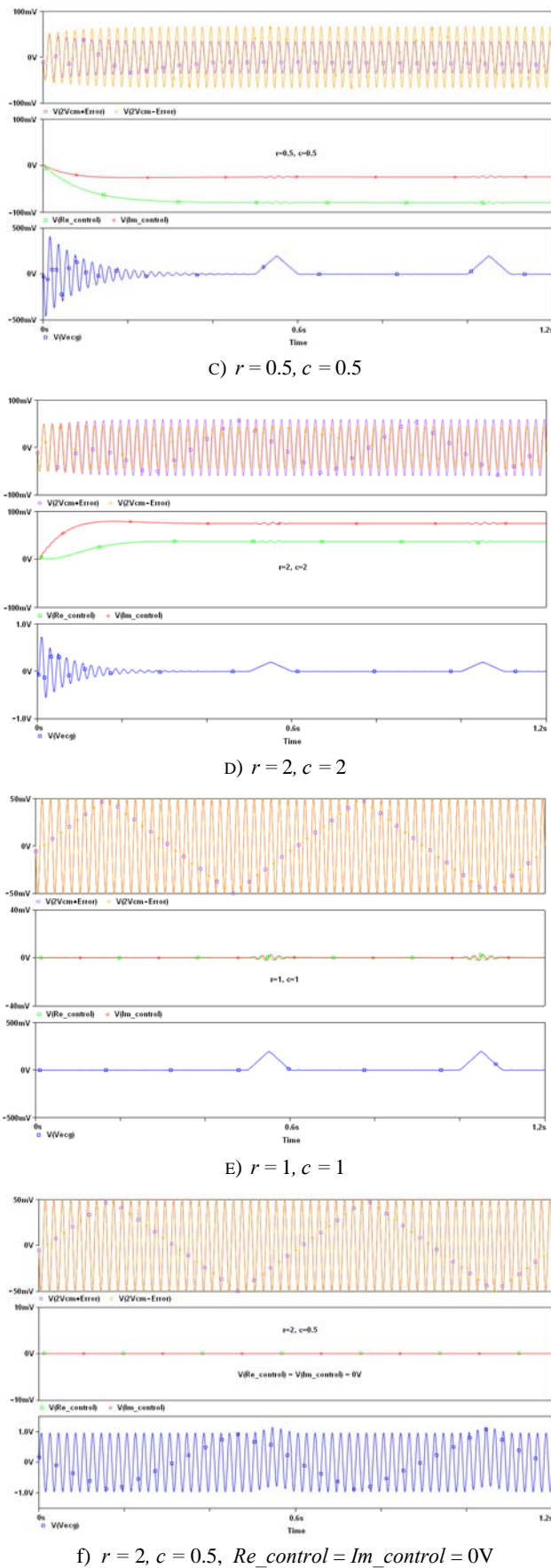l of Electronics, Vol. 4, No 2, pp. 126-129, 2010.