

Software PLL for Power-line Interference Synchronization: Design, Modeling and Simulation

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Abstract – Power-line interference is a common disturbing factor in almost all two-electrode biosignal acquisition applications. Many filtering procedures for mains interference elimination are available, but all of them are maximally effective when the filter notches are positioned exactly at the power-line harmonics, i. e. when the sampling rate is synchronous with the power-line frequency. Moreover, various lock-in techniques, such as automatic common mode input impedance balance, require precise in-phase and quadrature phase references, synchronous with the power-line interference. This paper describes in depth a design procedure of software PLL, generating synchronous reference to the common mode power-line interference, and achieved from its analog prototype using s to z backward difference transformation. The main advantage of the presented approach is that the synchronization is done in software, so it has no production cost. The presented PLL is intended for use in ECG signal processing, but it can be used after easy adaptation in various digital signal processing applications, where frequency synchronization is needed.

Keywords – Digital PLL, All-digital PLL, PLL Design Modeling and Simulation, Power-line Synchronization

I. INTRODUCTION

Power-line (PL) interference is a common disturbing factor in almost all biosignal acquisition applications. As a consequence of electrode impedance imbalance and the finite value of the amplifier CMRR, some AC noise remains even when special signal recording techniques are applied (shielding, driven right leg, body potential driving, etc). A further reduction of PL interference usually is achieved by digital post-filtering. Many algorithms for PL interference suppression are available, starting from simple comb filters [1], to advanced subtraction procedures and lock-in techniques [2, 3], but all of them tend to lose their efficiency when PL frequency differs from its nominal value. Maximal rejection is possible only when the sampling rate is synchronous with the PL frequency, because only at that case, the filter notches coincide with the PL harmonics.

Nowadays, the long-term (>24 h) stability of the PL frequency is very good and many home appliances (radio-clocks, etc.) use it as a real-time clock. Network operators regulate the daily average frequency so that clocks stay within a few seconds of correct time. In practice the

nominal frequency is raised or lowered by a specific percentage (± 200 ppm or ± 0.01 Hz) to maintain synchronization. Over the course of a day, the average frequency is maintained at the nominal value within a few hundred ppm [4].

However, due to the continuously changing load on the power grid, the short-term stability is not perfect. The PL frequency could vary typically below ± 0.1 Hz, but can go as high as ± 0.2 Hz. Larger deviations indicate that the power system operates near its limits and will result in automatic load shedding to prevent the system from collapse.

Note that the PL voltage is produced by many generators connected in parallel. These generators have a large inertial torque, thus the PL frequency could not have rapid changes. The frequency fluctuation usually takes a few tens of seconds due to the large rotating masses involved. A bandwidth of 0.1Hz or higher is sufficient to track these fluctuations.

Recently a lock-in technique for input common mode impedance balance was developed [5]. The approach is based on two digitally regulated control loops to maintain resistive and capacitive input common mode impedance balance. The control loops require precise in-phase and quadrature phase references, synchronous with the common mode PL interference. If the synchronization is lost, the negative feedback can become positive, leading to instability problems and lack of convergence.

Now, software PLL for synchronization with the PL interference is described. It is intended to generate references for input common mode impedance balance in two-electrode ECG signal acquisition [5], but can be used also in other applications where frequency synchronization is a must.

II. ALL-DIGITAL PLL DESIGN

A. All-digital PLL block diagram

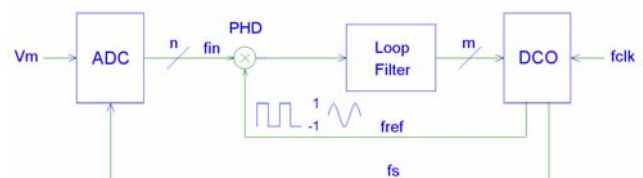


Fig. 1. All-digital PLL block diagram

The all-digital PLL structure is shown in Fig. 1. It consists of Phase Detector (PHD), Loop Filter and Digitally (or Numerically) Controlled Oscillator (DCO or NCO), instead Voltage Controlled Oscillator (VCO) in

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conventional PLL. The difference is that the DCO is a discrete oscillator. Simply, it is a timer or digital-to-frequency converter, whose output frequency is a multiple to the system clock f_{clk} . Another basic difference to analog PLL is the input signal. In analog PLL it is analog, now it is in digital form, after ADC it is n -bits data stream. The mixer or phase detector (PHD) simply is a multiplier with square wave or sine wave reference. The square wave reference greatly simplifies the mixer operation to consequently change the sign of the incoming data [3], instead of floating point multiplication. Next, the Loop Filter (LP) integrates the data in time, and due to averaging increases the resolution, so the DCO input is m -bits ($m > n$) word. For proper processing at low oversampling ratios, the sampling rate f_s must be multiple to the reference frequency f_{ref} .

B. Loop gain linear model in s-domain

Each analog PLL is at least second order control system. The first pole, at DC, is related to the VCO, which serves as an ideal integrator included in the loop [6]. The second pole is due to the Loop Filter, and must be compensated by a zero for stability. Frequently, a third pole is inserted for additional filtering for frequencies where the loop gain is below 0dB.

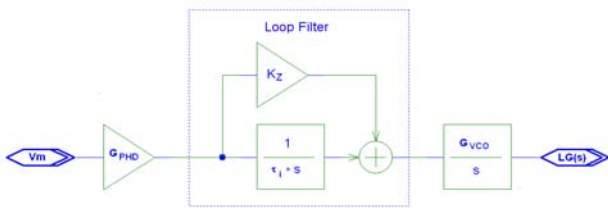


Fig. 2. Loop gain linear model in s-domain

The switching type phase detector gain [3] is:

$$G_{PHD} = \frac{\Delta V_{out}}{\Delta \phi_{in}} = \frac{\pm V_m \cdot 2/\pi}{\pm \pi/2} = \frac{4V_m}{\pi^2}, \frac{V}{rad} \quad (1)$$

The transfer function of the loop filter, shown in Fig. 2, is:

$$G_{LF}(s) = \frac{1 + k_z \tau_i s}{\tau_i s} \quad (2)$$

It is an ideal integrator, compensated with forward path. The integrator unity gain frequency is:

$$f_i = \frac{1}{2\pi\tau_i}, \text{ Hz} \quad (3)$$

Eq. (2) has zero for frequency:

$$f_z = \frac{1}{2\pi k_z \tau_i}, \text{ Hz} \quad (4)$$

For covering all PL frequency fluctuations with reserve VCO range of $\pm 1\text{Hz}$ is enough. Thus, the VCO gain is [7]:

$$G_{VCO} = \frac{\Delta \omega_{out}}{\Delta V_{in}} = 2\pi \frac{\pm 1\text{Hz}}{\pm V_{DD}/2} = \frac{4\pi}{V_{DD}}, \frac{rad}{sV} \quad (5)$$

The VCO serves as an ideal integrator and its transfer function in s-domain is:

$$G_{VCO}(s) = \frac{G_{VCO}}{s} \quad (6)$$

Multiplying Eq. (1), (2) and (6), the loop gain is:

$$LG(s) = \frac{1 + k_z \tau_i s}{\tau_{vco} \tau_i s^2} \quad (7)$$

Where τ_{vco} is:

$$\tau_{vco} = \frac{1}{G_{PHD} G_{VCO}} = \frac{\pi^2}{4V_m} \cdot \frac{V_{DD}}{4\pi} = \frac{\pi \cdot V_{DD}}{16 \cdot V_m}, \text{ s} \quad (8)$$

For typical $V_m = 0.5\text{V}$ and $V_{DD} = 3.3\text{V}$ Eq. (8) becomes:

$$\tau_{vco} = \frac{\pi}{16} \cdot \frac{3.3}{0.5} \approx 1.3, \text{ s} \quad (9)$$

Equalizing Eq. (7) to unity when $k_z=0$, and substituting $s=2\pi f_u$, the unity gain frequency of the uncompensated loop gain (40dB/dec) can be found:

$$f_u = \frac{1}{2\pi\sqrt{\tau_{vco}\tau_i}}, \text{ Hz} \quad (10)$$

The unity gain frequency of the compensated loop f_c , when $k_z > 1$, can be found taking into account that f_u is in a geometric mean with f_z and f_c :

$$f_c = \frac{f_u^2}{f_z} = \frac{2\pi k_z \tau_i}{4\pi^2 \tau_{vco} \tau_i} = \frac{k_z}{2\pi \tau_{vco}}, \text{ Hz} \quad (11)$$

For $\tau_{vco}=1.3\text{s}$, $\tau_i=1\text{s}$ and $k_z=8$ using Eq. (4), (10) and (11), the frequencies f_z , f_u and f_c can be found as:

$$f_z = 0.02\text{Hz}, \quad f_u = 0.14\text{Hz}, \quad f_c = 0.98\text{Hz} \quad (12)$$

Note, that the unity gain frequency f_c corresponds to the 3dB bandwidth of the closed loop system, illustrated in Fig.3. The closed loop bandwidth f_{3dB} is about 1Hz, and is fast enough because a bandwidth of only 0.1Hz is sufficient for tracking PL frequency.

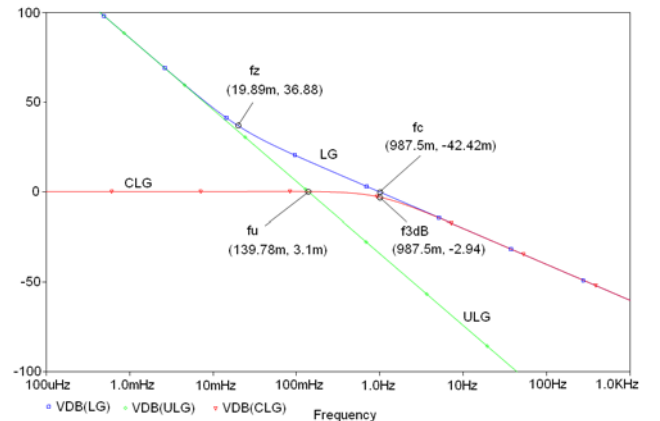


Fig. 3. Loop gain (LG), uncompensated loop gain (ULG) and closed loop gain (CLG) vs. frequency

C. Loop gain linear model in z-domain

The transfer function of an arbitrary integrator in s-domain is:

$$T(s) = \frac{1}{\tau_i s} \quad (13)$$

The transfer function of the same integrator in z-domain is:

$$T(z) = \frac{T}{\tau_i(1-z^{-1})} \quad (14)$$

Where, $T=1/f_s$ is the sampling interval. Equalizing Eq. (13) to Eq. (14) leads to the relation:

$$s = \frac{1-z^{-1}}{T} \quad (15)$$

Eq. (15) is the so called *backward difference operator* for mapping s -plane to z -plane, wherein the left half-side of the s -plane is mapped into circle with radius $r=0.5$ and center $(0.5, 0)$ in the z -plane, inside the unit circle. Important property of the mapping is that stable analog filters are transformed into stable digital filters [8].

Thus, replacing s with Eq. (15) in Fig. 2, z -domain equivalent model easily can be found. For simplicity the product of $G_{PHD}G_{VCO}$ is replaced by $1/\tau_{vco}$, see Eq. (8).

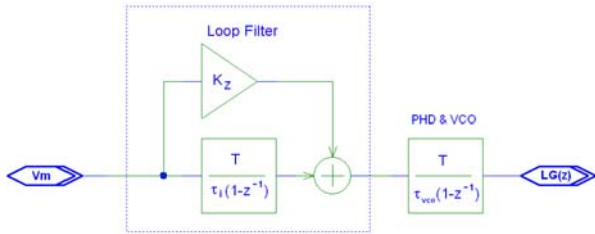


Fig. 4. Loop gain linear model in z-domain

The frequency response is shown in Fig. 5 appended to the s -model simulated curves from Fig. 2. Sampling rate is 2kHz, i. e. $T=0.5$ ms. Phase response is also given in Fig. 5. It can be seen that the phase margin (when the loop gain intersects 0dB axis) is 89 degree.

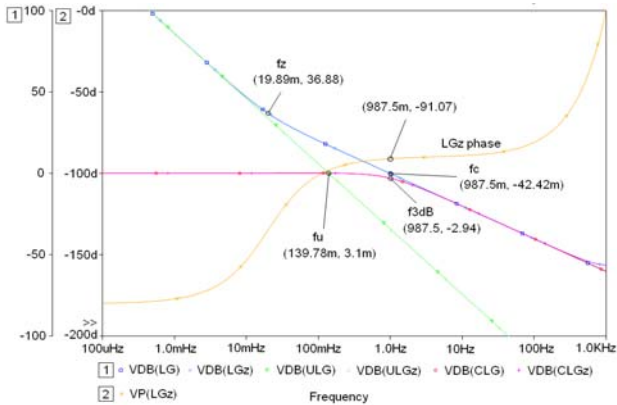


Fig. 5. 1 axis: Loop gain curves from s and z models.
2 axis: Loop gain phase response

In conventional PLL design usually a third pole is inserted for high-frequency filtering and reducing VCO jitter. It affects frequencies faraway from 0dB point to maintain stability. The best and simple way for high-frequency filtering is by one PL period moving-average filter (averager). Adding one PL period averager will introduce group delay of 10ms in the loop. Evaluated at

1Hz this delay corresponds to 3.6 degree phase lag. Adding additional delay of one sampling period, or 0.18 degree, the total phase margin will drop by about 4 degree. We can conclude that adding 1PL period averager in the loop is possible and will reduce the phase margin from 89 to 85 degree which still preserves very good stability. The modified loop filter by added 1PL period averager is shown in Fig. 6. The delay of one sampling period is added in the numerator of the PHD&VCO model.

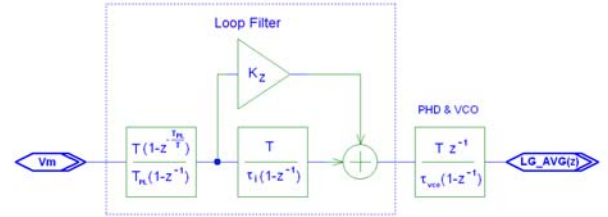


Fig. 6. Loop gain with added averager

Thus, the loop gain can be expressed as:

$$LG_{AVG}(z) = LF(z) \frac{Tz^{-1}}{\tau_{VCO}(1-z^{-1})} \quad (16)$$

Where $LF(z)$ is the loop filter transfer function:

$$LF(z) = \frac{T(1-z^{-\frac{T_{PL}}{T}}) T + k_z \tau_i (1-z^{-1})}{T_{PL}(1-z^{-1}) \tau_i (1-z^{-1})} \quad (17)$$

Simulation of the loop gain from Fig. 6 is shown in Fig. 7. The simulation conforms that phase margin drops to 85 degree.

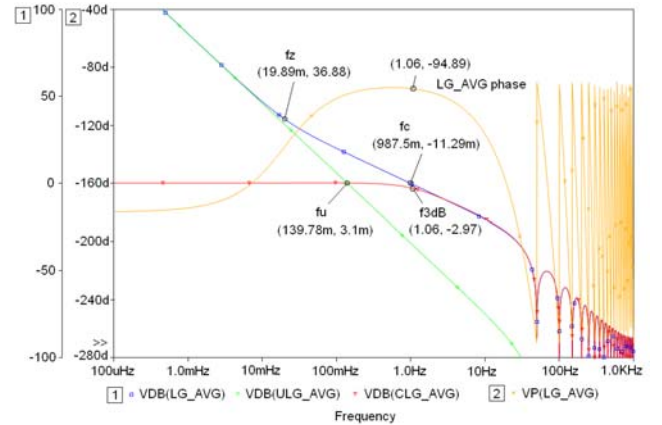


Fig. 7. 1 axis: Loop gain curves with averager.
2 axis: Loop gain phase response

Substituting the parameters with their values in Eq. 17, i. e. $T_{PL}=20$ ms, $T=0.5$ ms, $\tau_i=1$ s, $k_z=8$, the loop filter can be realized as structure shown in Fig. 8.

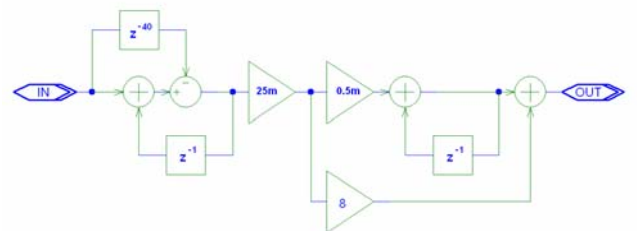
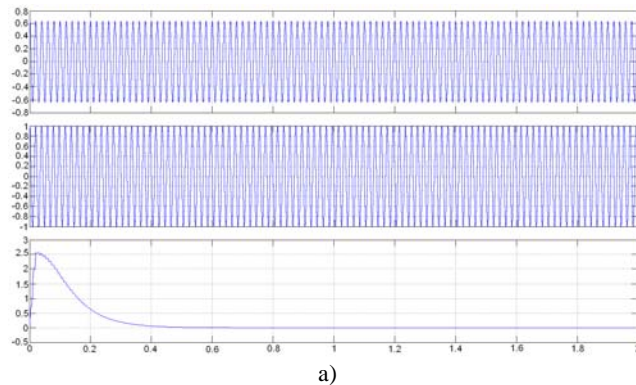


Fig.8. Loop filter realization for 2 kHz sampling rate

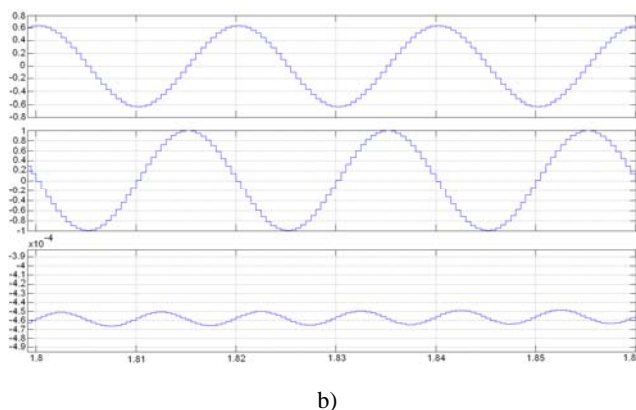
It should be noted that the loop speed depends on the input signal amplitude. Automatic Gain Control (AGC) of the input signal amplitude could be added in addition for constant settling time.

D. Matlab simulation

Matlab simulation is run to evaluate the stability of the designed PLL in transient analysis. The simulation scheme consists of loop filter structure shown in Fig. 8 and DCO with sensitivity $\pm 1\text{Hz}/3.3\text{V}=0.6\text{Hz}/\text{V}$, see Eq. (5). To show the phase difference between input and reference waveforms, sine wave mixing is used instead of square wave. Because the phase detector gain in sine wave mixing is $4/\pi=1.274$ times lower than in square wave mixing written with Eq. (1), the input amplitude V_m is increased 1.274 times or $1.274 \times 0.5\text{V}=0.637\text{V}$ to keep the loop speed. The simulation result is shown in Fig. 9. The first trace is the input frequency, the second trace is the DCO generated reference, and the third trace is the DCO input. In Fig. 9b the signals from Fig. 9a are zoomed at 1.8s simulation time.



a)
I trace: input sine wave with 0.637V amplitude,
II trace: DCO output sinusoid with 1V amplitude,
III trace: DCO input control voltage



b)
Zoom at 1.8s simulation time

Fig. 9. Matlab simulation

From the DCO input shown in the third trace in Fig. 9a, it can be seen that the loop has stable response. When the DCO input is settled the generated reference leads the input sine wave in 90 degree, see the second trace in Fig. 9b. The third trace in Fig. 9b shows the remained ripples in the DCO control voltage, which are with doubled frequency

and about 10uV amplitude. To minimize the DCO input remaining ripple the ADC sampling rate must be multiple to the generated reference. Thus, the averager included in the loop filter will have maximal rejection for PL harmonics.

E. Frequency resolution

The DCO is a discrete oscillator, in other words it is a digital to frequency converter, so it will jump within a discrete frequency step depending on a system clock f_{clk} . Nowadays, the modern microcontrollers for signal processing have system clock $f_{\text{clk}} \geq 100\text{MHz}$. Evaluating the ratio $50\text{Hz}/100\text{MHz}$ it can be found that the frequency resolution at 50Hz is 0.5ppm or 25uHz. The DCO full scale range is 2Hz. It is covered by $0.5\text{ppm} \times 50\text{Hz}/2\text{Hz}=12.5\text{ppm}$ steps or about 16bits. So, depending on the system clock frequency, the DCO input can be a 16bits word, and 1LSB of the DCO will correspond to about 30uHz at 100MHz clock. The ADC resolution could be few bits lower, e. g. 12bits, because the resolution is increased due to averaging in the loop filter.

III. CONCLUSION

The design procedure of software PLL was described in details. The PLL structure is derived from its analog prototype using s to z backward difference transformation. The PLL generates synchronous reference to the common mode power-line interference. The main advantage of the approach is that the synchronization is done in software, so it has no production cost. The presented digital PLL is intended for use in ECG signal processing, but it can be used after easy adaptation in various digital signal processing applications, where frequency synchronization is needed.

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