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High Efficiency UV Photodiodes Fabricated on p-type Substrate

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Abstract – **Newly developed "pure-boron" photodiodes, with high sensitivity and stability in the whole ultraviolet range (UV), are described. The main purpose of this work is to create and characterize a large-area UV photodiode, representing a structure of a pixel in a backside illuminated CMOS image sensor, featuring maximum fill factor and hence sensitivity. The diodes have been processed by the Technology center of DIMES (Delft Institute for Microsystems and Nanoelectronics) on a p-type epitaxial wafer and thus are compatible with standard foundry processing. Care has been taken to keep the electrodes buried as much as possible to limit dark leakage current from interfaces. An electrical and optical characterization has been done by PTB (Physikalisch-Technische Bundesanstalt) using the UV beam lines of the Storage ring facility BESSY in Berlin.**

Keywords – **Pure-boron, p-type substrate, CMOS compatibility, backside illumination, CMOS image sensors**

I. INTRODUCTION

"Pure-boron" (pure-B) diode, fabricated on an n-type starting material, has been well described before in [1], [2], [3], [5]. The name "pure-B" designates the most important production step for creating the photodiode. In this step, a few nanometers thin amorphous pure boron layer is deposited on silicon by means of CVD (chemical vapor deposition) process.

Here we propose a p-type starting material to implement the photodiodes. The advantages, among others, are: standard CMOS processing compatibility, and the ability to utilize the same process for building the pixels in a backside illuminated image sensor [6]. The stack consists of a highly doped p-type substrate, p-epitaxy, n-cathode (buried), and high resistivity p-epitaxy. The pure boron is deposited as a final step on this stack, prior to metal contact formation (Fig. 1).

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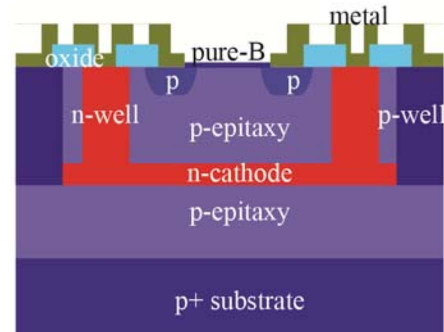

Fig. 1. Diode cross-section showing the stack composition (not to scale)

II. DIODE FABRICATION

A. Processing steps (down to top)

1. Starting material: highly doped (~1×10^{19} at/cm^3) boron doped material is used as a substrate. This is also the choice of material for CMOS image sensors, to limit the collection of generated photo carriers from very deep in Si. The diffusion process would create a cross talk, and would result in blur (loss of modulation transfer function: MTF).
2. p-epitaxial layer: a 2.5 μm p-epitaxial layer with a doping concentration of 1×10^{17} at/cm^3 is formed on top of the p^+-substrate. This layer shields the cathode from the low-quality crystalline interface of the p^+ substrate, and hence reduces the dark leakage current.
3. n-cathode: the 1 μm phosphorous doped cathode (1×10^{16} at/cm^3) is formed on top of the buried p-epi layer. The concentration is chosen such that it is not high enough to cause early diode breakdown, but not very low that it prevents full depletion of the high resistivity p-epitaxial layer.
4. Sidewall inverting implant: to prevent a p-n junction being formed in the diode sidewalls, a low energy inverting implant is used (boron, 100keV, 5×10^{12} at/cm^2). The same mask as that of the deep p-well is reused in this step.
5. High resistive p-epitaxial: this 1.5 μm high resistivity region (~ 1×10^{14} at/cm^3) should be fully depleted under normal operating conditions.
6. Deep wells: high energy (500keV) p-and-n implants are used to create the deep wells (1.5 μm) that form a ring around the diode. The p-well is connected to the anode ring while the n-well connects the top cathode contact with the buried cathode. Thanks to the pre-p implant, it can be ensured that the cathode

is properly inverted without having to rely completely on the deep p-well.

7. Contact implants: shallow p^+ and n^+ contact implants to the anode and cathode are formed. After the boron deposition, n and p metal contacts will be made on the electrodes.
8. Annealing: the wafers get a 30 minute annealing at 950C.
9. Boron deposition: A 375 nm oxide is used as a mask for the selective deposition of boron through a CVD (chemical vapor deposition) process. The thickness of the boron layer as deposited is 3 nm.
10. Metallization: 0.875 µm thick aluminum is used for the contact metal. This is alloyed at 400°C for 30 minutes.

B. Diode design and layout

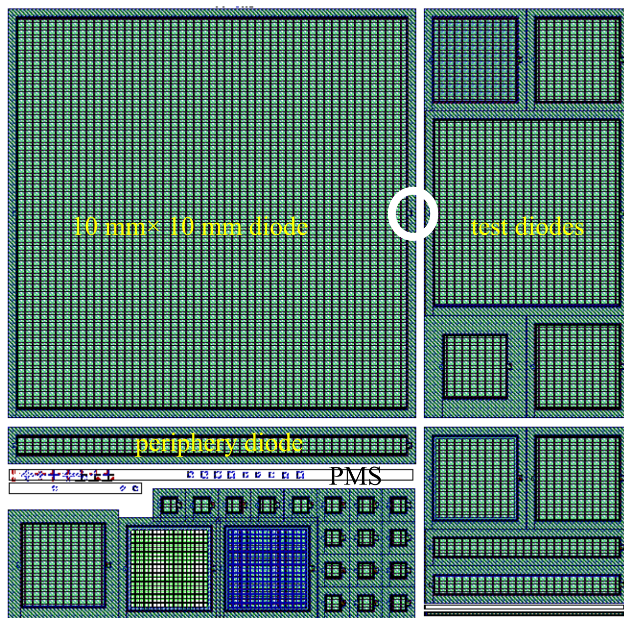

Fig. 2. Top view of the layout containing the 10 mm × 10 mm diode, the periphery diode, various test diodes and process monitoring structures (PMS)

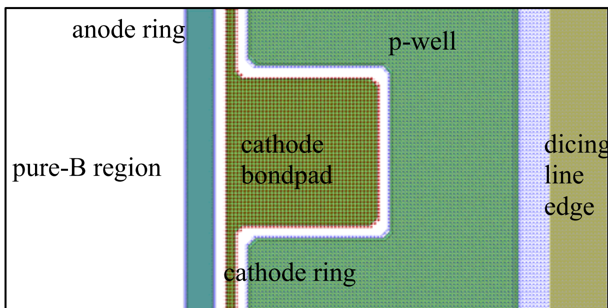

Fig. 3. Section of the diode layout (white circle in the top view) showing the important implant regions

The top-layout of the mask containing the 10 mm × 10 mm diode as well as several test structures is shown in Figure 2. A zoom-in view of the diode (white circle) is shown in Figure 3. The p-well ring (~ 185 µm) surrounds the entire structure to isolate the die edge. The n-type well ring is 9 µm wide, while the shallow p-type anode ring is 18 µm. The cathode ring is separated from the p-well as well as the anode by 6 µm to reduce high electric fields. The anode ring is connected to the p-well ring by opening the n-well ring, so that both are in the same potential. Further, they both vertically connect to the p-epitaxy and p^+-substrate. The width of the open region sensitive to photons (covered with pure-B) is 9.1 mm.

In addition to the diode, several test devices are also designed in the same mask intended for process control. This included perimeter diodes (with a larger perimeter-to-area ratio), as well as several design variations such as to monitor the current leakage from the sidewalls.

III. Measurement

A. Electrical measurement

The I-V characteristics of the pure-B based on p-type substrate is shown in Figure 4, and the equivalent diode representation in Figure 5. The dark current is low, with an average dark current of 260 pA at 0.5 V reverse bias, and comparable to the n-type diodes presented before [1], [2], [3]. The contribution from the deep junctions was found to be negligible (Figure 5). From comparison with the periphery test diodes, it was found that the leakage current was dominated by the area component (> 95%).

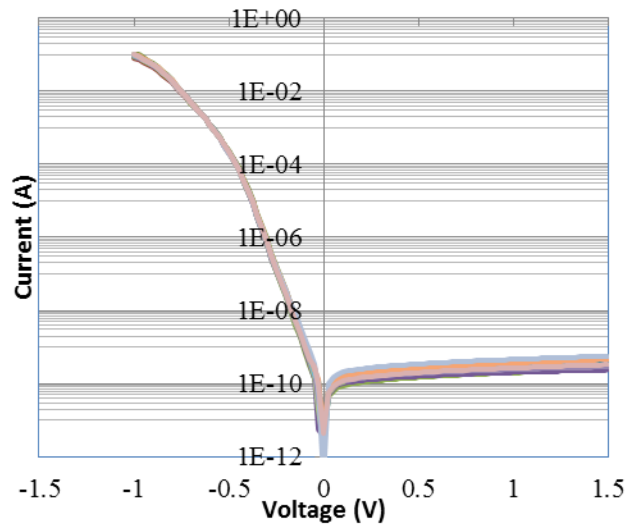

Fig. 4. I-V characteristics of 21 diodes on wafer level in dark

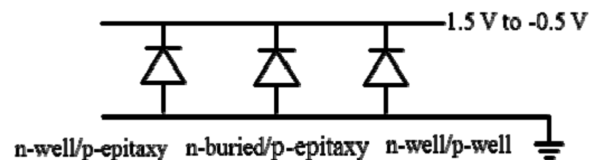

Fig. 5. Equivalent circuit of the diode depicting the different diode sections contributing to the dark current. The n-well p-epitaxy provides the lateral depletion into the p-epitaxy region, while the n-buried/p-epitaxy provides the vertical. The dark current contribution of the sidewall p-well/n-well is negligible

B. Optical measurements

I. Deep UV (DUV), and Vacuum UV (VUV)

All optical tests were carried out at the synchrotron radiation laboratory of PTB (Physikalisch-Technische Bundesanstalt) in Berlin, Germany.

In DUV/VUV, the absorption depth is very short, for example 6 nm at 193 nm. This is also the wavelength which is preferred in modern lithography.

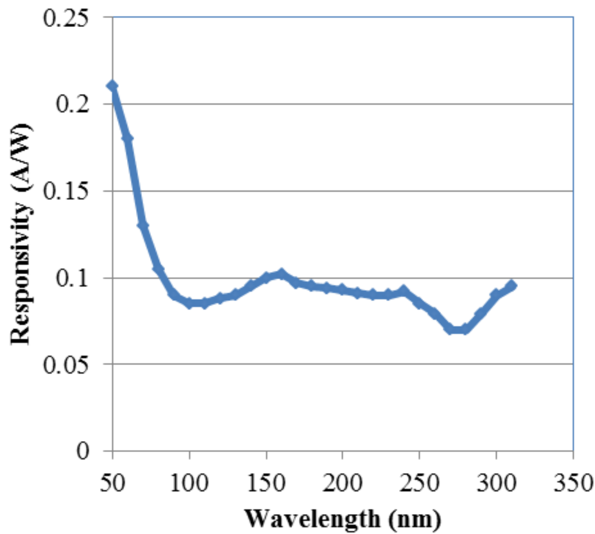

Fig. 6. Responsivity measured in the VUV/DUV range

It can be seen from Figure 6 that these diodes exhibit good responsivity in DUV of more than 0.07 A/W in the whole VUV/DUV range. Simulation indicates that the diodes have an effective dead-layer of 10 -- 15 nm. The dead-layer is a result of various components: a) presence of recombination centers in the interface, b) reduce lifetime of carriers in the highly doped boron region, c) presence of reverse electric fields that act as a potential barrier for minority carriers from being properly collected, and d) recombination of carriers in other regions in the diode such as the sidewalls. In the case of the pure-B diodes on a p-substrate, the main mechanism responsible for the dead layer in DUV is a reduced lifetime in the highly doped boron region.

II. Extreme UV (EUV)

The penetration depth of EUV photons around 13.5 nm wavelength is about 700 nm. To ensure a good collection of photons, the total active diode thickness has been chosen to be 5 μm. The high resistivity p-epitaxial region, the n-cathode, as well as the p-type epitaxial region provides collection of photons in this UV regime. It must be noted that a depletion zone is created in the bottom p-epitaxy region, which allows collection of carriers. It is evident from Figure 7 that the responsivity is more than 0.26 A/W at 13.5 nm which is also the work horse of next generation lithographic machines.

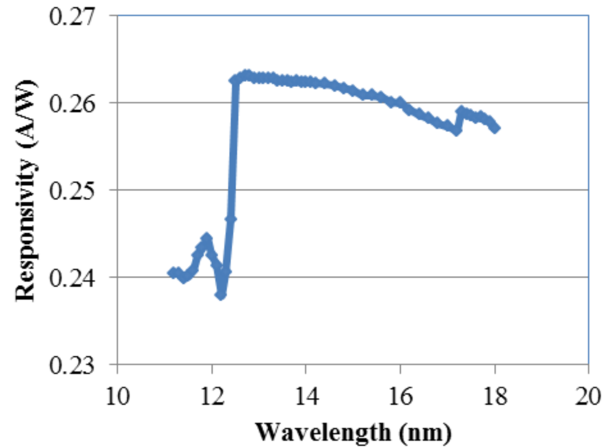

Fig. 7. Responsivity measured in the EUV range

Thus, these diodes are able to be utilized as a broadband detector that can work in the whole UV range, rendering a single design solution for multiple application domains.

III. Stability

To check the stability, the diode was irradiated at 121.6 nm with a power of 179 nW for about 40 minutes, and the diode signal monitored (Figure 8). It can be seen that most of the loss occurs in the first few seconds, of up to 8%.

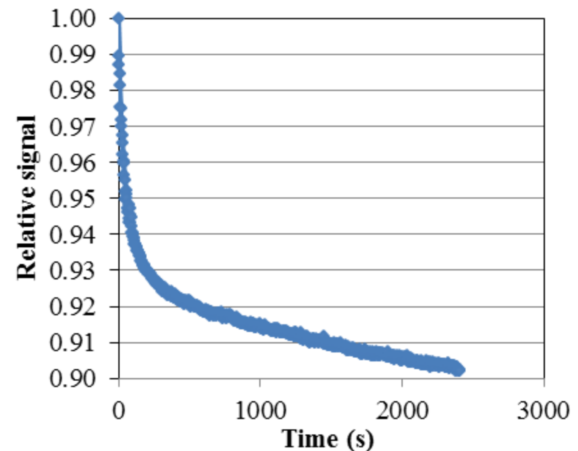

Fig. 8. Stability of the diode: the diode was irradiated at 121.6 nm, with a power of 179 nW for about 40 minutes

A recovery after the irradiation was also noted as shown in Figure 9. It was concluded from this test that the diodes exhibit stability characteristics similar to the diodes fabricated on n-type substrate that have been demonstrated before [7].

IV. Discussion

In this paper, the technology of pure-B has been implemented for producing photodiodes on p-type substrates. P-type substrates are standard for commercial silicon fabrication foundries. It has been found that these diodes retain the same qualities as the diodes fabricated on n-type substrate. Moreover, these diodes yield themselves to be utilized for image sensor pixels that are backside illuminated.

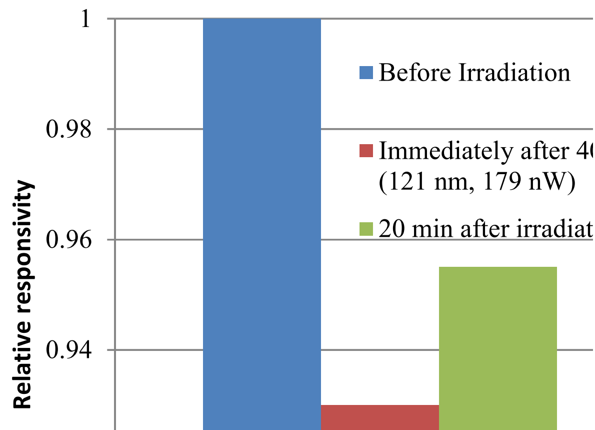

Fig. 9. Recovery of the responsivity after irradiation, probed at the centre of the diode

The pure-B can then be processed on the back surface, as a substitute for the standard ion-implantation.

The disadvantage of the ion-implantation is the roll off created by the doping profile, as well the deep diffusion in to the bulk of the substrate that makes the detector almost non-useable in the DUV/VUV ranges.

The as deposited pure-B is 3 nm. However, due to the ~ 700° C deposition temperature, there is an in-diffusion into silicon of a few nm [1], [2]. The sharp gradient results in a delta-doping profile, and creates an internal electric-field that directs the minority carrier (in this case electron) towards the depletion region. This helps the diode to be sensitive in the DUV range. Similarly, for the diode to be sensitive in the EUV regime, the thickness of the total collection volume is maximized (5 μm). There is negligible recombination loss of the deeper penetrating EUV photons in the 1 μm cathode region.

To reduce the dark current, the cathode is kept “buried”. This means, no part of its depletion with the p-type interacts with the substrate that is of a lower crystalline quality. Similarly, the sidewalls are adequately annealed to remove any defects due to the high-energy sidewall implants. This results in a diode that is dark-current limited by the diode depletion region.

In case of a backside illuminated image sensor, the cathode would be formed as part of a standard CMOS process using shallow junction implants (front-end processing). Thus deep n-well implants are not required. The deep p-well implants are still required to connect the pure-B layer that would be deposited in the backside of the sensor, facing the incoming optical path. One of the challenges is the thermal budget required for such a deposition, which is limited by the thermal budget of the metal layers. However, it has been demonstrated that high quality boron can be deposited at acceptable temperatures, with good optical and electrical performance [8].

V. Conclusion

Pure-B based photodiodes fabricated on p-type substrates exhibit good sensitivity and stability in the whole UV range. These diodes can be manufactured in a CMOS compatible process. They lend themselves into pixels that can be used in backside illuminated CMOS image sensors. These diodes exhibit very good dark current properties as well, and therefore are suitable in various applications that require good sensitivity, stability and dark current performance in the UV regime.

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