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Development of the Personalized Recommender System COsys for Career Orientation

Malinka Spasova Ivanova and Tsvetelina Georgieva Atanasova

Abstract - In the paper the implementation of the System for Career Orientation COsys for university level students and after that when they become lifelong learners is presented. This work is a reflection of the enormous needs for an improved and flexible transition of students from the university settings to their future workplaces in the industry. The main idea behind COsys is to propose a personal and social-oriented learning environment forcing students to perform self-analysis of their current competences and to learn by recommendations. Also, it supports skills development related to CV and motivational letter writing as well as preparation for interview.

Keywords – Recommender system, Personalized learning, Socialization, Career orientation

I. INTRODUCTION

In the last decade the interest on the topic about services development for career orientation has dramatically increased [1] – [3]. Almost all universities over the world, including in Bulgaria, possess centres for career development with aim to advise young people and to support them in their career orientation. These services are often used by our students for preparation for a given job and job searching. On the employers' side, human resources departments are well developed and they very rigorously select the perfect employee for a given position. It means that a student has to know what his future plans and goals are; what is the level of his current knowledge and what kind of competences he must possess in order to secure his dream job position. The quality and effectiveness of career development services proposed by universities will increase if the services are automated and if they allow each student to personally see the real situation of his current knowledge as well as to support him through the recommendation of a suitable learning path.

Career orientation unites the process of choosing a profession and lifelong learning. As it to be efficient, the movement of a student from an education institution to the corporate sector should happen as smoothly as possible. COsys suggests possible solutions of the above described problems.

The aim of this paper is to present the developed COsys with functionalities for competences testing, learning path recommendation, searching for knowledge, giving support in CV and motivation letter writing, giving assistance in

M. Ivanova is with the College of Energy and Electronics, Department of Electronics and Computer Technologies at Technical University of Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: m_ivanova@tu-sofia.bg

T. Atanasova is with the Department of Computer System and Technologies, Faculty of Mathematics and Natural Science at South-West University "N. Rilski", 66 Ivan Michailov str., 2700 Blagoevgrad, Bulgaria, e-mail: atanasova.tsvetelina@gmail.com interview preparation. COsys is designed as a web-directed application and its development is based on social Web 2.0 technologies, recommender systems techniques and programming language Ruby on Rails.

II. METHODOLOGY

The following methodology is applied at the COsys realization: (1) development of survey tools for analysis of the most important and critical competences for every individual student and according to that generation of personal recommendations for learning, (2) detailed exploration and analysis of the needed competences of an employee for successful realization, taking into account the opinions of Bulgarian companies and 50 students from South-West University "N. Rilski", (3) applying Unified Modeling Language for COsys functionality description and design, (4) examination of existing algorithms for recommendation generation, (5) using the principles of software engineering for system development. The system is implemented on Ruby on Rails, using WEbrick web server, SQLite RDBMS, Redis digital repository.

III. COMPETENCES ANALYSIS

The first step of COsys development is related to clearing and understanding the connecting points between the universities' level of engineering education and the corporate sector requirements. For this purpose a survey tool is created and distributed to managers of ICT companies and students. Also, a statistical study is performed during seminars organized by the Career center of the local university. Managers of 10 companies and 50 students are interviewed. They had to answer questions like the following: "Do you think that the young students possess the listed competencies?" (to the managers) and "Do you think that you possess the listed competencies?" (to the students). The suggested competencies for voting are grouped into five categories: technical - available technical skills, including skills for programming and skills for working with hardware devices; functional - abilities for performing of concrete engineering activities related to the job position, social - competences related to the human behavior and effective communication and socialization, global - abilities for working in multicultural team, meta ability for knowing how to learn, how to adapt, how to assess

We wish to understand whether the knowledge framework of employers and the future employees is synchronized or whether there is a gap between them.

The survey results show several differences and similarities in expectations of the company managers and the students' point of view about their university education and their future work realization (Figure 1). The following

competences are important for the employers according to their opinion: technical - technical skills, computer skills; functional skills - office skills, selling skills, entrepreneurship; social - communication, skills for socialization; global - foreign language; meta - adaptivity, motivation, willingness to work, and efficiency.

Students' higher vote is given for competences such as: technical - computer skills; functional - client servicing; social - communication, ability for socialization; meta motivation, self-management, willingness to work, efficiency, adaptavity.

As it can be seen the main differences are related to the technical and functional skills. Also, students have not pointed the knowing of foreign language as a competence with high priority. Another difference is discovered in the meta competences set - ability for self-management is chosen by students as an important competence.

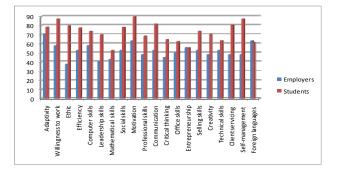


Fig. 1. Needed competences according to the responders

This comparison shows that the connection between the university education and the job market is not efficient, because of the differences between the students' expectations and the real requirements for specific competencies from the side of managers. On the other hand, the students need a personalized environment to support them in their career development. In this sense, the system COsys is designed with the aim to offer a possible solution for students to improve the mandatory competencies they have lack of.

IV. COSYS FUNCTIONAL DESCRIPTION

The functional analysis of COsys is performed with support of UML notation that is applied in preparation of a deep explanation about the functionality of the software system.

COsys includes six modules to support students in their competences evaluation according to the requirements of a concrete job position and to recommend appropriate learning paths.

The first module is *Registration* and its functions offer a possibility for creation of an account in COsys system and an individual student profile preparation.

The second *Competences Analysis* module proposes a quiz and makes an analysis about the existing student's competences.

If there is a discrepancy between existing and required competences for a given job position then the third module *Recommender* generates recommendations with a suitable learning path to this student.

The forth module *Market Information* includes search engine and the possibility for looking of available job positions.

The fifth module *Access to Information Resources* connects a student to the information resources – for example how a CV to be written, how a motivational letter to be constructed or what are the steps for interview preparation.

The last module *Learning Sources* suggests two types of learning sources that could improve student knowledge in a given domain. The first learning source is related to materials in different media format like ebooks, dictionaries, scientific papers, lecture notes, presentations, videos and other electronic resources. The second type leaning sources includes human experts and more experienced persons who share their knowledge in socialoriented online environments.

V. RECOMMENDATION APPROACH

Nowadays, the recommender applications are widely used for information filtering and offering to users information products close to their personal interests, including products with human social elements like professionals, groups of interests, social events [4] - [7]. One definition of recommender systems is given in [8] and they are described as applications that produce individual recommendations or as approaches that direct every individual user to interesting and useful for him products among a big amount of possible choices.

For purposes of this work seven classes of recommender systems are explored with aim one approach to be chosen for implementation in COsys (Table 1).

TABLE 1. CLASSES OF RECOMMENDER SYSTEMS

Classes	Description
Content-based	It recommends resources that a user has read or has liked in the past
Collaborative- based	It recommends resources that are read and liked by users with similar profiles compared to the current user
Demographic- based	It recommends resources that are read and liked by users with similar demographic profiles
Knowledge- based	It recommends knowledge in a given domain
Learning path-based	It recommends knowledge formed in learning paths
Social societies- based	The recommendations are produced as consequences of social relations and communications of a user
Hybrid	It includes two or more from the above mentioned techniques

The recommendations generation in COsys is based on collaborative filtering of items with similar rating results. In our case, the rating type is formed by the number of likes and dislikes related to a given learning resource. The userbased kNN model for collaborative filtering with a variant of the Jaccard similarity coefficient is applied after detailed exploration of existing research [9] – [11]. The Jaccard coefficient shows the similarity between two users in one system where the users like or dislike a resource and it calculates according to the following formula:

$$I(u_1, u_2) = \frac{|L_{u1} \cap L_{u2}| + |D_{u1} \cap D_{u2}| - |L_{u1} \cap D_{u2}| - |D_{u1} \cap L_{u2}|}{|u_1 \cup u_2|}$$

where J is the Jaccard index of similarity between users u_1 and u_2 , L and D are respectively like and dislike user's activity.

Also, the probability can be calculated and it is possible for a prediction to be done whether a given user will like or dislike a given resource:

$$P(u, resource) = \frac{\sum_{i=1}^{n_L} f(u, u_i) - \sum_{i=1}^{n_D} f(u, u_i)}{n_L + n_D}$$

VI. PERSONAL LEARNING BASIS

The concept of Personal Learning Environments (PLEs) is still in a developing stage. Researchers are working on forming the functional, technical and educational framework of PLEs. Anyway, there are good practices related to the PLEs implementation [12] - [14]. The main idea is that learning is under the control of every individual person who possesses concrete learning needs and goals in a given moment. Usually, PLEs are web based applications and they aggregate in real time several information and knowledge sources according to the arranged tools of users. Also, users can integrate social driven tools converting one part of their PLEs in social media. It means that a PLE is defined as a controlled environment in context of learning goals and learning domain, every PLE is organized as an intentional environment. On the other hand every individual learns in serendipitous way taking the advantages of shared knowledge in an unexpected messages stream of other users.

COsys integrates this concept of PLEs, proposing sn unique learning environment with features of personalization and socialization, of intentional and unexpected learning (Figure 2).

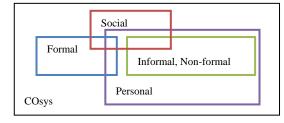


Fig. 2. COsys as a personal and social environment

VII. COSYS IMPLEMENTATION

COsys is mainly written in Ruby on Rails [15] following the principles of software engineering and applying agile software development process. The technical architecture of COsys consists of three layers and it is presented on Figure 3. The first layer is a web browser. The second layer includes the WEBrick server that is used as a web server managing the Ruby application. The Dispatcher distributes the requests from the server to the controllers. The controllers arrange the information and send it as a result to the client through Action or through Active Record to the Recommendable Gem. The Recommendable Gem reads the information from Redis and reads and writes from Resque. The third layer has two databases. Redis stores data about the rating and recommendation of materials. RDBMS (relational database management system) SQLite contains data about all the rest, like registration info, use profile and set of collected materials.

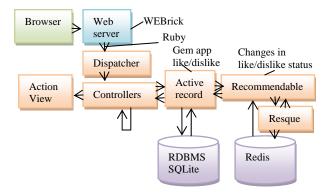


Fig. 3. Technical architecture of COsys

The developed web-based application COsys contains friendly user graphical interface. It is intuitive and easy for navigation. It ensures fast access to the main modules of the system through the right menu. A screen shot with recommended resources is presented on Figure 4.

D Tecross Thropeformen S Fooders Eller	Препоръчани материали			
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Comm	How to improve stamwork	Hits / www.manuecturing.co.ut/manueckinter	.0	9
lecture .	Act of Pullic Speaking- the Grantest Speeches in History	Nopu/www.theprestummet.com/tgutoumestownet_penet_eps/104+225		0
Aproperne Sperophysics 10 met	Europato ormape aparterio esas yvene o paffora a Espona	http://www.part.cadehgia.orga.eu/hg/tocuments/caricitation.vdae	6	0
Deatherster to per	Разбері своята вмодночать в нетелитектност (ЕФ)	http://www.hattpaatf.jum/An-text.htm	0	1

Fig. 4. COsys implementation

One typical scenario of CoSys use includes the following steps:

(1) A student has to become a registered user. So, he fills the required fields on the registration form and in this way he gets access to the system;

(2) He searches for open job positions and reads the position specifications. He chooses one job and wishes to know whether his current competences are enough to become a successful employee.;

(3) The student takes a test to understand what the level of his current knowledge is. The results point how suitable for the current open position he is.;

(4) If there is a gap between the test results and job requirements then recommender system offers an

appropriate learning path to this student to achieve the needed competencies.;

(5) If the student is ready for the selected job position then the system recommends him to read basic information, additional materials and examples about CV writing and motivation letters creation. Also, the system recommends materials about interview preparation to be read.;

(6) The student can continue with job searching, repeating the steps from (2) to (5).

VIII. DISCUSSION AND CONCLUSION

In this work the development of COsys is presented as a system creating a bridge among carrier centers in universities and the industry employers.

Carrier orientation is a widely discussed topic from different stakeholders, because of its importance for the future of society. This term includes not only the made choice about the future profession, but also the further choices related to deeper specialization in a domain and lifelong learning. The aim of the career orientation is to: (1) propose more flexible support to every individual in his decision making processes among sequences of choices related to his career development and (2) ensure individual progress in personal aspect.

In the context of European politics, career development becomes an integral part of the strategy for progressing of human resources. The advantages of technical and economical changes in our society have to be used for increasing the competitiveness of our students on the labor market in the case of globalization. The qualitative orientation and self-determination of the students is one main topic from the Higher education reforms and "Bologna" process.

As it can be seen different institutions in our society are looking for highly qualified and well trained staff ready to perform specialized technical work. One step for achieving that is ensuring a communication gate between employees and employers. We assert that the presented work in this paper has the ability to support career development of students and their personal progress in lifelong learning aspect.

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Modular Package Based on MATLAB and National Instruments' DAQ for Studies of Mechanical Oscillatory Systems by Undergraduate Students in Engineering

Stoyan Zhivkov Nikolov and Emil Nikolov Dimitrov

Abstract - A software modular package is developed as an educational tool aiding undergraduate students in engineering to understand mechanical oscillations and their parameters. The package consists of three functional modules for conduction of multiple real-life experiments (via DAQs by National Instruments), simulative studies and comparative analysis of the results. Each module displays processed data both graphically and numerically and saves data to file for additional processing with MATLAB.

Keywords – Mechanical oscillations, MATLAB, 2nd order ODE, DAQ (by National Instruments), simulation, comparative analysis, education.

I. INTRODUCTION

The physical phenomena fundamental to engineering have been studied experimentally through decades and centuries. Mathematical models describing these phenomena are verified and documented. An effective education in engineering requires working knowledge of the fundamental physical principles underlying technical systems. The commonly accepted approach to facilitate such education is based on study of theory and applying it in solutions of practical engineering problems. The hidden flaw of this approach gathers significance as technical progress advances - a growing difficulty of traceability in compliance between fundamental theory and practice appears.

The contemporary technology is developed well enough to offer an elegant solution of this major educational issue. The thriving software of today combined with affordable data acquisition systems (DAQ) could provide the engineering students worldwide with powerful and flexible educational tools. High-level programming languages apply abstract theoretical models in programs with capabilities for calculation and visualization of complex mathematics. The existing DAQs combine low cost with high accuracy and sampling rate. These features have made them a tool applicable far outside the realms of industrial control and R&D. These systems have already entered university labs to provide mediation between theory and practice in education.

The modular package described in this paper utilizes similar technique – enables joint simulative and experimental studies of the principles behind one of the most common processes in engineering – oscillations. Using the modules students unravel the correlation between parameters of the equations and the ones of the physical phenomenon. Thus, a sense about the dynamics of oscillatory systems is developed. Secondary educational tasks include gathering understanding of major DAQ parameters (sampling rate, acquisition time, hardware channels, etc.) and parameters of simulation (simulation step, simulation time, amount of calculated points, etc.). These ideas are put in practice through the data acquisition solutions by National Instruments and the software environment of MATLAB.

II. STRUCTURE OF THE PACKAGE

The package consists of three software tools – a module for simulations, a module for DAQ and a module for comparative analysis. Through consecutive use of all three tools a student performs the full cycle of understanding a process – theoretical description, experimental study, comparison of results.

A DAQ by National Instruments with USB connection to PC is used to acquire experimental data. The experimental set consists of a stand, a set of springs with known values of elasticity coefficient, a set of weights with known mass. Discs with different areas made of light material are used as dampers. The oscillations are converted to electrical signals via a tensometric bridge in the stand connected to an instrumentation amplifier. Students are offered to study an oscillatory system having wide variety of parametric combinations.

Simulations are performed for a program - defined set of parameters of a dynamic mechanical system – elasticity coefficient, body mass, damping coefficient, stationary spring length, initial amplitude of the transient process. The analytical solution of the governing equation is implemented in the module for simulations. Depending on the user-defined values of the input parameters three modes are available: overdamped, critically damped, underdamped (oscillatory). The results of the calculations are displayed graphically and numerically.

S. Nikolov is with the Department of Electronics and Electronics Technologies, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: nayots@tu-sofia.bg

E Dimitrov is with the Department of Electronics and Electronics Technologies, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: edim@tu-sofia.bg

The module for comparative analysis extracts data from files generated by the previous two modules and displays all results in a single graphics. It supports two data

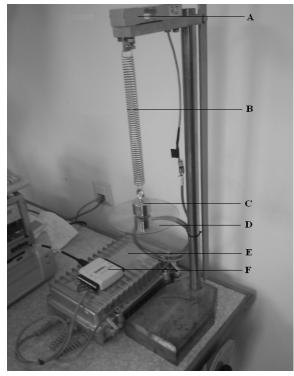


Fig. 1. Experimental set. It consists of: A) tensometric bridge, B) spring, C) mass, D) damper disc, E) instrumentation amplifier and power supply unit, F) a DAQ by National Instruments

comparison methods. The first method utilizes data from single-type files – only simulation results or only experimental ones. The second method is used in comparison of two different data types – an experiment and a simulation. Such comparison helps students analyze the compliance between these two methods of study.

III. MODULE FOR SIMULATIONS

The analytical solution of the following second order ODE is evaluated:

$$\frac{d^2x}{dt^2} + \frac{c}{m}\frac{dx}{dt} + \frac{k}{m}x = 0 \tag{1}$$

where: t-time

c - damping coefficient

- k elasticity coefficient
- m body mass

This formula is a mathematical description of a transient process. All three possible modes of its numerical evaluation are programmed in the algorithm – aperiodic, critically aperiodic, oscillatory.

User-defined values of the input parameters are used by MATLAB to calculate each amplitude point as a function of time (vector) and generate graphics of the output curve. The calculated values can be stored numerically in a file. Several secondary parameters of the transient process are calculated – Q-factor, logarithmic decrement, frequency of oscillation (if applicable). In "Process Information" field a short explanatory text about the process mode is displayed.

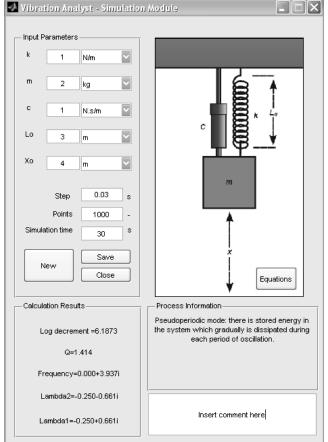


Fig. 2. Vibration Analyst – Simulation Module and data window

The module for simulations consists of a primary and an auxiliary window. The primary one is a configuration window for parameters of a mechanical system identical to the experimental. User inputs values for elasticity coefficient, body mass, damping coefficient, stationary coil length, initial amplitude. Additional input parameters configure the simulation – simulation time, calculation step, amount of points calculated. The latter three relate to one another via the equation:

$$Calculated_Points = \frac{Simulation_Time}{Calculation_Step}$$
(2)

This equation is implemented in an algorithm and is dynamically rebalanced if user changes a value. Thus, a student gathers understanding about the major simulation parameters, the connections between them and their influence over the quality and quantity of data visualization.

The "Equations" button opens an auxiliary window. It contains the mathematical description of the studied process. These are the equations implemented in the simulation algorithm of the module. They can serve as a reference at any time during program execution.

Only after each field is given a value the simulation can be started. A graphics of the calculated process curve is generated automatically in a new window at the completion of the simulation. This window contains all standard MATLAB tools for analysis of graphics. Prior to saving data to file the user is provided a field to enter their short comment on the data contents. It is incorporated automatically in the data file along with all input parameters.

IV. MODULE FOR EXPERIMENTAL STUDIES

This module is a communication program with any DAQ by National Instruments equipped with USB connection to a PC. If operating connection is detected DAQ information is extracted – device name, channel number, min. and max. sample rates supported. They are used in due course of program execution to check validity of the corresponding user-defined values for acquisition parameters. In the field to the right of the window a pinout schematic of the connected DAQ appears. Supported DAQs are NI-6008, NI-6009, NI-6210, NI-6211, NI-6212, NI-6216, NI-6218.

The user interface is organized as text boxes in dialog mode. The user has to enter values for the following parameters required by National Instruments' DAQs: sample rate, (hardware) channel, trigger type, acquisition time, samples per trigger. If a user-defined value is outside DAQ's capabilities a closest valid value automatically substitutes it. Sample rate, acquisition time and samples per trigger are connected via the formula:

An algorithm calculates and refreshes the numerical indications in case of a value change. The aim is to help a student perceive the connections between parameters of experimental data acquisition.

Acquisition start is enabled only after full parameter configuration of DAQ. A progress bar indicates elapsed time. If unwanted connection loss happens during the acquisition process a warning message is displayed and program execution is cancelled. If no errors occur acquired data is displayed as a graphics in a separate window. The window contains all standard MATLAB tools for analysis of graphics. Similarly to the previously described module here a short user comment can be incorporated in a data file. File saving marks the end of an experiment cycle.

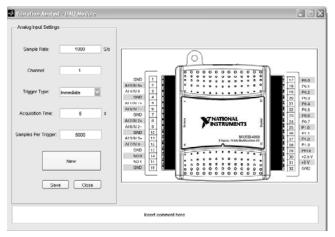


Fig. 3. Vibration Analyst - DAQ Module and data window

V. MODULE FOR COMPARATIVE ANALYSIS

This module enables a student to perform the last step of the study of a mechanical oscillatory system. Data saved to files in the modules for simulations and experimental studies can be visualized here in a single graphics and analyzed. Two modes of joint visualization are supported – for single data type and for multiple data types. The first mode allows used to open and draw a joint graphics for up to 8 data sets – from experimental files only or simulative files only. This mode enables comparative analysis of several different configurations of parameter values. Such an analysis helps a student perceive the "sensitivity" of a system towards changes in particular parameters. The joint graphical image emphasizes the differences in resonance frequency, attenuation rate, amplitudes.



Fig. 4. Vibration Analyst – Comparison Module and data window

The second mode of analysis enables comparison between two data sets of different file types - one experimental set and one simulative set. The mode is appropriate for comparative analysis of the pros and cons of the two methods for studying the same configuration.

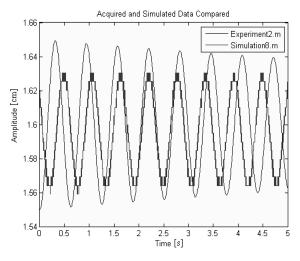


Fig. 5. Comparison of results - multitype mode

Some small differences in the curves represent real-life physical effects unaccounted for in the simulation. This depicts the accuracy degree of a simulative model and its possible inconsistencies with the physical process.

VI. CONCLUSION

The technology of today is capable of adapting complex abstract concepts and high-precision measurements for better education of engineering. The modular package described in this paper guides students through a wellstructured method of knowledge gathering. The same information is displayed in several different ways – graphically, numerically, via observation and comparison. Thus, students perceive multiple projections of a physical process. Aided by the modules they can quickly and accurately understand its principles and the connections between parameters. The package is appropriate tool for interdisciplinary education that meets the contemporary need for a thorough and working knowledge of a high professional level.

ACKNOWLEDGEMENTS

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Integration of Sensors into a Sensor Platform for a Cardiovascular Telemedicine Application

Gustavo Aragón and Harald Mathis

Abstract – In this paper we present a sensor platform, developed for ambient assisted living (AAL) for the monitoring of cardiovascular parameters. It allows the connection of three different sensors and wireless communication with a mobile end device, used for the interaction with the patient. Interconnection with a server incorporates information storage into a database and allows the posterior information analysis by a physician, who is able to send messages to the patient.

Keywords – AAL, Sensor platform, nanopotentiostate, FLORES-sensor, SPO2-sensor

I. INTRODUCTION

Ambient assisted living (AAL) has gained more importance as a research field and confronts the demographical condition of developed countries where the population tends to become elderly. Germany, for example, will have in year 2060 almost as many young people under 20 years old as people over 80 years old [1]. Moreover, problems with mobilization and control of risk factors can aggravate the problem, making AAL essential to assure a healthy and independent life to patients.

Fraunhofer FIT develops together with the Charité and T-Systems Germany new concepts for ambient assisted living for the prevention of cardiovascular diseases within the project MAS (Nanoelectronics for Mobile AAL-Systems) funded by the EU[2]. Cardiovascular diseases (CVD) constitute the cause number one of mortality globally. In 2008 30% of all global deaths were caused by CVDs [3]. In many cases person death could be avoided with an early detection of the symptoms. Moreover, for precise diagnosis more than one clinical parameter must be monitored as mentioned in the research of clinical decision support systems [4].

The objective of MAS is the integration of different miniaturized sensors for the measurement of relevant diagnostic parameters in a mobile end device. Physicians are brought close to the patients by applying telemedicine for the transmission of patient's parameters. This process requires the construction of miniaturized sensors, which should communicate wireless with the mobile end device, in order not to affect the mobility of the user. Nowadays, biometric devices do not support standardized protocols to facilitate communications. For this reason, the concept of a sensor platform overcomes the problem by creating a unique standardized platform able to communicate wireless with a mobile end device.

G. Aragón is with Fraunhofer FIT Biomos, Fraunhofer Gesellschaft, Schloß Birlinghoven 1, 53754 Sankt Augustin, Germany, e-mail: gustavo.aragon@fit.fraunhofer.de

H. Mathis is with Fraunhofer FIT Biomos, Fraunhofer Gesellschaft, Schloß Birlinghoven 1, 53754 Sankt Augustin, Germany, e-mail: harald.mathis@fit.fraunhofer.de

The telemedicine chain has been implemented and tested. Three different sensors, nanopotentiostate, FLORES sensor and SPO2 sensor have been connected to a sensor platform, which collects the data and sends the information wireless to the mobile end device. The mobile end device displays the information and sends it to a server, which can be used by the physician to analyze the information, make a diagnosis and send a message to the patient. The chain is presented in Figure 1.

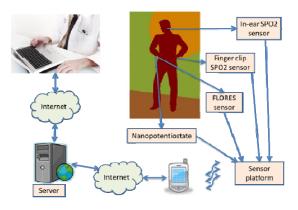


Fig. 1. Assistance system (AAL) concept

II. SENSOR PLATFORM

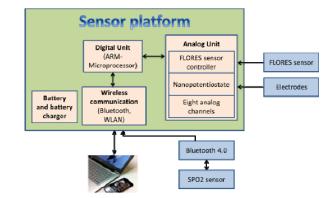


Fig. 2. Sensor platform structure

The sensor platform is an electronic unit that allows the connection of different biomedical sensors and the communication with a mobile end device. It does not only work as a data-logger, where data from the sensors are read, saved and transmitted to the mobile; but also as a sensor controller, which entirely controls the sensors developed in Fraunhofer FIT. The sensor platform is composed of a digital unit which contains the main microprocessor, an analog unit for analog data processing, Bluetooth or WLAN interfaces and a battery with its corresponding charger's electronics. Figure 2 shows the structure of the sensor platform.

The digital unit works with a central ARM microprocessor. It controls the different sensors, reads the data coming from the AD converter, processes the digital signals, controls the memory and transmits the data through Bluetooth or WLAN to the mobile end device. Algorithms for data processing and evaluation are implemented in the microprocessor, so that evaluated information is sent to the mobile end device. The functions of the mobile end device are limited to information display and communication with the server.

The analog unit implements the analog processing of signals from the different sensors. Signal digitalization is done with the AD converter ADS1298 from Texas Instruments. It enables the simultaneous conversion of eight analog channels with a frequency of 32Khz and provides a final resolution of 24 bits. As an analog voltage reference for data conversion, the ADS1298 uses a self-generated low-noise reference voltage of 4V, which establishes a voltage input in the range of -4V to 4V. However, the unit is only used with positive voltages. The communication with the microprocessor is done over an SPI interface, which allows a fast data reading and a complete programming interface of the AD converter. For this application a clock frequency of 10MHz was chosen for the SPI-Interface.

The eight inputs of the AD converter are divided into four for the FLORES sensor; one for the nanopotentiostate and three are left free for further applications. Though, it is possible to use the eight inputs of the ADS1298 for other analog signals if necessary. Every input possesses a zener diode as protection limiting the input voltage to 4V in the presence of an overvoltage, and an analog low-pass filter to eliminate the high-frequency noise.

The ground of the analog unit is separated from the ground of the digital unit using ferrite cores. To filter the supply voltage, a π -filter was constructed. In order to isolate signals coming from or going to the microprocessor, digital isolators ADUM140x from Analog Devices were incorporated in the circuit. They combine high-speed CMOS and monolithic air core transformer technology. Ground separation was used to overcome noise problems due to high clock frequency at the digital unit. Other noise problems were undertaken by a correct positioning of the different electronic components and by the design of a four layer electronic card.

For the communication with the mobile end device, an external Bluetooth 2.1 module from Stollman was used. A serial interface enables the communication with the central microprocessor. It can be used for data reception and transmission, and to program the module. The communication with the microcontroller uses a baud rate of 921600 baud. After the initial programming of the module, the settings remain saved in the internal memory. An integrated antenna allows coverage range up to 60m in open air. As we do not use the whole transmission power, the coverage range is reduced to about 10m. As profile was chosen a Serial Port Profile (SPP), which facilitates the integration of the software in the mobile end device.

Due to mobility reasons and flexibility in the use of the platform, a Li-Po battery was integrated with a battery charger BQ24103 from Texas Instruments for an in-case recharging. The charger displays the charging state through

LEDs. It applies a fast recharging cycle with high current of approximately 1.2A in the start phase and reduces the current to the minimal value in dependence of the voltage value reached by the cells.

The units of the sensor platform were placed into an aluminum case for protection of the user and of the electronic parts. Figure 3 shows the physical sensor platform.



Fig. 3. Housing of the sensor platform

III. SENSORS

So far, three sensors have been integrated into the platform: the nanopotentiostate for electrochemical measurements; the FLORES sensor for fluorescent-based detections and an SPO2 sensor for the detection of oxygen saturation in blood, for pulse measurement, and for recording the plethysmogram (PPG) signal.

However, the connection of more than three sensors to the sensor platform is possible due to the eight analog inputs of the AD converter.

A. Nanopotentiostate

The nanopotentiostate is an electrochemical sensor developed by Fraunhofer IMS[5] that converts biochemical information from an analyte into current response. Using this principle, measurements of glucose, lactate, cholesterol and other biomarkers are possible by immobilizing enzymes sensitive to each biomarker[6]. Figure 4 shows the nanopotentiostate as an ASIC and inserted in housing. The housing is a TQFP-32 case, which provides flexibility to solder it to the analog unit.

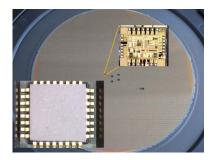


Fig. 4. Nanopotentiostat ASIC and in a TQFP-32 case

Electrochemical processes take place at the electrodesolution interface. Therefore, a three-electrode configuration must be used for the measurements with the nanopotentiostate. The three electrodes are: working electrode (WE), counter electrode (CE) and reference electrode (RE). The working principle [5] of the nanopotentiostate is shown in figure 5.

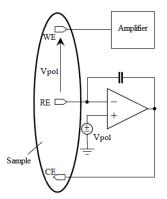


Fig. 5. Nanopotentiostate working principle [5]

The nanopotentiostate controls a polarization voltage between the RE and the WE in a close loop. The controller feeds in a current to the system through the CE, while measuring the inducted current at the WE. Due to the high impedance of RE, in the range of **10MO**, no current flows through this electrode. The measured current at WE is proportional to the concentration of analyte in the sample, in this case of the selected biomarker. Figure 6 shows cyclic voltammograms taken with the nanopotentiostate.

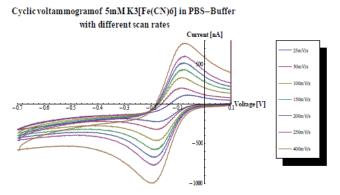


Fig. 6. Cyclic voltammograms of potassium ferricyanide with different scan rates

B. FLORES sensor

FLORES sensor is a sensor that measures fluorescence intensity irradiated by a biomarker. It consists of a laser diode as source of light for fluorescence excitation, four photodiodes for the conversion of visible light into current, an optical filter, and a transimpedance amplifier. Figure 7 shows the FLORES sensor. Recently, efforts to miniaturize fluorescence sensors [7] are increasing, due to the benefits and specificity of fluorescence detection.

The laser diode focuses its light beam into a microfluidics channel in order to excitate particles labeled with fluorescent colorant. The particles emmit visible light with a longer wavelenght than the absorbed light and, therefore, lower energy. The emmited light goes through the optical filter and reaches the photodiodes, which convert its intensity into a current signal. The signal is then amplified by the transimpedance amplifier and sent to the ADS1298 in the sensor platform. Signals for the laserdiode

and for the control and amplification of the current signal from the photodiode come from the sensor platform.

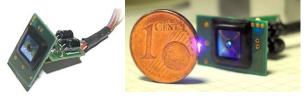


Fig. 7. FLORES sensor

Figure 8 shows a comparison between measurements of Qdots with the FLORES sensor and the Tecan reader.

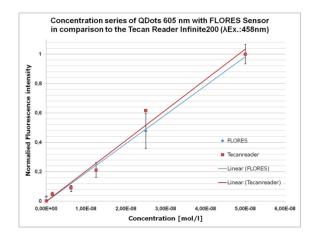


Fig. 8. Measurement of Qdots with the FLORES sensor and the tecan reader

C. SPO2 sensor

Two kinds of SPO2 sensors were tested and integrated into the sensor platform. One is a common on-finger SPO2 sensor, for which a sensor controller from Corscience is used. The other one is a new in-ear SPO2 sensor acquired from CIS Forschungsinstitut für Mikrosensorik und Photovoltaik. The further electronic design was accomplished by Fraunhofer FIT and differs from this presented in [8] in the integrated Bluetooth communication and the oriented battery design.

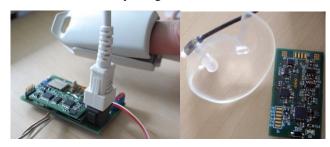


Fig. 9. Finger clip and in-ear SPO2 sensor

Both designs work with Bluetooth Low Power 4.0 and are supplied by a coin battery. They allow the measurement not only of the oxygen saturation in blood, but also of pulse rate and PPG of a person. The first design with the Corscience module and the second design with the in-ear sensor are shown in figure 9. Both sensors are equipped with two LEDs, which irradiate light in two different wavelengths, one in the red and the other in the near infrared region. Moreover, an integrated photodiode measures the light reflected in the finger or in the auditory canal depending on the sensor. The relation between these two signals corresponds to the oxygen saturation. The frequency of the signal corresponds to the pulse and the signal constitutes the PPG.

IV. CELLPHONE APPLICATION

For information display from the sensors connected to the sensor platform, an application for android operating system was developed and programmed on a Samsung S4 smartphone (see Figure 10). In contrast to other research projects [4] [9], the application collects data not only from one sensor but from the three connected to the sensor platform and sends the information to the server. A communication protocol is integrated to facilitate the interconnection of more sensors in the future.



Fig. 10. Screenshot of the android application

The application opens a communication channel with the sensor platform through Bluetooth 2.1. Bluetooth communication ensures safe data transmission, due to its limited coverage range of 10m. At the application start, the user chooses a sensor to be displayed, which triggers the reception and transmission of data from the sensor. For the nanopotentiostate, the application shows a cyclic voltammogram used for studying the kinetics of the electrochemical reactions and for the determination of the concentration of different analytes. For the FLORES-Sensor, four signals corresponding to the four photodiodes are continuously displayed on the screen. For the SPO2-Sensor, the PPG-Signal, the oxygen saturation and the pulse are displayed.

For an enhanced communication between the sensor platform and the mobile end device, a communication protocol has been developed and implemented. The protocol establishes a well-defined data communication that permits a fast implementation of the software in both sides of the chain: mobile interfaces and sensor platform. In this way, selecting another sensor ID incorporates and defines the use of other sensors, which can be controlled by the software with the same commands.

Important in this app is the capability to communicate with an external server developed by T-Systems Germany. Information collected from the sensor platform is saved in the internal memory of the mobile end device, while it does not communicate with the server. As soon as the communication channel is open, the information is sent to the server. The server saves the information in a database, where patient information is classified for further analysis by a physician.

T-Systems Germany developed a GUI for the physician side. Physicians are able to see information coming from different patients, to analyze it and to send a message to the patient if necessary. Physicians find two possibilities for analyzing information, real-time analysis and analysis of information saved in a historical file.

V. CONCLUSIONS

A chain for mobile assisted living system for cardiovascular diseases have been implemented and tested by Fraunhofer FIT together with the Charité and T-Systems Germany. Three sensors were integrated into a sensor nanopotentiostate for electrochemical platform. а measurements, a FLORES sensor for fluorescent measurements, and an SPO2 sensor for oxygen saturation measurements. The sensor platform communicates with a mobile end device through Bluetooth 2.1., which displays sensor information. The information is sent to a central server to be saved in a database, from which it can be reached by a GUI and accessed by a physician for further analysis and communication with the patient.

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FPGA TV Adaptive Positioning System

Rosen Petrov Spirov, Petko Nikolaev Tzanov and Neli Stanislavova Grancharova

Abstract – The paper presents a system for precise positioning with stepper motors TV tracking system based on FPGA Altera DE2 board.

Keywords -Image Processing, FPGA, PowerElectronics, TV.

I. INTRODUCTION

The development of television monitoring system is topical themes, providing opportunities to identify the parameters of the relative motion of an object to TV system. In systems with mechanical tracking, the center of the screen TV system following object by turning the TV camera. Positioning can be realized by driving stepper motors, as in fig.1.

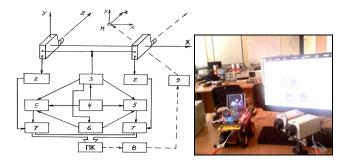


Fig. 1. TV automatic system

Where: 1 - TV camera

- 2 Block forming signal
- 3 Sinhrogenerator
- 4- Discrete oscillator
- 5 -Address counters
- 6 Control unit
- 7 Bblock of registration
- 8 Control unit
- 9 Driving device
- 10 M observed object
- PK Personal Computer.

Project used FPGA integrated driving structure with board Altera DE2 [1]. GPIO outputs controlled by impulses IC drivers, switching power supply circuits of stepper motors.

The camera's analog image information is converted into an ITU656 standard digital stream on the DE2 development board. This stream is used in three ways:

R. Spirov is with the Faculty of Electronic, Technical University - Varna, 1 Studentska str., 9010 Varna, Bulgaria, e-mail: rosexel@abv.bg

P. Tzanov is with the Department of Electronics and Microelectronics, Faculty of Electronics, Technical University -Varna, 1 Studentska str, 9010 Varna, Bulgaria, e-mail: pepitas@dir.bg

N.Grancharova is with the Department of Social science, Faculty of Electronics, Technical University - Varna, 1 Studentska str, 9010 Varna, Bulgaria, e-mail:nelly2000@abv.bg • It controls the auto-tracking camera's left, right, up, and down operation.

• It provides a vision sharing system and JPEG compression of the wireless transfers.

• It provides the in-vehicle display.

This image capture module preprocesses the image by modifying the image size, removing interlacing mode, and calculating the frame buffer memory address.

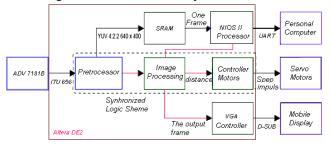


Fig. 2. The capture module processes the image

To acquire the distance between the target and the launcher, visual information is needed for the computation of the positions [2]. A camera with NTSC output is connected to the video input of the DE2 port. The data stream is processed through the ADV7181 video decoder chip on the board. The ADV7181 operates on a 27MHz clock and produces an 8-bit output encoded in ITU656 standard (YUV 4:2:2). Originally modules were to be designed to process this output and convert it to RGB color space. However, due to the difference in the refresh rate of the NTSC and VGA, synchronization of the components causes many problems. Three modules from the Altera DE2 TV demonstration files are ported for the purpose of data conversion and synchronization of the video input and the VGA display. The ITU656 decoder module converts this 8-bit input into three 8-bit signals for Y, Cb and Cr -YUV 4:4:4 standard, which provide the brightness Y and chrominance Cb and Cr, information of the pixel. The 24bit output is fed to the YUV2RGB module that translates the data from YUV to RGB color space. This data output is then supplied to a line buffer module that allows writing to one line and reading from the other for the VGA display. Module XY detector also takes the output from the line buffer and the video interface module that supplies the x and y positions of the pixel to determine the laser point coordinates.

In Fig.3 is given an overview of all hardware components in our system, which are all hooked up to the Avalon bus.

Our system works as following: a video camera is connected to the Altera DE2 and sends NTSC analog signals to the board. An Analog Devices ADV7181 converts analog video signals from a camera to digital signals in YUV format.

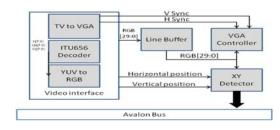


Fig.3. The video interface and Avalon bus

The converter has an I^2C interface, which allows for the output format and other parameters to be configured. The ADV7181 decoder controller takes digital video input from the ADV each pixel from YUV to 16-bit RGB. A double line buffer in the FPGA's block RAM is used used for data transfer between the 27 MHz frequency domain of the video controller and the 50 MHz frequency domain of the Avalon bus [2]. Each line of the image data is sent to a buffer in the SDRAM using DMA controller. The Nios II then performs processing on the buffer in SDRAM in order to find the center of the object we are tracking and to mark up the image.

II. THE IMAGE PROCESSING

Figure 4 shows the software structure of the system. The software polls the status of the ADV7181 controller until it encounters the beginning of a frame of video in the correct field. It then transfers a line of video at a time, using the DMA controller, to a buffer in SDRAM.

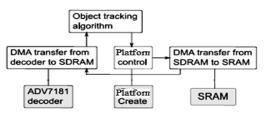


Fig. 4. The software design

For each line, it waits for the proper horizontal clock in order to copy the line at the appropriate time. By changing the number of lines copied and the number of bytes to copy from the line buffer to the SDRAM for each line, the resolution of the image can be tuned; currently it is set to 320x200. Only the first field of video is copied, since it already contains every alternating line and only 200 out of every 484 lines of video are needed.

After copying the frame of video to the buffer, the object tracking algorithm is used to find the center of the object. The details of the tracking algorithm are described in the next section. The center of the object is then marked up with a crosshair, and the UART is used to move the robot either left or right, with the speed of the robot increasing with increasing distance from the object center to the center of the frame. Finally, the marked-up image is copied using the DMA controller to the SRAM buffer in the VGA controller. Due to the limitations of the Nios II and timing constraints imposed by real-time video display, we use a very simple object tracking algorithm, which only works under certain assumptions:

• The object has a pre-defined color

- The object has regular shape
- Background is simple and has a much different color than the target object

For each input frame, first divided the whole frame into small blocks - 16x 16 in final implementation. Then we calculate how many pixels have the color of the target object, which is the color the center of the object we get from last frame [3].

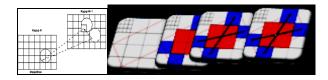


Fig. 5. The algorithm

For the first frame, simply use the center of the screen as the object center. To decide whether a pixel has the same color as the object, we separately compare each pixel's R,G, and B with the target's value within a predefined threshold. Afterwards, we judge if this block belongs to the target object based on if the majority of its pixels are of the same color as the object. This is done for every block and so to know which blocks belong to the object. After that it average the positions of the highest, lowest, leftmost and rightmost blocks to calculate the center of the object [4].

The center value is saved and used for finding blocks of the object in next frame. By processing the image block by block, we reduce the number of membership decisions from one pixel a time to one block a time.



Fig. 6. The camera's field of view

This technique also has a reasonable ability to tolerate noise in the image. However, due to the Nios II's limited computational power, we cannot do multiplication for each pixel in each frame as fast as we need. Thus, we turn every possible integer multiplication into integer shifts and additions, as shown in RTL design on fig.7.

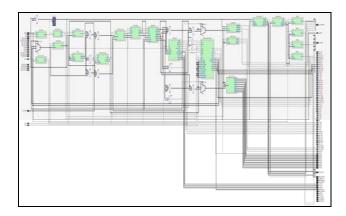


Fig. 7. The RTL QuartusII design of TV system

III. POSITIONING BLOCK

For half-stepping or full-stepping a stepping motor, the control system is at its simplest. For two-winding motors, the machine is either a four-state or eight-state machine with four or eight outputs per motor. UPDOWNcounter increments or decrements state if forward is '1' or '0' respectively. The rate at which state is changed depends on the values of speed and the frequency of the system's base clock. MotorOutput converts the variable state to relevant control bits tied directly to the transistors of Fig.8.

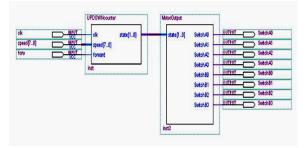


Fig. 8. The stepping motor velocity control unit.

For velocity control, an up/down variable frequency counter is necessary. For position control, the state variable can be conveniently expanded beyond the four or eight necessary steps (which conveniently correspond to the first two or three bits of any binary number) for a more expansive image of the motor's current position.

The actual velocity safely increments and decrements based on what the intended velocity is [5]. Notice that the slope is different for increasing and decreasing speed; this corresponds to differences in acceleration and deceleration capable of a motor as in:

```
PROCESS (clk)
VARIABLE t :INTEGER RANGE 0 TO 2097151:= 0;
CONSTANT accel :INTEGER RANGE 0 TO 2097151:= 390625;
CONSTANT decel :INTEGER RANGE 0 TO 2097151:= 195312;
BEGIN
IF (clk'EVENT AND clk = '1') THEN
t := t + 1;
IF(t > accel) THEN
IF (vactual < vintended AND vactual > 0) THEN
vactual <= vactual + 1;</pre>
t:=0;
ELSIF (vactual > vintended AND vactual < 0) THEN
vactual \le vactual - 1;
t := 0:
END IF:
END IF;
IF(t > decel) THEN
IF (vactual < vintended AND vactual < 0) THEN
vactual \le vactual + 1;
t - 0
ELSIF (vactual > vintended AND vactual > 0) THEN
vactual \leq vactual - 1:
t:=0:
END IF;
END IF:
END IF;
END PROCESS;
```

Typically this code segment can be simplified by assuming acceleration and deceleration rates of the motor are identical. One way to get an adaptive acceleration position control is to simply create an intended velocity vs. position profile curve for the actual velocity to approach that is dependent on the deceleration intended. Ignoring constants of integration and using basic time equations for acceleration, velocity, and position, we can arrive at the following:

$$a = k, v = kt, p = \frac{kt^2}{2}$$
(3)

$$\mathbf{v} = \pm \sqrt{2kp} \tag{4}$$

Using common sense gives the following relation for intended velocity and Δp where Δp is intended position – current position.

A more common way to move from one position to another is to calculate the time to stall between steps using motor position data and the motor's intended final position. If a simple point to point control system is desired and it is assumed that the motor will remain busy and stop before new instructions are followed the simple approximate equation can be used:

$$\Delta t = \frac{\Delta x}{s}$$
(5)

 Δt is the time needed to wait between steps, Δx is a constant equal to how much the motor moves per state change, and s, speed, can be calculated as follows where Δp is intended position – current position and Δn is initial position – current position:

$$s = MinimumOf \begin{cases} \sqrt{2k_{Accd}\Delta n} \\ s_{Accd}\Delta n \\ \sqrt{2k_{Cand}\Delta p} \end{cases}$$
(6)

A counter can be built that waits the amount of time necessary and steps accordingly in the direction towards the intended position. Also, care should be taken so that Δn is offset slightly so that it is never zero. For purely open loop motor control, pulse width modulation (PWM) is a great means of varying time average current through the motor windings. The frequency at which the counter resets is the primary PWM frequency while the frequency at which it increments is the base frequency. The primary frequency should be limited to somewhere between 10KHz and 30KHz. Lower frequencies are a source of audible noise. Higher frequencies cause the external driver to become progressively less power efficient and can cause a lot of relevant electromagnetic interference. The base frequency should be equal to the primary PWM frequency * resolution of the pulse width. This frequency may not be fast enough to match the stepping of states through the sinusoid, but at such high frequencies the advantages of switching to fullstepping the motor should be considered. The output of the counter serves as an input to the second additional element: a comparator set. This controls switching based on whether the PWM value is greater than or less than another input value.

Another logic element is a sinusoid function or lookup table. For this application, a lookup table saves time, processing power, and possible chip space for low resolutions that are more than adequate for micro-stepping motor control. The input resolution determines how many states there are per sinusoid and the output resolution is the same as the resolution of the pulse width. This element's output is a sinusoidal value for the comparator element. To improve accuracy of the motor's micro-stepping, this sinusoid table may be altered to compensate for the imperfections in the torque vs. rotational position curve for the motor. In the following equation where n is an integer from 0 to *StatesPerSinusoid-1*, *K* is some real number typically less than one that can be altered until the curve provides sufficient accuracy for the controller. This technique is a quick fix and is not guaranteed to always work but can usually provide improvement noticeable by the naked eye at low stepping frequencies.

resolution_{punc}
$$\left| \cos \left(\frac{2\pi}{\text{StatessPerSinusoid} - 1} n \right) \right|^{\kappa}$$
 (7)

The previous up/down counter can still be used, but the constant dividend must be recalculated as there are now more than four or eight states to cycle through.

Accompanying this application note are two identically coded VHDL examples for acceleration compensated dynamic position uni-polar motor control system. The first folder contains an entire Quartus project built for the ALTERA DE2 board, as in fig.9.

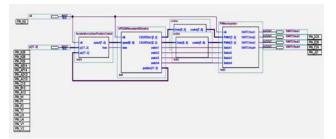


Fig. 9. A schematic representation design.

The second folder only contains the individual text files of component and package VHDL code [5]. The code was built to control a 100 step per revolution two winding bipolar motor via 64 states per step micro-stepping. The control system limits the motor to run at a maximum of four revolutions per second in either direction. The motor is also limited to accelerate at two revolutions per second² and limited to decelerate at four revolutions per second². The sinusoid table has been simplified assuming symmetry and distorted to match the motor using K = 0.7 in equation (7).With ALTERA's DE2 board, the pin assignments correspond to the switch array for pi (position intended), the 50 MHz clock for clk, and the first four pins on the left side of the first general IO header for the motor switches and shematic on fig.10.

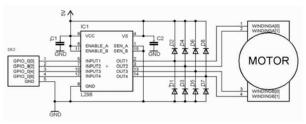


Fig. 10. Schematic of motor drive circuit

Any PLD can be used, but the PLD the system was designed with is the Cyclone II EP2C35F672C6N on the ALTERA DE2 board which utilizes a 50 MHz clock.

Certain constants must be changed if a different base frequency signal is used so the equations in this application note are repeated in comments within the code. The 18 bit positional input data is provided by the simple bitwise representation of the 18 switch array on the DE2 board so another means of delivering an 18 bit binary number to the PLD will be required if the DE2 board is not used.



Fig. 11.The TV positioning system

IV. CONCLUSION

Object detection and tracking has been an active research area for a long time because it is the initial important step in many different applications, such as video surveillance, face recognition, image enhancement, video coding, and energy conservation.

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Computer-Aided Test Set Selection in Analog Circuit Diagnosis

Elissaveta Dimitrova Gadjeva, Ekaterina Nikolova Dimitrova and Dimitar Yordanov Shikalanov

Abstract – An approach is developed to optimal test node set and optimal test characteristics selection in analog circuit diagnosis. The possibilities for statistical simulation of the general-purpose circuit simulators such as *PSpice* are applied to construct and analyze models of faulty circuits introducing multiple parametric faults and to investigate the fault coverage.

Keywords – Fault Diagnosis, Optimal Test Set, Fault Coverage, Monte Carlo Simulation

I. INTRODUCTION

The lack of fault models and accessibility to internal nodes complicate the analog circuit testing and diagnosis. In addition, it is necessary to take into account the influence of design and process tolerances. The variety of response parameters of analog circuits makes analog circuit testing difficult and expensive. A number of approaches are proposed to select the optimal set of test nodes and test characteristics in order to increase the fault coverage [1-5]. In [1] a fault-based technique is developed based on hierarchical fault models for parametric and catastrophic faults, to determine automatically the test frequencies and detect AC faults in linear analog circuits. In [2] a parametric fault diagnosis approach to analog/RF circuits is proposed. Using sensitivity investigation, the optimal test set is selected to distinguish the faults and to increase the diagnostic resolution. In [3] a method is developed for improving fault detection in high frequency circuits based on sensitivity analysis and S-parameter measurements. The test frequencies are selected maximizing the sensitivity of the magnitude and phase of the S-parameters. An algorithm is presented in [4] that reduces functional test sets to only those that are sufficient to find out whether a circuit contains a parametric fault.

The possibilities of the general-purpose circuit analysis programs such as *Cadence PSpice* allow to construct and analyze models of faulty circuits introducing multiple parametric and catastrophic faults. Based on statistical simulation and fault coverage investigation, the optimal test node set and optimal test characteristics can be obtained.

E. Gadjeva is with the Department of Electronics and Electronic Technologies, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: egadjeva@tu-sofia.bg

E. Dimitrova is with the Department of Electronics, Faculty of Electronic Engineering and Technologies, Technical University of Varna, 1 Studentska Str., 9010 Varna, Bulgaria e-mail: edimitrowa@yahoo.com

D. Shikalanov is with the Department of Informatics, New Bulgarian University, Montevideo 21 Str., 1635 Sofia, Bulgaria, e-mail: dys@nbu.bg

II. MODELING OF PARAMETRIC FAULTS

The standard circuit *PSpice*-like simulators allow to build user-defined statistical distributions using .DISTRIBUTION statement. Statistical modeling can be used for the simulation of faults in circuit elements. Deviations of $\pm 20\%$ and $\pm 50\%$ for the passive elements are automatically generated. In addition, the design and process tolerances are also introduced in the distribution with probability *P* (Fig.1).

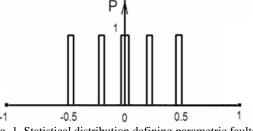


Fig. 1. Statistical distribution defining parametric faults

The description of the user-defined distribution has the form:

for resistor element with 1% design tolerance:

.Distribution Distr_R (-1,0) (-0.5,0) (-0.5,1) (-0.45,1) (-0.45,0) (-0.2,0) (-0.2,1) (-0.15,1) (-0.15,0) (-0.01,0) (-0.01,1) (0.01,1) (0.01,0) (0.15,0) (0.15,1) (0.2,1) (0.2,0) (0.45,0) (0.45,1) (0.5,1) (0.5,0)

for capacitor element with 5% design tolerance:

.Distribution Distr_C (-1,0) (-0.5,0) (-0.5,1) (-0.45,1) (-0.45,0) (-0.2,0) (-0.2,1) (-0.15,1) (-0.15,0) (-0.05,0) (-0.05,1) (0.05,1) (0.05,0) (0.15,0) (0.15,1) (0.2,1) (0.2,0) (0.45,0) (0.45,1) (0.5,1) (0.5,0)

The computer model of the faulty resistor for parametric fault generation is presented in Fig. 2 [5].

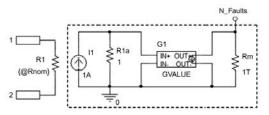


Fig. 2. Computer model of the faulty resistor for parametric fault generation

 R_1 models the resistor element of nominal value {@Rnom}. R_1 and R_{1a} are defined by correlated statistical distribution. The models from the library BREAKOUT.LIB are applied for the fault generation. They are described in the form:

.model RGR RES R=1 LOT/Distr_R 100%

The VCCS G1 is defined in the form:

{-IF((ABS(V(%IN+, %IN-)-1)>0.01),1,0)}

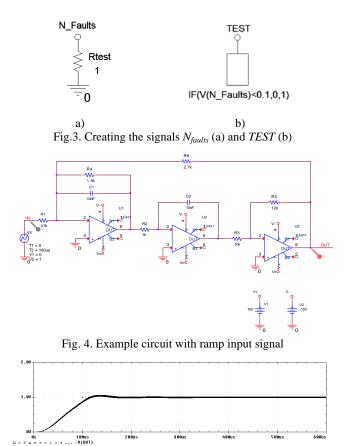


Fig. 5. The output voltage $-V_{out}(t)$ of the circuit with design tolerances

In this way, the current $I_{G1} = 1$ A if the deviation is outside the design tolerance limits (the value of R_1 is faulty), otherwise $I_{G1} = 0$ (the value of R_1 is correct).

The resistor R_{test} is connected between the global node N_Fault and the reference node in the main circuit [5] (Fig. 3a). As a result the voltage V(N_Fault) is equal to the multiplicity of the fault [5]. The voltage of the node TEST V(TEST) = 1 if the simulated variant corresponds to a faulty circuit, and V(TEST) = 0 if the circuit is correct (Fig. 3b).

III. TEST SET SELECTION USING SIMULATION IN THE TIME DOMAIN WITH RAMP INPUT SIGNAL

The example circuit shown in Fig. 4 is used to illustrate the proposed approach. A ramp input signal is applied to the input node. It is modeled by independent voltage source with piece-wise linear approximation of VPWL type. The corresponding parameters are: T1 = 0. V1 = 0, T2 = 100 μ s, V2 = 1V. The output signal of the circuit with design tolerances is obtained using *Monte Carlo* simulation (Fig. 5). The following characteristics of the circuit response are monitored [6]:

- 1. Steady state voltage V_{st}: ST;
- 2. Overshoot: OV;

$$OV = \frac{V_{\max} - V_{st}}{V_{st}} .100 \,[\%]$$
(1)

3. Rise time *TR*;

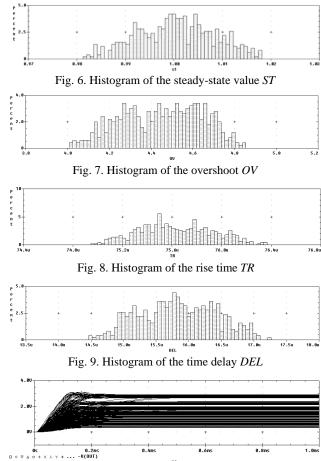


Fig. 10. The output voltage –V(out) of the circuit with generated parametric faults

These secondary characteristics can be calculated in the graphical analyzer *Probe* using the available functions included in *Probe* defined as macros:

ST = max(rms(-V(OUT))) OV = Overshoot(-V(OUT)) TR = Risetime_StepResponse(-V(out)) D_I = XatNthY(V(IN),0.5,1) DIFF = 0.5*max(AVGX(-V(out),1ms))+V(out) D_O = XatNthY(Diff,0,1)

In order to obtain the non-faulty limits of the secondary characteristics, a *Monte-Carlo* simulation is performed. The design tolerances with uniform distribution of the parameters are defined for the circuit elements. The non-faulty limits of these characteristics $[ST_{\min}, ST_{\max}]$, $[OV_{\min}, OV_{\max}]$, $[TR_{\min}, TR_{\max}]$ and $[DEL_{\min}, DEL_{\max}]$ are obtained from the corresponding histograms shown in Fig. 6, Fig. 7, Fig. 8 and Fig. 9 correspondingly.

In order to simulate the faults, a *Monte Carlo* simulation is performed and parametric faults are generated using the distribution shown in Fig. 1. The voltage $-v_{out}(t)$ of the circuit with generated parametric faults is shown in Fig. 10.

The parameter M_{tst} is calculated for the monitored parameter M in the following way:

$$M_{ist} = \begin{cases} 0 \text{ if } M_{\min} \le M \le M_{\max} \\ 1 \text{ otherwise} \end{cases}$$
(2)

^{4.} Time delay DEL.

The histogram of M_{tst} gives the percentage of recognized faults with respect to all modeled variants $(M_{tst} = 1)$. Monitoring the parameters *ST*, *OV*, *TR* and *DEL*, the histograms of ST_{tst} , OV_{tst} , TR_{tst} and DEL_{tst} are obtained using the following macros in *Probe*:

 $ST_tst = 1-0.5^*(sgn(ST-STmin)+1)+0.5^*(sgn(ST-STmax)+1)$ $OV_tst = 1-0.5^*(sgn(OV-OVmin)+1)+0.5^*(sgn(OV-Vmax)+1)$ $TR_tst = 1-0.5^*(sgn(TR-TRmin)+1)+0.5^*(sgn(TR-Rmax)+1)$ $DEL_tst = 1-0.5^*(sgn(DEL-DELmin)+1)+$

0.5*(sgn(DEL-DELmax)+1)

Finally, the parameter *TST* is calculated in the following way:

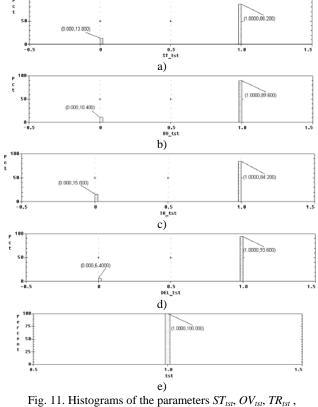
 $TST_i = 1$ if a fault is recognized using all monitored parameters for the *i*-th *Monte Carlo* run.

 $TST_i = 0$ if a fault is not recognized using all monitored parameters for the *i*-th *Monte Carlo* run or if the circuit is correct.

The following macros in *Probe* are used to calculate *TST*: ALL_TST = ST_tst +OV_tst+TR_tst+DEL_tst

 $TST = 0.5^{*}(sgn(ALL_TST-0.5)+1)$

The histograms of ST_{tst} , OV_{tst} , TR_{tst} and DEL_{tst} are presented in Fig. 11a, Fig. 11b, Fig. 11c and Fig. 11d correspondingly. The percentage of recognized faults by monitoring the steady state voltage V_{st} is 86.2%, the overshoot OV: 89.6%, the rise time TR: 84.2% and by time delay DEL 93.6%. The percentage of recognized faults by monitoring all parameters is obtained from the histogram of TST for TST=1. For the considered example it is 100% (Fig.11e).



g. 11. Histograms of the parameters SI_{tst} , OV_{tst} , IR_{tst} DEL_{tst} and TST

In order to obtain the number of generated correct and faulty variants, the histogram of the signal MAX(V(TEST)) is built. The variants with MAX(V(TEST)) = 1 correspond to faulty circuits and the variants with MAX(V(TEST))=0

correspond to correct circuits. For the considered example, applying the statistical distribution shown in Fig. 1, all modeled variants correspond to faulty circuits. The histograms in Fig. 11 can be used for the fault coverage calculation using each of the monitored parameters.

$$F_C = 100 \cdot \frac{N_R}{N_F} [\%], \qquad (3)$$

where N_R is the number of recognized faults;

 N_F –the total number of the modeled faults.

The test set of the monitored parameters can be investigated using the proposed approach. If the subset *ST*, *TR* and *DEL* of monitored parameters is included in the tested group, 100% of the variants in the histogram of *TST* are characterized by TST = 1 (recognized faults). In this way, the optimal test set can be selected, which is characterized by maximal fault coverage F_C .

IV. TEST SET SELECTION USING SIMULATION IN THE TIME DOMAIN WITH PERIODIC INPUT SIGNAL

The example circuit shown in Fig. 4 is used to illustrate the approach. A periodic input signal is applied to the input node. It is modeled by pulse voltage source of VPULSE type. The corresponding parameters are: low voltage level $V_1 = 0$, high voltage level $V_2 = 1$ V, time delay $T_D = 0$, rise time $T_R = 50\mu$ s, fall time $T_F = 50\mu$ s, pulse width $P_W = 150\mu$ s and period *PER* = 500 μ s. The output signal of the circuit with design tolerances, obtained by *Monte Carlo* simulation, is shown in Fig. 12.

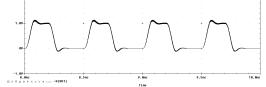


Fig. 12. The output voltage -Vout(*t*) of the circuit with design tolerances

The corresponding amplitudes V_{out1} , V_{out2} and V_{out3} of the first, second and third harmonic of the circuit response are monitored. The test parameters $V_{out1,tst}$, $V_{out2,tst}$ and $V_{out3,tst}$ are calculated according to (2) for the monitored parameters V_{out1} , V_{out2} and V_{out3} . In order to create the histograms of the selected test parameters, it is necessary to obtain the waveforms of the harmonics $v_{out1}(t)$, $v_{out2}(t)$ and $v_{out3}(t)$. This is realized by connecting to the output node three band-pass filters with center frequencies equal to the first, second and third harmonic (Fig. 13). The waveforms of the harmonics $v_{out1}(t)$, $v_{out2}(t)$ and $v_{out3}(t)$ are obtained at the corresponding nodes OUT1, OUT2 and OUT3. Monitoring the parameters V_{out1} , V_{out2} and V_{out3} , the histograms of $V_{out1,tst}$, $V_{out2,tst}$ and $V_{out3,tst}$ are obtained using the following macros in *Probe*:

VO1_tst = 1-0.5*(sgn(MAX(V(OUT1))-VO1min)+1)+ 0.5* (sgn(MAX(V(OUT1))-VO1max)+1)

VO2_tst = 1-0.5*(sgn(MAX(V(OUT2))-VO2min)+1)+ 0.5*(sgn(MAX(V(OUT2))-VO2max)+1)

VO3_tst = 1-0.5*(sgn(MAX(V(OUT3))-VO3min)+1)+ 0.5*(sgn(MAX(V(OUT3))-VO3max)+1)

ALL_Vtst = VO1_tst + VO2_tst + VO3_tst

 $TST = 0.5^{*}(sgn(ALL_Vtst-0.5)+1)$

A Monte Carlo simulation is performed and parametric faults are generated using the distribution shown in Fig. 1.

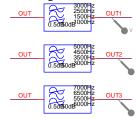


Fig. 13. Band-pass filters for obtaining the harmonics $V_{out1}(t),\,V_{out2}(t)$ and $V_{out3}(t)$

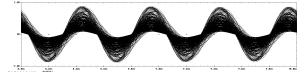


Fig. 14. First harmonic V_{out1}(t) of the circuit with generated parametric faults

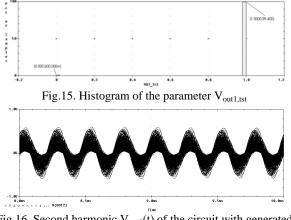


Fig.16. Second harmonic V_{out2}(t) of the circuit with generated parametric faults

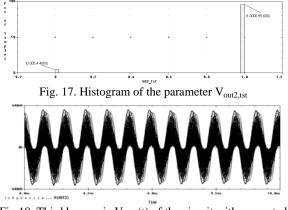
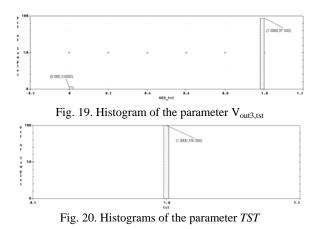


Fig.18. Third harmonic V_{out3}(t) of the circuit with generated parametric faults

A *Monte Carlo* simulation is performed and parametric faults are generated using the distribution shown in Fig. 1. The voltages $v_{outi}(t)$ and the histograms $V_{outi,tst}$, i = 1, 2, 3 of the first, second and third harmonics are shown in Fig. 14 - Fig. 19 correspondingly. The test set of monitored parameters can be investigated in order to optimize the set of these parameters and to select optimal test subset, which is characterized by maximal fault coverage F_C . For the considered case 99.4% of the modeled variants are recognized by the first harmonic, 95.6% - by the second harmonic and 97% - by the third harmonic.



Monitoring $V_{out1,tst}$, $V_{out2,tst}$ and $V_{out3,tst}$, all monitored faults are recognized (TST = 1), as shown in Fig. 20. If the subset V_{out1} and V_{out3} of the monitored parameters is included in the tested group, 100% of the variants in the histogram of TST are characterized by TST = 1 (recognized faults). The subset V_{out1} and V_{out2} also ensures 100% fault coverage. In this way, the optimal test characteristics can be selected.

V. CONCLUSION

An approach has been developed to optimal test node set and optimal test characteristics selection in analog circuit diagnosis. The test parameter set is defined and investigated based on time-domain characteristics. Two basic approaches are applied – using ramp input signal and using pulse input signal. Macro-definitions are constructed for determination the test parameters and the percentage of recognized faults. Examples are presented for obtaining optimal test sets.

ACKNOWLEDGEMENT

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Investigation of Commutation Processes of Current Fed Inverter Using PSpice

Georgi Tzvetanov Kunov, Georgi Hristov Gigov and Elissaveta Dimitrova Gadjeva

Abstract – The commutation processes in bridge current fed transistor inverter are investigated in the present paper. The three possible modes of operation of the inverter are considered: the mode when the transistor commutation frequency is equal to the resonance frequency of the parallel load resonant circuit; the mode of inductance detuning and the mode of capacitance detuning. The influence on the commutation processes and commutation losses of the parasitic capacitances is taken into account. Based on simulation model of the transistors, the commutation losses are investigated as a function of the work voltage and the work current. The simulation results are represented graphically as a family of characteristics.

Keywords – Power Electronics, CF Inverters, Induction Heating, PSpice Simulation, Transient Analysis.

I. INTRODUCTION

The bridge current fed inverters are widely used in variety induction technologies [1]. Their theory based on thyristor realization is considered in many literature sources [2-5]. Recently, transistor current fed inverters are widely used. This was made possible thanks to the development of technologies in the production of power semiconductor devices.

The transistor current fed inverters allow to increase the working frequency up to hundreds kilohertz. Moreover, a number of features in their modes of operation are observed. They are reviewed in a number of monographies [6,7,8]. Aside from the attention remain the characteristics of the switching processes of the transistors in different modes of operation (resonance, inductance and capacitance detuning of the control frequency in respect to the frequency of the load resonant circuit).

There is also an omission on the part of the producers of power transistors. No data are available for the switching losses as a function of drain-source voltage for MOSFET (as well as collector-emitter voltage for IGBT) transistors. This relationship is important because the drain-source voltage at which transistors are switched is a function of the operating mode of the inverter.

The present paper is devoted to the above mentioned problems.

G. Kunov is with the Department of Power Electronics, Faculty of Electronic Engineering and Technologies, Technical University- Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: :gkunov@tu-sofia.bg

G. Gigov is with the Department of Power Electronics, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: georgigi@abv.bg

E. Gadjeva is with the Department of Electronics and Electronic Technologies, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: egadjeva@tu-sofia.bg

II. COMMUTATION PROCESSES IN THE CURRENT FED INVERTER

The principle circuit of the transistor current fed inverter (CFI) is given in Fig. 1. The inverter power supply is represented by an ideal current source. The realization of this source is described in [8].

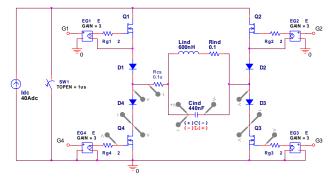


Fig. 1. Principle circuit of the transistor current fed inverter

A. Commutation processes in CFI working at resonance

The waveforms illustrating the work at resonance, are shown in Fig. 2a - Fig. 2e.

The main variables considered are marked on the corresponding graphs: a) P_{sw-on} – switching losses at turn-on of the transistor, P_{sw-onf} – switching losses at turn-off, P_{st-on} – static losses in on-state, P_{st-off} - static losses in off-state; b) V_{g-Q3} and V_{g-Q4} – gate pulses of corresponding even and odd transistor; c) I_{d-Q3} – the current through the transistor Q_3 , V_{ds-Q3} – the voltage on the same transistor, V_{as-D3} – the voltage between the anode of the diode D_3 and the source of Q_3 ; d) V_C – the voltage on the load resonant circuit , I_{Rcs} – the inverter current, I_C – the resonant current through the capacitor of the load; e) the current and the voltages for even transistors and diodes.

The specific features of this mode are: 1) the inverter current and voltage are in phase; 2) In the time interval t_0 - t_2 , the switching mode of the transistor Q_3 is ZVS (zero voltage switching), and for Q_4 is ZCS (zero current switching); 3) In the time interval t_3 - t_5 the switching of the transistors Q_3 and Q_4 is opposite to the previous; 4) In the time interval t_2 - t_3 Q_3 is turn-on and the power P_{st-on} is defined by the drain current and the resistance R_{ds} ; 5) In the time interval t_5 - $t_6 Q_3$ is turn-off, the voltage V_{ds-Q3} follows the load voltage up to its maximal value. Up to this moment the losses P_{st-off} appear as a result of the current through the parasitic capacitances of the transistor. After the time point, corresponding to the maximum of V_C , the diode D_3 is turnoff and the voltage V_{ds-Q3} remains constant equal to the value V_{Cmax} stored on the parasitic capacitance C_{ds} of the transistor Q_3 .

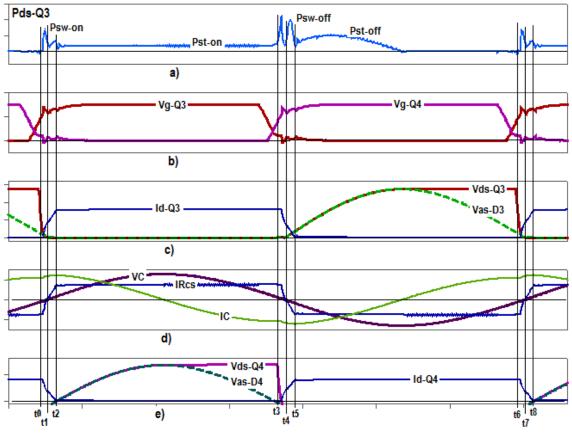


Fig. 2. Commutation processes in CFI working in the resonance $(f_{sw} = f_0)$

In this mode of operation, P_{sw-on} and P_{sw-onf} do not exceed 2 to 3 times P_{st-on} . In work at resonance, the commutation losses are small and the losses during turn-on and turn-off time intervals dominate.

In work at resonance, the commutation losses are small and the losses during turn-on and turn off time intervals dominate.

B. Commutation processes in CFI working at inductance detuning

The waveforms illustrating the work at inductance detuning, are shown in Fig. 3a – Fig. 3d. The main parameters considered are denoted on the graphs in the same way as in Fig.2.

The specific features of the system are: 1) the inverter current I_{Rcs} lags the load voltage V_C - Fig.3c (time interval t_0 - t_4); 2) in the interval t_1 - t_5 the switching mode of the transistor Q_3 is ZVS and for Q_4 - hard switching (switching at nonzero current and voltage); 3) in the interval t_6 - t_7 the switching of transistors Q_3 and Q_4 is opposite of the previous: The transistor Q_3 is switched at nonzero current and voltage, the switching of transistor Q_4 is ZVS. The switching losses P_{st-off} during turn-off of the transistor Q_3 are shown in Fig.3a. Their maximum value exceeds hundred times the static losses P_{st-off} . The maximum value of P_{st-off} is a function of the instantaneous values of the current I_{d-Q3} and the voltage V_{ds-Q3} at the switching moment, i.e. of the angle of detuning.

C. Commutation processes in CFI working at capacitance detuning

The waveforms illustrating the work at capacitance detuning, are shown in Fig. 4a - Fig. 4d. The main parameters considered are denoted on the graphs in the same way as in Fig.2.

The specific features of the system are: 1) the inverter current I_{Rcs} exceeds the load voltage V_C - Fig.4c (time interval t_0 - t_3); 2) in the interval t_1 - t_2 the switching mode of the transistor Q_3 is hard switching and for Q_4 - ZVS; 3) in the interval t_4 - t_5 the switching of transistors Q_3 and Q_4 is opposite of the previous: the transistor Q_3 is ZVS, Q_4 is switching is connected to the application of reverse voltage on the diodes with a large value of dV/dt. As a result, the reverse currents of the diodes (passing through the parasitic capacitances of the transistors) can cause perturbation to the gate circuits of the transistors. It is recommended the use of SiC diodes.

The switching losses at turn-on P_{sw-on} of the transistor Q_3 are shown in Fig.3a. Their maximum value exceeds more than a hundred times the static losses P_{st-on} . The maximal value of P_{st-off} is a function of the instantaneous values of current I_{d-Q3} and the voltage V_{ds-Q3} at the time of switching, i.e. of the angle of detuning.

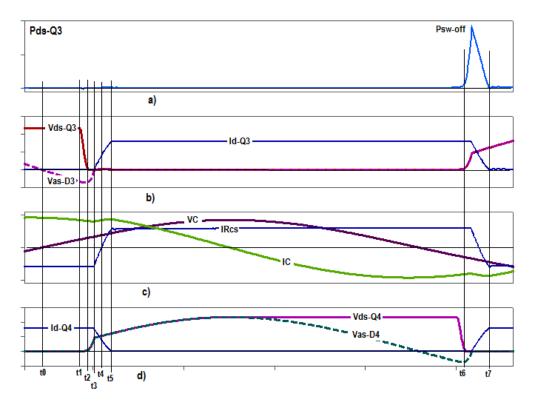


Fig. 3. Commutation processes in CFI working in the inductance detuning $(f_{sw} < f_0)$

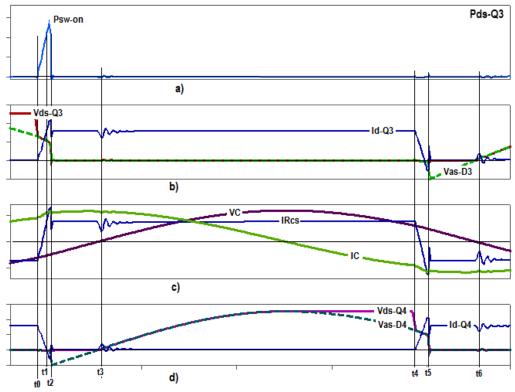


Fig. 4. Commutation processes in CFI working in the capacitance detuning $(f_{sw} > f_0)$

III. INVESTIGATION OF THE COMMUTATION LOSSES DEPENDING ON V_{DS} and I_D

given voltage V_{ds} [9]. There exist in the practice cases when, depending of the mode of operation of the circuit, it of interest investigation of the commutation losses for different values of the voltage V_{ds} and of the current I_d .

Usually, the information for the commutation losses is given in the datasheet as a function of the current I_d for a

The circuit for investigation of the commutation losses depending on drain-to-source voltage V_{ds} as well as depending on drain current I_d is shown in Fig. 5. The simulation results for the power P_{ds} depending on V_{ds} is shown in Fig. 6.

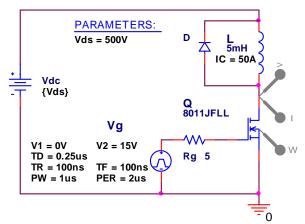


Fig. 5. Basic circuit for investigation of the commutation losses

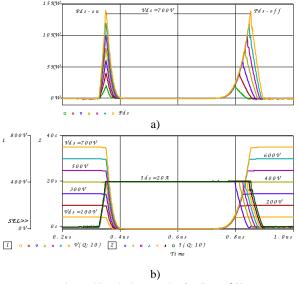


Fig. 6. Simulation results for $P_{ds} = f(V_{ds})$

The simulation results for the energies E_{on} and E_{off} depending on V_{ds} and I_d are presented in Fig. 7 and Fig. 8 respectively. The following macrodefinitions in the graphical analyzer *Probe* are used:

Eon_mJ = Swing_XRange(W(Q),0.3us,0.45us)*0.075us Eoff_mJ = Swing_XRange(W(Q),0.65us,0.95us)*0.15us

In order to obtain graphically the dependencies $E_{on} = f(V_{ds}, I_d)$ and $E_{off} = f(V_{ds}, I_d)$ shown in Fig. 7 and Fig. 8, with respect to two independent variables V_{ds} and I_d , parametric sweep in combination with *File/Append* waveforms option in *Probe* are used.

IV. CONCLUSION

The commutation processes in current fed transistor inverters have been investigated in the three possible modes of operation of the inverter. A *PSpice* model of the circuit is built and simulated and the commutation losses are investigated as a function of the work voltage and the work current, taking into account the transistor parasitic capacitances. The simulation results are represented graphically as a family of characteristics.

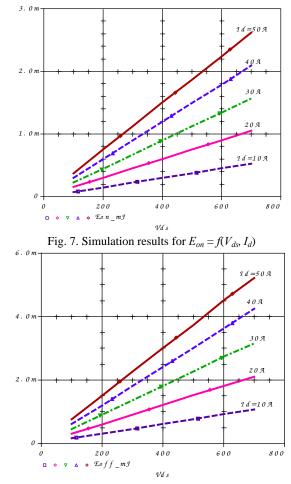


Fig. 8. Simulation results for $E_{off} = f(V_{ds}, I_d)$

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Analysis of a Step-Up DC Converter Considering Real Parameters

Peter Trifonov Goranov

Abstract - Main focus of the work is to obtain the dependencies defining terms of proper performance of boost DC to DC converters, taking into account their real parameters. For this purpose the relation between the increment of the output voltage and the deviation of the control parameter – the duty cycle, is analyzed. Defined is the maximum value of the duty ratio, ensuring proper functioning of the converters. Real characteristics are examined.

Keywords – DC to DC converter, Step-Up, Boost, Buck-Boost Converter, Real Characteristics.

I. INTRODUCTION

In the proposed paper is analyzed the influence of the actual parameters of a step-up converter on its proper performance. It includes the impact of the internal resistance of the power supply, the channel resistance of the power MOS transistor, the resistance of the connecting wires. Such problems are mentioned in [1], [2], [3].

In some experiments with DC-to-DC converters at which the output voltage is boosted, there is the following effect – to a certain amount of increase in the duty cycle the output voltage increases. After this value the growth stops, although rising of the duty cycle, and next – the output voltage drops sharply to near zero.

The process is illustrated in Figure 1. It is used a standard circuit of step-up converter [4]. When the duty ratio (δ) increases, the output voltage (U_o) increases too, which leads to an increase in load current (I_o) and the consumed by the source current (I_s), respectively. That generates reducing the actual supply voltage of the DC converter (U_d) in the real circuit and U_o, respectively. Usually, the converters comprise an automatic control of one of the load parameters (typically the output voltage). To correct this decrease the coefficient δ is increasing. This leads to stabilization and setting the operating mode of the converter.

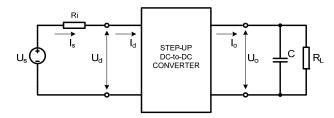


Fig. 1. Block Diagram for Analyses

If it turns out that a certain increase of δ , respectively U_o,

P. Goranov is with the Department of Power Electronics, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: pgoranov@ecad.tu-sofia.bg I_o and I_{s} , the reducing the converter input voltage U_d is large enough and the unsatisfactory operation is obtained – the output voltage can't reach the required stabilized value. In an attempt to compensate for the error the converter's control circuit starts to increase modulation depth δ until the maximum duration of a transistor gate pulse is reached ($\delta = \delta_{max}$, eg. 95%). Usually this results in nearly a short circuit at the input of the converter, and significant reduction of output voltage. This emergency operation holds over activating the current protection or the interruption of load.

Very often, the DC-to-DC converters are designed to a predetermined operation mode set, with a given duty cycle, which may be significantly less than the maximum possible. Then, in case of this unstable mode described above, the input inductor may become magnetic saturated that ensures a short-circuit mode of the converter input.

The same effect can be caused by the substantial reduction of the load $R_{\rm L}$.

The purpose of the study is to analyze the conditions of maintaining the stable mode of converter operation, determine the proper range of δ variation with known parameters of the actual DC converter.

II. ANALYSES

A. Postulation of the Problem

For analysis of the mode of operation of a real step-up DC-to-DC converter the following formulation is used:

- ◆ constant supply voltage U_s=const;
- power source internal resistance is R_i=const;
- efficiency $\eta=1$;
- load resistance is R_L=const.

The dependence of the increment of the output voltage dU_0 yield by the increment of the duty cycle d δ , taking into account real parameters of the converters, is examined. For this purpose and the relationship between the output voltage and the coefficient δ is obtained.

B. Real Output/Input Voltage Ratio

For the Block diagram of Figure 1 the following equations can be written:

• input voltage of the converter -

$$U_d = U_s - R_i I_s \tag{1};$$

• load current – $I_o = U_0 / R_L$.

The following ratios are known for the step-up converter:

$$U_o = \frac{U_d}{1 - \delta} \tag{2}$$

$$I_s = I_d = \frac{I_o}{1 - \delta} = \frac{U_o}{R_T} \cdot \frac{1}{1 - \delta}$$
(3)

Substituting U_d from (1) in (2) the result is

$$U_o = \frac{U_s}{1 - \delta} - \frac{R_i \cdot I_s}{1 - \delta} \tag{4}$$

or

$$\frac{U_{o}}{U_{s}} = \frac{1}{1 - \delta} - \frac{R_{i}}{R_{L}} \cdot \frac{U_{o}}{U_{s}} \cdot \frac{1}{(1 - \delta)^{2}}$$
(5)

The solution of the equation is

$$\frac{U_o}{U_s} = \frac{1}{1 - \delta} \cdot \frac{1}{1 + \frac{R_i}{R_L} \cdot \frac{1}{(1 - \delta)^2}}$$
(6).

The relationship between the input and the output voltage in real step-up converter is expressed by equation (6), which contains the part showing the ideal ratio and the correction, taking into account the real parameters of the converter.

This relationship is shown in Figure 2, together with the ideal characteristic depending on the duty cycle at different values of the ratio R_i/R_L (0.01, 0.05, 0.1). The similar results are published in [3].

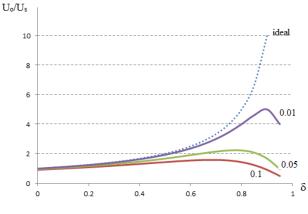


Fig. 2. The Relative Output Voltage U_0/U_s versus δ

C. Output Voltage Increment

The change of the output voltage is described by a series of equations that mathematically described the processes in the scheme.

Using the real relationship (6) the output voltage increment is determined by

• supply voltage variations – dU_s , which are out of the scope of this paper

$$dU_o = \frac{1}{1 - \delta + \frac{R_i}{R_L} \cdot \frac{1}{(1 - \delta)}} dU_s \tag{7};$$

• δ -coefficient variations – d δ .

This dependence of the output voltage increment from $d\delta$ is described by

$$dU_o = -U_s \cdot \frac{\frac{R_i}{R_L} - (1 - \delta)^2}{\left(\frac{R_i}{R_L} + (1 - \delta)^2\right)^2} \cdot d\delta \qquad (8)$$

or

$$\frac{dU_o/d\delta}{U_s} = \frac{(1-\delta)^2 - \frac{R_i}{R_L}}{\left((1-\delta)^2 + \frac{R_i}{R_L}\right)^2}$$
(9).

n

The converter is operated in normal, step-up mode, while satisfying the requirement $dU_0/d\delta \ge 0$, which takes place at

$$\left(1-\delta\right)^2 - \frac{R_i}{R_L} \ge 0 \tag{10}.$$

D.Maximum duty ratio

For a stable operation of the inverter the requirement (10) must be fulfilled, that indicates the relationship between the duty cycle and the actual parameters of the converter – the ratio R_L/R_i . The maximum "allowable" value could be obtained from

$$\left(1-\delta\right)^2 = \frac{R_i}{R_L} \tag{11}.$$

Solution of the boundary equation is

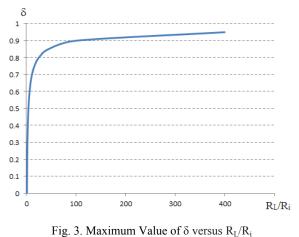
$$\delta_{\max} = 1 \pm \sqrt{\frac{R_i}{R_L}}$$
(12).

Due to the limited value of the duty ratio $-\delta \le 1$ the solution is

$$\delta_{\max} = 1 - \sqrt{\frac{R_i}{R_L}}$$
(13).

The dependency is shown in Figure 3 and Figure 4 (the difference in scaling) – the maximum permissible value of the coefficient δ can be determined for known value of

 $R_L/R_i.$ It is seen that the parasitic impedance R_i has a negligible influence if $R_L/R_i{>}100.$



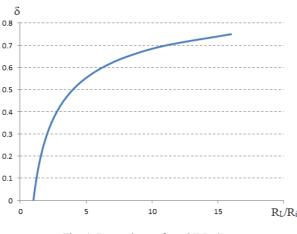


Fig. 4. Dependence δ_{max} OF R_L/R_i

E. Maximum duty ratio in real circuits

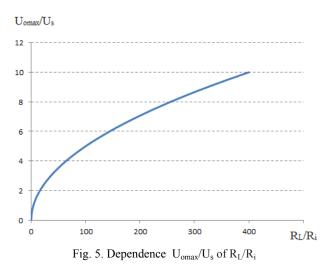
The resulting range of duty cycle variation, commented above, can be used for manual control of the output voltage.

If the automatic control circuit is used to adjust the output voltage this rule is not applicable. Usually, the regulator aims to stabilize the output voltage of a predetermined level. When the output voltage stabilization requires increased duty cycle over the limit value, $\delta > \delta_{max}$, will get unstable mode.

To avoid receiving this mode, the set point for the value of the output voltage must not exceed the maximum possible real value $-U_{omax}$. It is obtained at the maximum value of the coefficient $\delta - \delta_{max}$ of (13), replacing in (6)

$$\frac{U_{o\max}}{U_s} = \frac{1}{2} \cdot \sqrt{\frac{R_L}{R_i}}$$
(14).

The dependence is presented in Figure 5. It is seen that, for example in relation $R_L/R_i = 100$, the relative value of the maximum voltage is $U_{omax}/U_s = 5$. Therefore, the output voltage shouldn't be set to a larger value, otherwise the converter will operate improperly.



III. ANALYSES OF BUCK-BOOST CONVERTERS

All analyses, descriptions and considerations made before are applicable to all DC converters in which a boosting of the output voltage exists. Similarly, they can be analyzed to derive the required ratios defining the field of sustainable operation.

A. Real Output/Input Voltage Ratio

For all buck-boost converters relationship between input and output voltage is expressed by

$$U_o = \frac{\delta}{1 - \delta} U_d \tag{15}.$$

Based on equation (1) the relationship between the input and the output voltage in real converter is expressed by

$$\frac{U_o}{U_s} = \frac{\delta}{1-\delta} \cdot \frac{1}{1+\frac{R_i}{R_L} \cdot \frac{\delta^2}{(1-\delta)^2}}$$
(16).

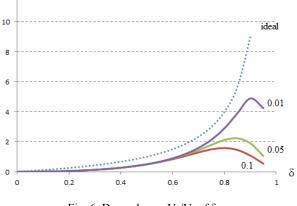


Fig. 6. Dependence U_o/U_s of δ

U_o/U_s

Equation (16) is presented graphically in Figure 6. It can be seen significant influence of real input parameters when coefficient $\delta > 0,4$. Naturally output voltage starts from zero.

B. Output Voltage Increment

Increment of the output voltage caused by deviation of duty cycle is obtained from expression (17)

$$\frac{dU_{o}/d\delta}{U_{s}} = \frac{(1-\delta)^{2} - \frac{R_{i}}{R_{L}} \cdot \delta^{2}}{\left((1-\delta)^{2} + \frac{R_{i}}{R_{L}} \cdot \delta^{2}\right)^{2}}$$
(17).

C. Maximum duty ratio

The converter is operated in normal mode, while satisfying the requirement $dU_0/d\delta \ge 0$.

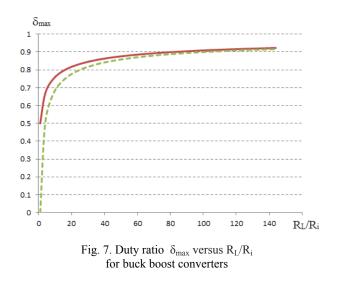
Maximum operating duty ratio is derived from the condition

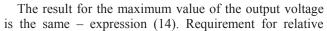
$$\left(1-\delta\right)^2 = \frac{R_i}{R_L} \cdot \delta^2 \tag{18}$$

Solution is

$$\delta_{\max} = \frac{1}{1 + \sqrt{\frac{R_i}{R_L}}}$$
(19).

This dependency is displayed graphically in figure 7. For comparison the same dependency for the step-up converter is shown (with a dotted line). It is seen the less influence of real parameters in case of buck-boost converters.





value of the output voltage must be fulfilled in order to stay in proper mode of operation.

IV. EXPERIMENTAL RESULTS

Results of real circuit measuring of the output voltage U_{omeas} compared with calculated values U_{ocalc} (in Volts) are shown in Table 1. The circuit parameters are as follows: supply voltage $U_s=24V$, input resistance $R_i=0,45\Omega$, load resistance $R_L=4,5\Omega$, period of load frequency T=47µs. The control parameter is pulse width (t_p). The results and simulation results confirm the obtained dependencies.

TABLE 1. RESULTS FOR OUTPUT VOLTAGE

t _{p,} μs	0	10	20	25	30	35	40	45
δ	.0	.213	.426	.532	.638	.745	.851	.957
Uomeas	21.4	25.8	31.3	34.3	36.4	35.8	27.8	8.4
U _{ocalc}	21.8	26.3	32.1	35.2	37.6	37.1	29.3	10

V. CONCLUSION

In the paper is analyzed the influence of real parameters on the range of voltage (U_o/U_s) and duty (δ) ratio. The equations are obtained for maximum output voltage and acceptable values of duty ratio with respect to the real relation R_I/R_i .

The real estimation of problems described above depends on the ratio R_L/R_i . The resistance R_i is the internal resistance of the source, but that the transistor R_{DSON} and connecting wires. For high power sources as an accumulator or a supercapacitor with currents of hundreds of amperes the internal resistance is a few milliohms (5-10 m Ω). For such currents the resistance of the channel of the MOS transistor is a significantly less and can be reduced to 1-2 m Ω . At the same time the load impedance is about 100-600 m Ω (12V, 24V or 60V at 100-200A).

The ratio R_L/R_i is approximately in the range 20-100. If it is close to the lower limit, the designer must be careful as the obtained dependencies show. This ratio is much greater than 100 for low-power applications and the influence of real parameters R_L/R_i can not manifest itself.

This effect is especially clearly seen in the power supplies with current limiting - lab voltage sources, photovoltaic panels. The operation with current limit highly increased internal resistance R_i of the power source.

In case of photovoltaic as a power supply the proper work of a step-up converter is very unpredictable because of variations of output panel current.

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Quasi Resonant DC-DC Converters

Nikolay Rangelov Rangelov and Nikolay Lyuboslavov Hinov

Abstract – In present paper a review of quasi-resonant DC-DC converter is done. Such converters have lower commutation losses in comparison with the hard switching converters. The main circuit of mentioned converters, which have ZCS and ZVS (zero current switching and zero voltage switching) are examined. The equivalent circuits are presented, which makes possible the analysis of such type of converters.

Keywords – Quasi-resonant converters, soft-switching, DC-DC converters

I. INTRODUCTION

In the work are examined quasi-resonant DC converter with so called "soft commutation" – zero current switching (ZCS) or zero voltage switching (ZVS). Such converters have decreased switching losses in comparison with converters with "hard switching". Different circuit version with and without transformer output are described, thus are shown their equivalent circuits, which helps the analysis and obtainment of waveforms of such converters.

Generally DC-DC converters operate in hard-switching mode of devices, which are switching-on and off with nonzero values of current or voltage, even worse with maximum values of current and voltage. With such commutation big losses are observed. The reduction of losses can be achieved with snubber groups or the soft switching method [1, 2, 3]. Typical for the method is the further addition to the power circuit of converter a resonant L_rC_r circuit and depending on the mode of connection, it may be serial or parallel. Thus we obtain ZVS when the connection is serial, while it is parallel we get ZCS.

II. ZVS DC-DC CONVERTERS

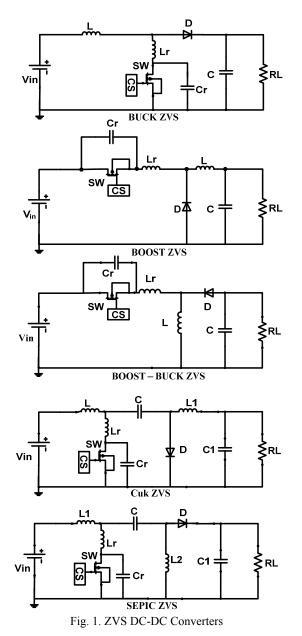
In Fig.1 are presented the basic circuits of DC-DC converters: Buck, Boost, Boos-Buck, Cuk and Sepic, as to them were added respectively serial resonant circuit for receiving ZVS mode.

From [1, 4, 7, 10, 11, 13, 14] is known that we can divide into 4 time intervals of operation of all ZVS quasi-resonant converters:

- First stage energy accumulation in resonant inductance;
- Second stage switch conductance;
- Third stage charging the resonant capacitor;
- Fourth stage resonant process.

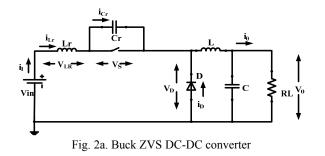
N. Rangelov is with the Department of Power Electronics, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: nikran80@gmail.com

N. Hinov is with the Department of Power Electronics, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: hinov@tu-sofia.bg



After some studies and simulations of DC-DC converters with ZVS and serial resonant circuit, we confirmed the a.m. four stages of operation. Thus we are going to examine in details the Buck DC-DC converter, shown in Fig.2a.

For the different stage of operation in Fig.2b-2e are presented the 4 equivalent circuit for each stage, while in Fig.3 are shown the waveforms, which illustrate its action. **First stage**: from the moment 0 to t_1 – time interval during which we have energy accumulation in the inductance Lr, while switch and diode are ON. The equivalent circuit of that stage is shown in Fig.2b. During that interval for currents and voltages are valid the following equations: $V_S = 0$, $I_L = 0$, $I_C = 0$, $V_{LR} = V_I$. The stage ends with zero current through diode, e.g. $I_D (\omega_s t_1) = 0$.



Second stage: for the time interval $t_1 < t \le t_2$, diode is OFF, e.g. there is no current through it. The equivalent circuit for this stage is shown in Fig.2c. During the stage are valid the following equations: $V_S = 0$, $I_{CR} = C_r d_{VS} / dt = 0$, $I_D = 0$, $i_s = i_{LR} = I_0$, $V_{LR} = Lr di_{Lr} / dt = 0$, and $V_D = V_I$. The stage ends with transistor's switching off $\omega_s t_2 = 2\pi D$.

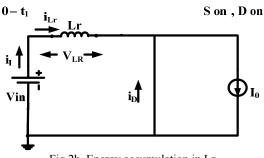
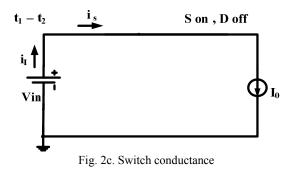


Fig.2b. Energy accumulation in Lr

Third stage: for time interval $t_2 - t_3$. The switch and diode are OFF, while capacitor Cr is charging. The equivalent circuit is shown in Fig.2d. During the stage are valid the following equations: $i_S = 0$, $I_D = 0$, $I_{LR} = I_{CR} = I_O$, $V_{LR} = 0$. The stage ends when the voltage across diode reaches 0, e.g. $v_D (\omega_s t_3) = 0$.



Fourth stage: for time interval $t_3 - T$. Diode changes its state from OFF to ON. The equivalent circuit of the stage is shown in Fig.2e. During that stage for currents and voltages are valid the following equations: $i_s = 0$. In resonant circuit are running resonant processes with the next initial conditions: $I_{LR} (\omega_s t_3) = I_0$ and $v_{Cr} (\omega_s t_3) = V_S (\omega_s t_3) = V_I$.

From waveforms, shown in Fig.3 it is obvious that transistor is switching ON and OFF with ZVS, while diode is switching OFF with ZCS.

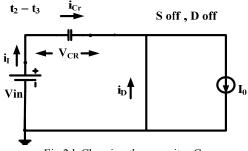
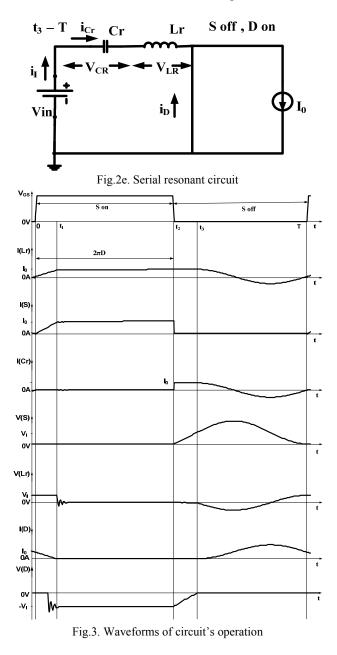


Fig.2d. Charging the capacitor Cr

The additional resonant circuit hardly changes circuit's operation, but helps decreasing commutation losses in switch, because we have ZVS in switching ON and OFF.

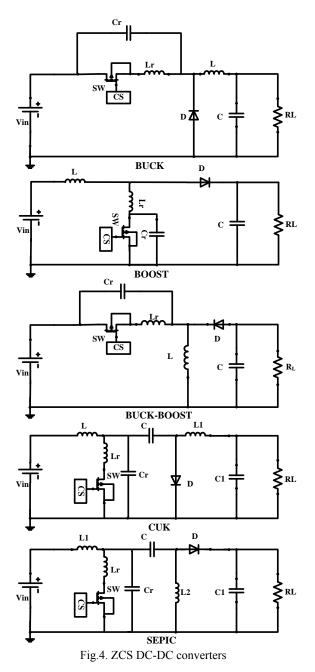


The differences with classic circuits (with hard switching) are in the transistor's voltage, which is higher

and depends on circuit's Q-factor. There is no difference between both type of circuits regarding the current.

III. ZCS DC-DC CONVERTERS

If we add in parallel a capacitor to serial connected switch and resonant inductance, we will obtain DC-DC converters with ZCS [1, 15, 16].

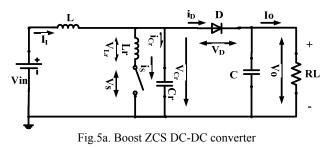


In Fig.4 are shown the basic circuits of DC-DC converters with ZCS – Buck, Boost, Boost-Buck, Cuk and Sepic.

Again, similarly to ZVS converters, we have 4 stages of operation [1, 3, 13]:

- First stage: during which capacitor is charging;
- Second stage: switch conductance;
- Third stage: energy accumulation in resonant circuit;
- Fourth stage: resonant process.

After some studies we found all 4 stages are usual for all circuits with ZCS DC-DC converters. The processes will be examined in details only for Boost DC-DC converter with ZCS. The circuit of the converter is shown in Fig.5a. The stages of operation are presented with their respective equivalent circuit in Fig.5b-5e.



First stage: time interval $0 - t_1$. During which the resonant capacitor Cr is charging. The equivalent circuit is shown in Fig.5b. Throughout that stage switch and diode are OFF, and for currents and voltages are valid the following equations: $i_S = 0$, $i_D = 0$, $v_{Lr} = 0$ and $i_{Cr} = I_I$. The stage ends when $v_D(\omega_S t_1) = 0$;

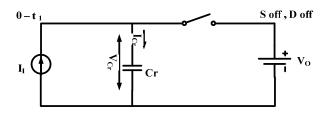


Fig.5b. Capacitor Cr charging

Second stage: time interval $t_1 - t_2$. During which we have energy accumulation in resonant inductance Lr. Stage's equivalent circuit is shown in Fig.5c. For currents and voltages are valid the following equations: $i_S = 0$, $i_D = I_I$, v_D = 0, $v_{Lr} = 0$, $v_{Cr} = v_S = V_O$, $i_{Cr} = 0$ and $i_D = I_I$. Stage ends when Control Systems switches ON the switch and transistor starts conducting – the moment $\omega_S t_2 = 2\pi(1 - D)$;

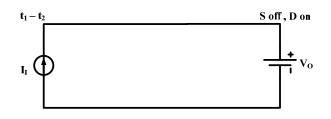


Fig.5c. Energy accumulation in Lr

Third stage: time interval $t_2 - t_3$. During which the switch is ON. The equivalent circuit is shown in Fig.5d. For currents and voltages are valid the following equations: $v_S = 0$, $v_D = 0$, $v_{Lr} = v_{Cr} = V_0$ and $i_{Cr} = 0$. Stage ends with diode's switch OFF, when $i_D (\omega_S t_3) = 0$;

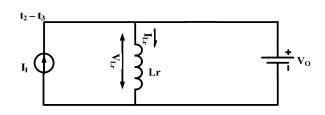


Fig.5d. Switch conductance

Fourth stage: time interval $t_3 - T$. During which resonant process run. Equivalent circuit is shown in Fig.5e, while for currents and voltages are valid the following equations: $v_S = 0$ and $i_D = 0$, $v_{Lr} = 0$. Initial conditions for resonant process are respectively: $i_{Lr} (\omega_S t_3) = i_S (\omega_S t_3) = I_I$ and $v_{Lr} (\omega_S t_3) = V_O$.

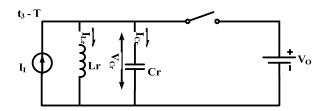
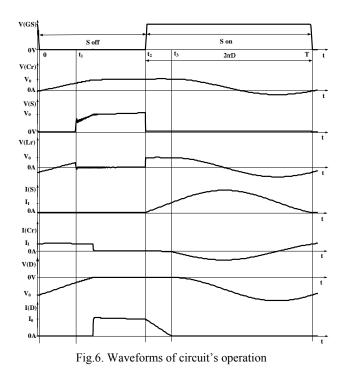


Fig.5e. Parallel resonant circuit

Waveforms, which describe operation of circuit are shown in Fig.6. From there is obvious that transistors switches ON and OFF with ZCS, while diode switches OFF with ZVS. Also the additional resonant circuit barely changes mode of operation, but assists for diminishing commutation losses, because of ZCS.



IV. CONCLUSION

After the studies carried out we can make a conclusion that circuits with additional serial or parallel resonant circuit have lower commutation losses. This achievement is because of ZVS and ZCS. This let us increasing the frequency of operation and from there decreasing values of circuit's passive components (inductances, transformers) and size and weight of Power Devices as a whole. The main weakness is the higher voltages or currents over the semiconductor switches, which augments conductance losses.

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Comparative Analysis of Supercapacitors and Batteries as Energy Storage Systems

George Vassilev Kraev and Nikolay Rangelov Rangelov

Abstract – The present paper examines supercapacitors, somewhere called ultracapacitors, and lead-acid batteries as storage systems. The study confirms the advantages and disadvantages of both elements. The experiments were made at Tecnalia, Derio (Vizcaya), E-48160, Spain.

Keywords – UPS, Inverter, supercapacitor, ultracapacitor, battery, lead-acid batteries, storage systems

I. INTRODUCTION

The global warming and climate change are todays concern, together with peak oil and high petroleum prices, pokes governments to support the renewable energy. Evidently new legislation has been implemented, especially in the European Union, accompanied with incentives and sanctions. So the branch of renewable energy production was commercialised. The push born rush in building wide range of wind power farm, photovoltaic plants, solar and geothermal powers. One of the biggest drawback of such production is the necessity of storage systems. Obviously the wind blows and the sun shines not when we need their energy, but under other (natural) laws, thus from here emerge the need of storage systems.

The work is far away from breakthrough as we desired, but our dream was in a way fulfilled — we found a huge bank of supercapacitors and their close friend lead-acid batteries at Tecnalia, Vizcaya, Spain. Such wonderful elements can be found in Bulgaria. Therefore we started studying the stock at Tecnalia. [1, 2, 3, 7]

II. THE SUPERCAPS

We will use the terms Supercapacitor and Ultracapacitor interchangeably. So, our devices are from ESMA (Trade Mark) and the model is 10EC303. [7]

The ultracaps were mounted in a rack and were connected 8 pcs. in two rows by 4 supercaps. The capacitors in each row were connected in series, while the two rows were in parallel each other. The supercapacitors' parameters are given in Table 1. [7]

The capacitor where charged through UPS from Accratech (Trade Mark), from Linear/1 range and the model is U91-5k. The UPS parameters are given in Table 2.

George Kraev is from the Department of Power Electronics at the Faculty of Electronics and Engineering Technologies, Technical University of Sofia: 8, Sv. Kliment Ohridski Blvd., 1756 Sofia, Bulgaria. Email: kraev@tu-sofia.bg

N. Rangelov is with the Department of Power Electronics, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: nikran80@gmail.com



Fig. 1. Supercaps, mounted in rack

TABLE 1. PARAMETERS OF SUPERCAPACITORS (10EC303)

PARAMETER	VALUE	UNIT
Application	Backup	
	power	
Operating temperature	$-50 \div +60$	°C
Operating voltage	14,5 ÷ 7,25	V; 25°C
window		
Capacitance	4500	F
Energy stored (within	355	kJ; 25°C
operating voltage		
window)		
Maximum power	506,25	kJ
Internal ohmic resistance	2 (3)	mΩ;
		25°C
Size (LxWxH)	538x205x260	mm
Weight	34	kg

The modern storage systems are considered to be the supercapacitors. They theoretically have unlimited live (because of infinite number of cycles charge / discharge). As shown in Fig.2, charging of supercaps is relatively fast. For 1 hour charging we have charged almost the full capacity of supercaps. In comparison with traditional storage systems (e.g. lead-acid batteries) the speed of charging is 14 times high (we have charged the lead-acid batteries at full capacity for 14 hours). While the limitless number of cycles charge / discharge or in other words – the lifecycle of such storage cannot be proved or rejected, the speed of charging is obvious. Therefore, we can consider that charging speed of supercapacitors is one of their biggest advantages.

TABLE 2. UPS PARAMETERS (AC	CCRATECH U91-5K)
-----------------------------	------------------

PARAMETER	VALUE	UNIT
Capacity	5 / 5	kVA/ kW
AC Input Voltage range	147 ÷ 264	V
Operating frequency	50 or 60	Hz
	100 / 110 /	
	115 / 120 /	
Output Voltage	200 / 208 /	V
	220 / 230 /	
	240	
Output Voltage waveform	sinewave	
Input Nominal Current	200V = 28A	А
(at full load)	240V = 23A	A
Size (HxWxD)	737 x 267 x	mm
Size (IIXWAD)	654	11111
Weight	134	kg

Our supercapacitors were made with one of the most advanced technology for their time. They are electrochemical and do not contain (unlike the lead-acid batteries) lead, arsenic, mercury, cadmium or other toxic ingredients. The supercapacitors are of asymmetric design and uses a negative electrode of activated carbon material (polarizable electrode) and a positive Faradaic (nonpolarizable) electrode. The positive electrode is made of nickel oxyhydroxide. A low cost aqueous KOH solution (as in alkaline batteries) is used for the electrolyte.

ESMA asymmetric ultracaps of third generation have long service live, low self-discharge, do not require maintenance during operation and storage, have wide operating temperature range and operates reliably even at extremely low temperatures (e.g. -50°C).

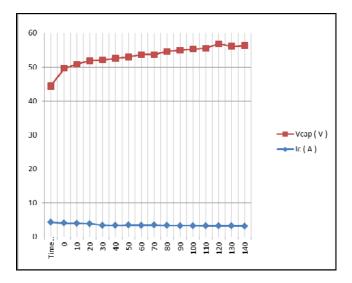


Fig. 2. Supercapacitor charging (X-axis: time in minutes, Y-axis: V_{CAP} – capacitors' voltage, I_C – charging current)

As shown in Fig.3 and Fig.4 we have discharged the supercapacitors with 2 different loads – the power of first load was 460 W, while the second was 2,3 kW. The waveforms show relatively fast discharging. What is more, nevertheless that the second load is 3 times bigger, the time for discharging does not change so much, in both cases it remains around 20 minutes.

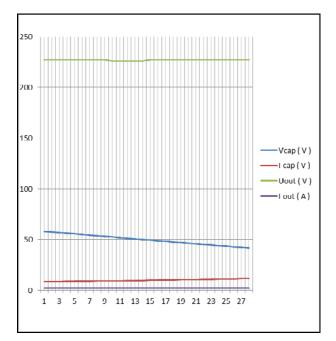


Fig. 3. Supercapacitors discharging with 460W load (X-axis: time in minutes; Y-axis: V_{CAP} – capacitors' voltage, I_{CAP} – capacitors' current, U_{OUT} – output voltage, I_{OUT} – output current)



Fig. 4. UPS front panel

This could be judged as one of the biggest disadvantages for the supercapacitors. Another disadvantage could be their high price. Not only the value of one piece of supercapacitor is astronomical, but the same conclusion could be made in relative units – price per unit capacity, measured in Amper hours (Ah), which is one of the main figures when we evaluate storage systems

Summarising the thoughts up to now we can say for supercapacitors:

- fast charging
- fast discharging
- high price

Of course, there are some parameters, which cannot be studied. For example we did not have studied the level of operation in low temperatures (e.g. -50° C).

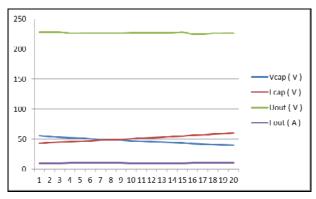


Fig. 5. Supercapacitors discharging with 2317W load (X-axis: time in minutes; Y-axis: V_{CAP} – capacitors' voltage, I_{CAP} – capacitors' current, U_{OUT} – output voltage, I_{OUT} – output current)

III. THE LEAD-ACID BATTERIES

The studied batteries were manufactured by EXIDE Technologies, the model is OPzS Solar 550. Their parameters are shown in Table 3. [5]

For charging and discharging we have used a Xantrex SW Series Inverter / Charger. Its parameters are given in Table 4.

TABLE 3. LEAD-ACID CELL PARAMETERS

PARAMETER	VALUE	Unit
Nominal Voltage	2	V
Nominal Capacity C ₁₂₀	550	Ah
Internal Resistance	0,63	mΩ
Short Circuit current	3250	А
Size (LxWxH)	126x208x520	mm
Weight (incl. acid)	26,7	kg

It is not extremely necessary to present the charging waveforms of lead-acid batteries. It is a boring curve, which gradually increment the voltage for a large pile of time. It is enough to say, that we have reached the full charging capacity of lead-acid battery for more than 14 hours.

For the batteries itself we can say that they are very high operational reliability under rough operating conditions, low maintenance due to optimised alloy and large electrolyte reserve (but they it anyway, while supercapacitors – don't), 20 years design life at 20 °C ambient temperature (80 % remaining capacity from C_{10}), the container is made from high quality transparent plastics, low gassing due to antimony alloy < 3 % (EN 50272-2).

 TABLE 4. PARAMETERS OF INVERTER/CHARGER(XANTREX SW

 Series) [8]

PARAMETER	VALUE	UNIT
AC Input Voltage	240	V
AC Input Current	60 pass thru 30 charging	А
Continuous Power (25°C)	4000	VA
Efficiency (peak)	94	%
Output Voltage (RMS)	240	V
DC Input Voltage	12	VDC
DC IN Voltage range	11,8 ÷ 16,5	VDC
Idle Consumption	<16	W
Max Charge Rate (12V)	150	А
Size (HxWxD)	38 x 69 x 53	mm
Weight	41	kg



Fig. 6. One cell of the battery

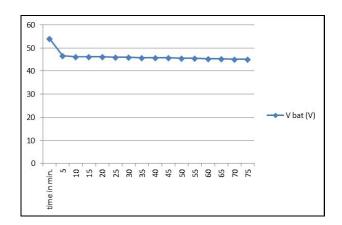


Fig. 7. Discharge of batteries with 2317W load (X-axis: time in minutes; Y-axis: V_{BAT} – Batteries' voltage)

IV. CONCLUSION

The comparison between supercapacitors and lead-acid batteries as energy storage systems can be given in a table, as follows:

TABLE 5. COMPARISON BETWEEN SUPERCAPS
AND LEAD-ACID BATTERIES

PARAMETER	SUPERCAP	BATTERRY
Price	extremely high	moderate
Price / capacity	high	low
Speed of charging	high	low
Speed of discharging	high	low
Self-discharge rate	low	moderate
Lifecycle	unlimited	relatively short
Power density*	low	high

*) The power density describes ability of device of obtaining power from a single volume unit.

The power density is one of the major disadvantages of supercapacitors in comparison with lead-acid batteries. For example, one supercap as described in Table 1 has approximately 140 Ah of capacity (energy), which makes the supercapacitor almost twice heavier and triple in volume comparing it to the lead-acid battery.

Perhaps combining advantages and trying to eliminate the disadvantages, the mutual work of supercaps and lead-acid batteries is worth consider. [9, 10]

ACKNOWLEDGEMENT

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Net Zero Energy House

Miroslav Olegov Gerasimov, Nikolay Luyboslavov Hinov and Irina Peteva Veleva

Abstract - The main topic of this paper is designing a Net Zero Energy House. This topic was chosen between many others due to the fact that is concerning a main issue that stands in front of our modern community. Energy efficiency and reducing energy consumption is main goal through all developed countries.

Keywords – Net zero energy house, power electronics, power conversion, alternative energy sources.

I. INTRODUCTION

The focus of this paper is to present the main aspects of the design process of Net Zero Energy House. House's energy system will be based on Photovoltaic array which will be scaled based on energy analysis. The excess amount of energy that has been produced during the lowconsumption hours will be used to power an Electrolyzer which will provide hydrogen needed for Fuel Cell (FC). The FC itself will produce electricity during nights and low light evening hours and will serve as an auxiliary power source during peak consumption hours. Hydrogen storage tanks will be used to store the produced hydrogen.

II. STRUCTURAL DESIGN

The goal of this project is to design a house that will produce more energy than it consumes in yearly plan. This could be done only if the house has been built with superior energy efficiency in mind. By far the most energy efficient houses are built according to the German Passive House Standard [1].

Passive house standard has severe criteria for energy consumption within the house. Heating demands should not exceed $15kWh/m^2$ per year and total primary energy consumption should be less than $120kWh/m^2$ [1]. These figures could only be reached with high performance HVAC system. The HVAC systems approved by Passive House Institute – Darmstadt rely on high performance heat exchangers with effectiveness as high as 90%. This system sucks out the air from laundry room, bathrooms and other utility rooms and exchanges it for fresh air with negligible difference in the temperature of both air fluxes. Due to the high effectiveness of the system usually no other active heating system is required.

Passive house standard represent a whole new way of

M. Gerasimov is with the Department of Power Electronics, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: m.gerasimov@hotmail.co.uk

N. Hinov is with the Department of Power Electronics, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: hinov@tu-sofia.bg

I. Veleva is with the Department of Power Electronics, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria.

construction and modeling of residential houses. Houses built to meet the criteria of this standard are designed to take maximum advantage of solar radiation [1]. They have precisely calculated triple glazed windows mainly installed on the south facing wall of the house. These windows are responsible for providing enough daylight in order to remove the need of artificial lighting. Furthermore, these windows will reduce the need of heating by more than 85% as they have positive net energy balance – their gain is bigger than losses.

Another important milestone in the structural design is the air tightness of the house. Building's envelope should not have air leakages and should be thermal bridge free.

This is done by using super insolation – exterior walls should have a U value (wall thermal conductivity) lower than 0.15 [W/m2K]. Insulation layers usually reach thickness as high as 25 - 30 cm. depending on the used materials.

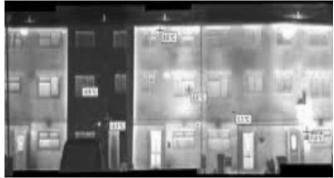


Fig.1. Passive house compared to conventional buildings

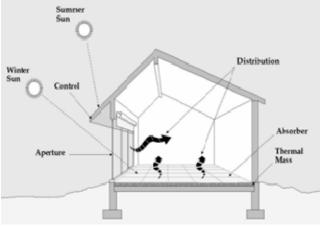


Fig.2. Passive solar design techniques

Orientation of the house is also important point in the design process. The house should mainly be facing south and be designed with passive solar techniques in mind. This includes positioning of windows, overhangs, proper shading for eliminating summer sun radiation penetrating into the house.

III. ENERGY BALANCE

Proper sizing of the energy system is crucial for Zero Energy Buildings. Precise calculations of energy consumption for all appliances, HVAC system, heating and domestic hot water (DHW) are important part of sizing the energy system.

Category of Energy Consumption	Zero Energy Building Annual, (kWh)	Typical House Annual, (kWh)
Space Cool	921	1830
Space Heat	1767	12900
Hot Water	348	490
Vent. Fans	14	170
Pumps & Aux.	213	190
Misc. Equip.	1576	1590
Area Lights	598	530
Total	5437	17700

TABLE 1. ENERGY CONSUMPTION COMPARISON

During the spring – summer period, production of electricity is higher and more excess energy is produced during the low consumption hours. This excess energy is used to power an Electrolyser which is extracting hydrogen from water and feeds it to a storage vessel for later use.

This type of energy system eliminates the need of batteries which supply energy for limited amount of time while the FC can produce electricity and heat until hydrogen is present in the storage vessel.

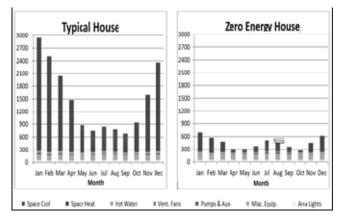


Fig. 3. Energy consumption chart comparison

IV. ENERGY SYSTEM

Energy efficiency is top priority in this project. Therefore building's energy consumption is dramatically reduced by using low consumption energy star appliances, air tight building envelop- eliminating the need of active heating system, using passive solar systems and excess heat from FC for providing domestic hot water, etc.

Due to this dramatic reduction in energy consumption, building's energy needs could easily be satisfied by photovoltaic array coupled with electrolyser and fuel cell.

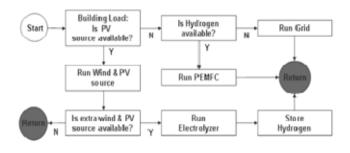


Fig. 4. Combined Solar- Hydrogen system process flowchart

Solar PV Array

According to the simulated energy consumption of the house, the optimal PV solar system consist of 13 PV panels by Ertex Solar with nominal power of 505W split in two strings of 8 and 6 panels each. Those PV panels will be connected to SMA DC/AC power inverters with nominal of 4 kW and 3kW each.

13 x Ertex Solar VSG 580 (P Azimuth angle: 0°, Inclination: 30		PV peak power: 7.05 kilip		
🐘 1 x S8 4000TL-21 🐘 1 x S8 3000TL-21				
Technical data				
Total number of PV modules:	13	Energy usability factor:	1.00 %	
PV peak power:	7.54 kWp	Performance ratio (approx.)*:	84 %	
Number of inverters:	2	Spec. energy yield (approx.)*:	1.160 kWh/kWp	
Nominal AC power:	7.00 kW	Line losses (in % of PV energy):		
AC active power:	7.00 kW	Unbalanced load:	77.00 kVA	
Active power ratio:	92.8 %	Self-consumption:	2:166.89 kWh	
Annual energy yield (approx.)*:	8744.70 kWh	Self-consumption guota:	24.8 %	

Fig. 5. DC/AC Power Invertors - Char

Hydrogen System

Hydrogen system will account for energy production during low light/night hours when PV modules are out of service.

PVGIS estimates of solar electricity generation

Location: 42º41'18" North, 23º17'57" East, Elevation: 577 m a.s.1,

Solar radiation database used: PVGES-CMSAF

Nominal power of the PV system: 7.0 kW (crystalline silicon) Estimated losses due to temperature and low irradiance: 8.8% (using local ambient temperature) Estimated loss due to angular reflectance effects: 2.8%

Other losses (cables,, inverter etc.): 14.0%

Combined PV system losses: 23.8%

Fixed system: inclimation=34°, orientation=3°					
Month	Ed	Em	H_d	H_m	
Jan	13.80	429	2.40	74,4	
Feb	18.90	530	3.31	92.	
Mar	24.30	752	4.38	130	
Apr	26.30	790	4.92	148	
May	28.70	\$\$9	5.50	170	
Jun	30.00	901	5.90	17	
Jul	31.70	983	6.25	19-	
Aug	30.60	949	6.07	18	
Sep	25.80	774	4.96	143	
Oct	21.40	664	3.97	12	
Nov	16.90	508	3.00	\$9.5	
Dec	12.10	374	2.08	64.5	
Yearly average	23.4	712	4.40	13-	
Total for year		8540		1610	

Fig. 6. PV solar system productivity simulation

The yield of hydrogen at home is realized through electrolyser powered entirely by PV system with rated power consumption of 3.5 kWh. Electrolyser is based on the PEMFC (polymer-electrolyte) technology and splits water by hydrogen and oxygen [2]. Hydrogen, produced in the process is fed to a compressor pressure line, where its pressure raises to 450 bar. Pressurized gas is stored in cascade arranged pressure tanks, the container having the least pressure is filled first. The estimated production of hydrogen is 2000 l./h. With duty cicle of 10 h the quantity will be enough to power the fuel cell for 12-14 h at constant full power. Heat recovery will be implemented from the electrolysis unit to the residential unit for boiler water and space heating in common areas. The electrolysis unit is assumed to be 65% efficient, where the waste is primarily in the form of heat. This heat will offset the amount electricity required for space heating during the fall/winter where base heating is still needed, but not a large amount is needed. In this instance, heat recovery was considered for space heating displaces for 15.1% of the required amount of electricity a year. Another advantage of hydrogen system is that if there is an excess of hydrogen it can be used as supplement fuel for hybrid vehicle. In this way a further reduction in utility (gas) bills will be accomplished.

Selected fuel cell is based on PEM (polymer-electrolyte) technology and has a rated power of 3 kW. Hydrogen consumption is 2500 l. / h. at peak power. A duty cycle of 12 hours a day is assumed for which 8 000 liters of hydrogen are needed. Fuel cell function is to maintain the electrical loads of the house at night and provide up to 140 l. /24h. domestic hot water.

Rapid start-up of the system allows use in times of peak demand.

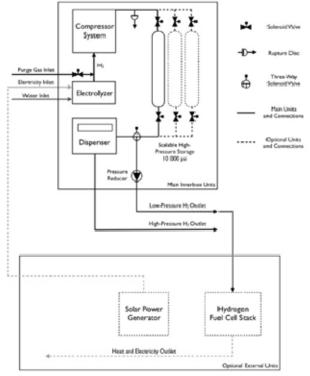


Fig. 7. Combined Solar-Hydrogen system diagram

V. SAFETY ANALYSIS

For the purposes of this analysis, the hydrogen system was broken down into its constituents and the possible types of failure that each could experience were listed, along with likely causes and possible effects.

Effects were rated for severity (S) on a scale of 1 to 10 where 1 is minimal and 10 could potentially cause injury or death. Causes were ranked based on likelihood of occurrence (O) on a scale of 1 to 10 where 1 is remote and 10 is certain. The severity and occurrence scores are then multiplied to form a criticality number (CRIT), which reflect the magnitude of identified risks. Since the goal of this preliminary analysis was to identify those risks for which controls and procedures must be developed or implemented, detection ratings for such controls and procedures have not been assessed here.

All of these failure modes could potentially result in fire, explosion, suffocation of an individual, or some combination of the three, as the components involved deal with compressed gas, in most places flammable hydrogen, and most of these components are located indoors. The objective of the safety measures described below will be to avert or mitigate these contingencies.

TABLE 2. PRELIMINARY FAILURE MODES AND EFFECTS ANALYSIS

Function	Potential Failure Mode	Potential Failure Effects	s	Potential Causes of Failure	0	CR
	Electrolysis not taking place while unit operates	lack of product		Loss of power; water leakage; low water flow	5	10
	Oxygen accumulation	rupture; fire		blockage of vent	2	2
Electrolysis	Water Purification Failure	e residue build-up		high impurity levels	3	3
	Electrolyte Leak	injury	8	mechanical failure	1	1
	Hydrogen gas leak	suffocation; fire 10 mechanical failure		1	1	
	Oxygen gas leak	suffocation; fire	8	mechanical failure	1	1
	Overpressure	explosion; leak; suffocation; fire	10	failure of downstream valve; failure to remove a downstream blind; leakage on suction side	3	3
Primary Compression	High Temperature	explosion; leak; suffocation; fire	10	failure of lubrication system; failure of cooling system	1	1
	Low Flow	leak; suffocation; fire	10	reduced flow	1	1
	Reverse Flow	leak; suffocation; fire	10	high discharge side pressure	1	1
	Overspeed	leak; suffocation; fire	10	speed control system failure	1	
	Loss of Containment	suffocation; fire	10	operation at fraction of capacity	1	1
	Overpressure	explosion; fire; suffocation	10	excessive fill rate; ignition; external fire; obstructed vent; (excessive heat input); ambient temperature change	3	1
Hydrogen	Underpressure	implosion; fire; suffocation	10	obstructed vent; excessive withdrawal rate; ambient temperature change;	1	;
Storage	High Temperature		10	external fire	3	1
	High External Liquid Level	implosion; fire; suffocation	10	flooding	3	
	Overfill		10	level control failure; uncontrolled inflow	3	1
	Low Level	implosion; fire; suffocation	10	level control failure; uncontrolled outflow	3	
Booster	Overpressure	explosion; leak; suffocation; fire	10	failure of downstream valve; failure to remove a downstream blind; leakage on suction side	3	3
	High Temperature	explosion; leak; suffocation; fire	10	failure of lubrication system; failure of cooling system	1	1
Compression	Low Flow	leak; suffocation; fire	10	reduced flow	1	
	Reverse Flow	leak; suffocation; fire	10	high discharge side pressure	1	,
	Overspeed	leak; suffocation; fire	10	speed control system failure	1	
- F	Loss of Containment	suffocation; fire	10	operation at fraction of capacity	1	

VI. ENVIRONMENTAL ANALYSIS

Combined Solar-Hydrogen system uses only water as a feedstock for hydrogen production which is much more environmentally friendly than using natural gas. Oxygen as a only byproduct is a vital part of the atmosphere and doesn't pose any ecological threat. Also the installation processes do not emit hazardous elements into the environment (in addition, all system components are encapsulated within the shell, which further reduces the impact on the environment due to corrosion). Thus the main influence is the use of electricity to power the plant. Since the installation supports modularity, implying additional alternative energy sources (solar panels) will provide a zero negative impact.

VII. ECONOMIC ANALYSIS

An important aspect of the policies in energy sector is to promote the use of renewable energy sources (RES). Optimal use of energy resources provided by the RES is a tool for achieving sustainable energy development and to minimize the adverse environmental impacts of activities in the energy sector.

Procedure "Energy efficiency and green economy" is implemented in the framework of the Operational Program "Development of the Competitiveness of the Bulgarian Economy" 2007-2013, funded by the European Union through the European Regional Development Fund (grants up to 50%) and the European Bank for Reconstruction and Development (credit resources - for the rest of the investment). Additional investment needed to build the energy system amounts to 117235 lv. In 40% gratuitous funding from the state, the investment cuts down to 70340lv. This is less than the usual price for a hybrid vehicles. Total energy consumption of the house is provided by clean sources, which, annually saves up to 26 tons emissions.

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STUDY OF THE ELECTRICAL PROPERTIES OF CNTFETS BASED ON COMPUTER SIMULATIONS

Angel Iliev Pashev, Dobromir Georgiev Gaydazhiev, George Vasilev Angelov and Ivan Stefanov Uzunov

Abstract – The paper reviews two approximations for energy level calculation based on the tight-binding model. Basic static and dynamic characteristics of CNTFET with doped source/drain area are performed using the Stanford University CNTFET model. The dependence of the output characteristics from the device geometry is given. An estimation of the transit frequency shows that the device can operate in the multi-GHz range.

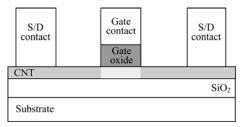
Keywords – Carbon nanotubes (CNT), graphene, CNTFET, device modeling, tight-binding model.

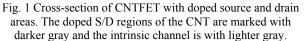
I. INTRODUCTION

The physical limit of the CMOS technology scaling is expected to be reached in the next 5-10 years. Increasingly more efforts are targeted at development of alternative electronic devices, to allow further frequency increase and power consumption reduction in the semiconductor technologies that will follow the 7 nm node [1]. Among the most promising novel devices are carbon based transistors in which graphene or carbon nanotubes (CNT) are used to form the channel region. Different types of carbon electronic devices have been reported in the literature back-gate or top-gate graphene FETs, CNTFET using Schottky barrier formed at the CNT - Drain/Source metal contact interface [2], top-gate CNTFET with doped D/S area and others [3]. Those devices benefit from the extremely high electron mobility and nearly ballistic transport to achieve very high speed and low power consumption, but still pose technological challenges that have to be overcome before they can move out of the laboratories into the production plants. The main technology issues are related to overcoming the high contact resistance at the interface between the carbon and most metals, selective removal of conducting CNTs and achieving good on/off current ratio.

In this paper an overview of the CNTFET devices and their models is presented. The models are used to analyze the basic static and dynamic characteristics of CNTFETs with doped source and drain regions (Fig.1). This structure is very similar to the planar CMOS FETs, thus it is possible to use many of the existing semiconductor processes in the device production. It inherits all the advantages of CNT electrical properties and has good on/off ratio [4], but also suffers from some of the common issues – high contact resistance and the need to selectively remove the conducting CNTs.

Most of the results reported here are obtained by simulations using the Verilog-A implementation of the Stanford University CNFET model reported in [5] and [6] or by theoretical analysis and custom Matlab code for calculations. The molecule structure, energy levels and other electrical properties of the carbon nanotubes are reviewed in the first section of the paper. The second section investigates the static characteristics of the CNTFET from Fig. 1 and their dependence on the CNT geometry. The influence of the different parasitic capacitances on the device speed is analyzed in the third section.





II. MODELING OF ELECTRICAL PROPERTIES OF CARBON NANOTUBES

Electrical behavior of the carbon nanotubes can be explained by reviewing the atomic structure and energy diagram of graphene –its building material. In essence, graphene is a single layer of graphite. It is a single atomic layer crystalline carbon with a hexagonal atomic lattice. The crystal lattice of this material and its Brillouin zone are shown in Fig. 2 (a) and (b) respectively. The valence and conducting bands of graphene touch at 6 points (marked with black dots on Fig. 2 (b)) throughout its Brillouin zone, zeroing the bandgap. In all other points, there is a gap between the energy bands. This defines graphene as a *"zero-bandgap"* semiconductor [7]. It has very high electron mobility which may exceed 15000 cm²/Vs. In comparison, the electron mobility of silicon at room temperature is around 1400 cm²/Vs [8].

Carbon nanotube is actually a hollow cylinder made of rolled up piece of graphene. The tube may have very different electrical properties depending on the angle at which the piece of graphene that makes it up is "cut". This angle is described by the chirality vector C(n,m), illustrated on Fig. 2 (a). In a planar sheet, the three carbon-carbon (C-C) covalent bonds for each atom are at 120° of each other. When a tube is rolled up, the angles between the bonds

I. Uzunov, Ph.D., A. Pashev and D. Gaydazhiev are with the Microelectronics and Nanoelectronics Technologies Department of Smartcom Bulgaria AD, 133 Tzarigradsko Chaussee blvd., 1784 Sofia, Bulgaria, e-mail: angel_pashev@smartcom.bg

G. Angelov, Ph.D. is Associate Professor with the Department of Microelectronics, ECAD Laboratory, FETT, Technical University of Sofia, 8 Kl. Ohridski blvd, 1797 Sofia, Bulgaria, email: gva@ecad.tu-sofia.bg

change, which leads to change in the allowed energy levels. The energy structure of a CNT is obtained by quantizing the energy structure of graphene (Fig. 2 (b)). The quantized levels can be expressed theoretically using the tight-binding model [7]:

$$E(k) = \pm \gamma \left[1 + 4\cos\left(\frac{3C_{x}ka}{2C} - \frac{3\pi paC_{y}}{C^{2}}\right)\cos\left(\frac{\sqrt{3}C_{y}ka}{2C} + \frac{\sqrt{3}\pi paC_{x}}{C^{2}}\right) + 4\cos^{2}\left(\frac{\sqrt{3}C_{y}ka}{2C} + \frac{\sqrt{3}\pi paCx}{C^{2}}\right) \right]^{1/2}$$
(1)

where k is the wave vector in the axial direction, p is the quantized wavevector in circumferential direction, $\gamma \approx 3.03 \text{eV}$ is the C-C covalent bond energy, $C_x = a(\sqrt{3}n + (\sqrt{3}/2)m)$, $C_y = a(3/2)m$ and the length of the covalent C-C bond a=0.142 nm.

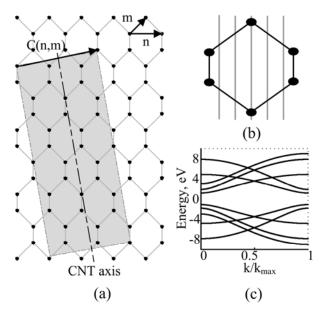


Fig. 2 (a) Carbon nanotube with chirality vector C(2, 1) overlaid on graphene atomic lattice; (b) Graphene Brillouin zone and CNT discretization lines; (c) Energy levels of a C(5,0) CNT calculated by the tight-binding model approximation.

The chiralities for which the quantization lines pass through the zero bandgap points of graphene yield conducting (metallic) CNTs. When the quantization lines do not pass through the zero bandgap points – the tubes are semiconducting. A CNTFET has to have only semiconducting tubes to achieve good on/off current ratio. In this article only FETs with semiconducting nanotubes are analyzed.

Expression (1) is used to create Matlab code calculating the energy levels and bandgap values of carbon nanotubes with different chiralities. A sample energy diagram for CNT with C(5,0) is shown in Fig. 2 (c). This is a semiconducting tube with energy gap between the highest valence and lowest conduction level of ~2.29 eV. This model can be used to calculate the energy levels of any CNT with high accuracy, but this approach is calculation intensive. If applied to simulate the behavior of larger CNTFET circuits, it will require a lot of processing power and the analysis runtimes will increase proportionally to the circuit complexity. For this reason a simplified approximation of the tight-binding model has to be used for circuit simulators targeted at larger circuits, i.e. Stanford CNTFET model [5], [6], PTM model [8]. Apart from precisely modeling the energy levels of the CNT, a number of other effects have to be taken into account to achieve accurate device model – scattering mechanisms in the intrinsic channel and S/D areas, band to band tunneling, Schottky resistance on the CNT-metal contact interface, parasitic capacitances etc.

A Verilog-A implementation of the model developed by Stanford University [5], [6] is used in this paper to analyze the static and dynamic characteristics of CNTFETs with different chiralities. The model includes the effects mentioned above and is computationally optimized to allow simulation of large circuits. It uses an approximation of the tight-binding model. The diameter of the tube is calculated by the following formula:

$$d = \frac{\sqrt{3}a}{\pi} \sqrt{n^2 + nm + m^2} , \qquad (2)$$

where a = 1.42 Å is the length of C-C covalent bond and C(n,m) is the chirality vector.

In order to calculate the energy levels the CNT is quantized in its circumferential and axial directions. The energy levels are calculated by the following approximation [5], [6].

$$k_p = \frac{2\pi}{a\sqrt{n^2 + nm + m^2}}\lambda, \qquad (3)$$

$$k_l = \frac{2\pi}{L_g} l$$
, $l = 1, 2, 3...$, (4)

$$E_{p,l} \approx \frac{\sqrt{3}}{2} a V_{\pi} \sqrt{k_{p}^{2} + k_{l}^{2}} \quad , \tag{5}$$

where k_p and k_l are the quantized levels in axial and circumferential directions respectively. The parameter λ is equal to the index *p* for metallic and to $(6p-3-(-1)^p)$ for semiconducting tubes, L_g is the gate length and $V_{\pi} = 3.033$ eV is the C-C covalent bond energy.

III. DC CHARACTERISTICS OF CNTFETS WITH DIFFERENT CHIRALITIES

The model uses only the first two k_p and ten k_1 values, since for voltages up to 1 V for typical devices (d < 3 nm, $L_g < 100$ nm), only these values have significant effect on the current [5], [6]. From (3) and (5) it is obvious that tubes with equal diameter yield identical energy levels. In reality, there are tubes with different chirality and equal diameters that have different energy levels and energy gap (E_g). For example if (1) is used to calculate the energy gaps of tubes with chirality C(5,3) and C(7,0), which have equal diameters of 0.548 nm, the result is respectively 1.566 eV and 1.482 eV. But equation (5) will result in energy gap of 1.556 eV for both tubes. Evidently, the simpler expression (5) should be used in cases where moderate accuracy is needed, while (1) is for the cases when high precision is needed.

The Stanford model is used to simulate the input and output characteristic of the CNT transistor from Fig. 1. To be able to compare the CNTFET performance to planar MOSFETs, the geometry of the transistor in all simulations is taken to be similar to the geometry of the modern planar MOSFETs – gate length $L_g = 32$ nm, gate oxide thickness $t_{ox} = 4$ nm, gate oxide permittivity $\varepsilon_{ox} = 15$. CNTFETs with single nanotube under the gate are used for the sake of

simplicity. The channel resistance is governed primarily by the diameter and the number of CNTs, so the gate width is not a crucial parameter for the static behavior of this transistor. However, it defines the gate parasitic capacitances and will be taken into account when reviewing the dynamic behavior in the next section of the article.

The output characteristics of two transistors with different chiralities are compared in Fig. 3. They closely resemble the output characteristics of a planar MOSFET, despite the fact that the physical principles defining both regions of the characteristic (linear and saturation) are different. The chirality vector defines the nanotube circumference and in practice, it is equivalent to the channel width of planar MOSFETs, defining the channel resistance and the maximum current that can flow through the tube. This is illustrated in Fig. 4, where the drain currents of tubes with different chiralities are compared. In fact, the dependence of the drain current from the CNT circumference, respectively CNT diameter. is approximately linear for constant gate voltages (Fig. 5). These dependencies are numerically illustrated in Table 1 where the bandgap values are also given.

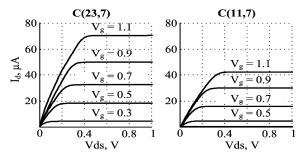


Fig. 3 Family of output characteristics of CNTFETs with C(23,7) and C(11,7).

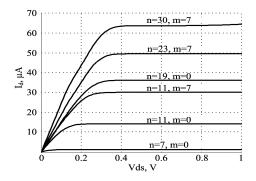


Fig. 4 Output characteristics of CNTFETs with different chiralities at $V_{ss} = 0.9$ V.

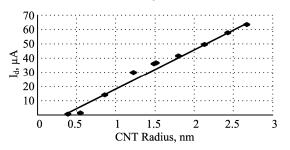


Fig. 5 The dependence of the drain current from the CNT diameter. The drain current is at V_{gs} =0.9 and V_{ds} =0.6.

Table 1 also shows that the energy gap decreases with the increase of CNT diameter. This is explained by the fact that when increasing the diameter the tube gets more atoms and hence gets more available energy levels. Statistically there is a bigger chance to have closer energy levels, resulting in lower energy gap. This is confirmed also by the transfer characteristics in Fig. 6. The lower energy gap results in lower threshold voltage V_{th} at fixed V_{gs} and V_{ds} , which leads to higher drain currents.

TABLE 1. CNTFET STATIC PARAMETERS FOR DIFFERENT CHIRALITIES. THE DRAIN CURRENT IS AT $V_{\rm GS}{=}0.9$ and $V_{\rm DS}{=}0.6.$

Chiral	ity	Diamete	Current	Eg, eV
n	m	r, nm	, μA	
5	0	0.392	0.470	2.292
7	0	0.548	1.257	1.482
11	0	0.861	13.965	1.015
11	7	1.231	30.036	0.686
19	0	1.488	36.137	0.563
15	7	1.524	36.750	0.563
23	0	1.801	41.660	0.479
23	7	2.129	49.650	0.397
27	7	2.435	57.900	0.353
30	7	2.666	63.639	0.322

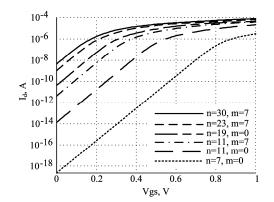


Fig. 6 Transfer characteristics of CNTFETs with different chiralities at $V_{ds} = 0.9V$

IV. STUDYING OF THE DYNAMIC CNTFET PROPERTIES

Two basic factors determine the dynamic performance of the transistor – the intrinsic channel propagation time and the delay caused by the parasitic capacitances. The channel propagation delay is basically defined by the carrier mobility. The parasitic capacitances are illustrated in Fig. 7 and they are as follows: C_{g-CNT} is the intrinsic gate to channel capacitance, C_{g-sd} are the parasitic capacitances from the gate contact to the dopes source/drain area, C_{g-sub} is the capacitance between the gate and substrate (backgate), $C_{CNT-sub}$ is from the CNT to substrate and C_{g-cont} represents the capacitances between the gate and source/drain contacts.

The dynamic properties are studied by a frequently employed approach of simulating a waveform of an inverter-type ring oscillator (RO). The RO inverters are using identical N-type and P-type CNTFETs with $L_g = 32$ nm, $t_{ox} = 4$ nm, $\varepsilon_{ox} = 15$, gate width w = 48 nm, gate height h = 64 nm and single CNT with C(19,0). The capacitance values are: $C_{g-CNT} = 4$ aF, $C_{g-sd} = 2$ aF, $C_{g-sub} = 1.4$ aF, $C_{g-cont} = 15$ aF. Since the SiO₂ layer is assumed to be 10 µm and the tube diameter is small, the $C_{CNT-sub}$ capacitance becomes less that 0.5 aF and can be neglected. Those values are given in [10] as typical for CNTFET with the geometry size listed above.

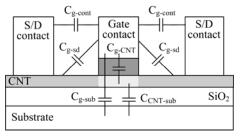


Fig. 7 Parasitic capacitances affecting the CNTFET dynamic performance.

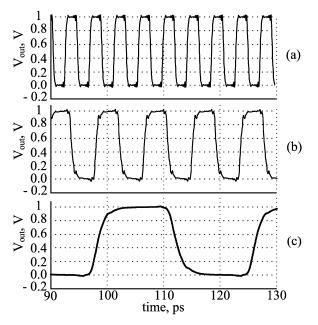


Fig. 8 Transient response of 7-stage ring oscillator circuit using CNTFETs. (a) without any parasitic capacitances, (b) C_{g-sub} and C_{g-sd} are added, (c) all parasitic capacitances from Fig. 7 are accounted for.

The output waveform is simulated at three different conditions: Fig. 8 (a) shows the effect only of the channel propagation delay; Fig. 8 (b) includes also the effects of C_{g-sub} and C_{g-sd} ; Fig. 8 (c) includes all parasitic capacitances. The parameters of the waveform (period and frequency of oscillation and delay of a single inverter stage) are summarized in Table 2. The first waveform actually gives the theoretical limit of the device. The extremely high carrier mobility results in a very high transit frequency of 1.61 THz (1/stage delay). It is reduced to 820 GHz by C_{g-sub} and C_{g-sd} and further to 251 GHz when the effect of C_{g-cont} is taken into account. Even after including the parasitic capacitances, the transit frequencies are still impressive and demonstrate the big potential of those devices.

TABLE 2. RING OSCILLATOR DYNAMIC PERFORMANCE SUMMARY.

Waveform	Period,	Freq,	Stage
	ps	GHz	delay, ps
Fig. 8 (a)	4.32	231.71	0.62
Fig. 8 (b)	8.54	117,05	1.22
Fig. 8 (c)	27,96	35,76	3.99

V. CONCLUSION

Some basic properties of the CNTFET devices are investigated by simulations and theoretical analysis. The calculation of the energy bands based on the tight-binding model is discussed and two different approximations are examined. The dependence of the energy levels from the geometry of the nanotubes is reviewed. The parallel between the static characteristics of CNTFETs and planar CMOS transistors is articulated and their similarity is noted. The dependence of those characteristics on device geometry is investigated. Time domain simulation gives an estimation of the dynamic properties of the CNTFET and confirms its suitability for multi-GHz operation.

ACKNOWLEDGEMENT

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Investigation of Radial and Axial Plasma Potential Distribution in Plasma Chemistry Prototype Reactor

Mladen Boykov Mitov, Valentin Hristov Videkov, Tsviatko Krastev Popov and Miglena Dimitrova Dimitrova

Abstract – Prototype of cylindrical plasma chemistry reactor with sectional cathode and common anode have been designed and built. The main goal of the proposed construction is to achieve and investigate uniform radial distribution of the plasma parameters. In order to perform diagnostics have been designed and built computerized electronic Langmuir probe system. First results of radial and axial plasma potential measurements have been performed and presented in this work.

Keywords – Plasma diagnostics, Plasma potential, Langmuir probe, Plasma Chemistry reactor

I. INTRODUCTION

Gas discharges are widely used in many different contemporary technologies such as plasma chemistry etching, plasma polymerization, thin layer dielectric deposition, etc [1, 2]. In order to proceed samples with large diameter, uniform plasma in radial direction is required in technological devices.

One of the main plasma parameters is the plasma potential i.e. the potential of the plasma in particular point of the plasma volume. Langmuir probes [3, 4] are less expensive than other types of plasma diagnostic tools, that's why, they are widely used for gas discharge plasma diagnostics.

Langmuir probe is thin metal wire with diameter up to few hundred micrometers and a length of few millimeters. The probe is usually biased from 0 to large negative potentials and the corresponding probe current is being registered. The result is the so called Langmuir probe current – voltage (I-V) characteristics. Example of such I-V is presented in figure 1 [5].

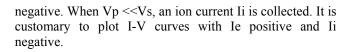
Let the plasma potential (space potential) be Vs, and the potential applied to the probe be Vp. When $Vp \gg Vs$, an electron current Ie is collected; the probe current is

M. Mitov is with the Department of Microelectronics, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: m_mitov@tu-sofia.bg

V. Videkov is with the Department of Microelectronics, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: videkov@tu-sofia.bg

Tsv. Popov is with the Faculty of Physics, Sofia University "St. Kl. Ohridski" 5, J. Bourchier Blvd., 1164 Sofia, Bulgaria, e-mail: tpopov@phys.uni-sofia.bg

M. Dimitrova is with Institute of Plasma Physics, Academy of Sciences of the Czech Republic v.v.i., Za Slovankou 3, 182 00 Prague 8, CR, e-mail: miglena.dimitrova@gmail.com



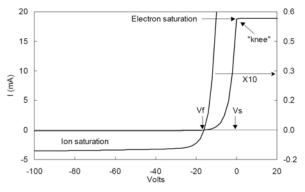


Fig. 1. An idealized I-V curve. The left curve is expanded 10X to show the ion current.

The space potential Vs (set in the figure as zero) is near the "knee" of the curve. At the far left, where all the electrons have been repelled, we have the Ion Saturation current, Isat. The Floating Potential Vf, is where the ion and electron currents are equal, and the net current is zero. In the Transition Region, the ion current is negligible, and the electrons are partially repelled by the negative potential Vp–Vs. In a Maxwellian plasma, this part of the curve is exponential. When Vp (or just V) reaches Vs, all of the random thermal flux of electrons is collected. In the Electron Saturation region, Ie grows only slowly because of the expansion of the sheath. From the I-V curve, the plasma density n, electron temperature KTe, and plasma potential Vs can be determined, but not the ion temperature. The floating potential is negatively shifted in regard to the plasma potential by a value of 3KTe

From the short explanation above is clear, that when the floating potential distribution in radial direction in cylindrical plasma is uniform, we will have uniform distribution in radial direction of the main plasma parameters.

II. EXPERIMENTAL SETUP

For the investigation of the plasma parameters, prototype of cylindrical plasma chemistry reactor with sectional cathode and common anode has been designed and built. The picture of the reactor in working condition is presented in figure 2.

The reactor consists of glass discharge tube with internal diameter of 75mm and length of 160mm. The cathode

consists of seven sections. Every part of the cathode is connected to the high voltage supply trough a ballast resistor with resistance of $5k\Omega$ / 50W. The reactor is connected to the rest of the vacuum installation with copper pipes trough the aluminum flanges. The probe and the anode are inserted in the reactor trough specially designed orifices, that allow their movement (anode can move in axial direction, the probe can move in axial and radial direction).

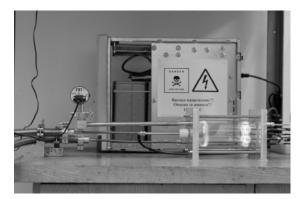


Fig. 2a. Reactor in working condition



Fig. 2b. Reactor in working condition

The power supply of the reactor can be regulated from 0 to 1500V DC with maximum output current of 300mA.

In order to perform diagnostics, has been designed and built computerized electronic Langmuir probe system. The system provides us with ability to measure floating potential, I-V characteristics and also electron energy distribution function by second harmonic method [6]. Block diagram of the probe system is presented in figure 3.

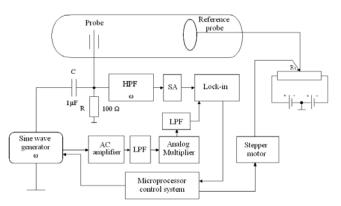


Fig. 3. Block diagram of the probe system.

Trough the capacitor C, on the probe is applied modulating signal with frequency $\omega = 768$ Hz, generated from DDS sine wave generator, controlled by the microprocessor system. On the resistor R (R =100 Ω / 0,1%) is formed voltage drop with the necessary amplitude for modulation. This resistor is also used for registering the amplitude of the current with frequency of 2ω in the probe circuit. Selective amplifier and Lock-in amplifier select from the probe signal only the part that is proportional to $I_{2\omega}$. The high pass filter with corner frequency ω helps to improve the quality of the signal. The output of the selective amplifier is connected to the input of the Lock-in amplifier.

The frequency doubling is managed trough a separate device (using analog multiplier). The signal from the output of the frequency doubler, is applied to the reference input of the Lock-in amplifier trough a low pass filter.

The potential of the reference probe is driven by a high power potentiometer with low resistance (R_1) . The potentiometer is driven by a stepping motor which is controlled by the microprocessor system.

The microprocessor system can work as a standalone device, or can be connected to a PC, which expands the features of the whole system.

III. EXPERIMENTAL RESULTS

The first measurements with this system were performed in different axial and radial positions of the plasma volume. They were divided in two groups – measurements held with sectional cathode, and measurements held with only the central section of the cathode (single cathode measurements). This was done to show the advantages of the sectional cathode. After processing the experimental data, from the I-V characteristics, the floating potential in every point of measurement has been obtained. The results are presented in the tables below. Table 1 presents the results for the measurements with single cathode and table 2 presents the measurements with the sectional cathode. The measurements have been done in 3 points of the axial direction. If we name these points P_1 , P_2 and P_3 , than the distance from this points to the cathode is as follows:

\mathbf{P}_1	=	85	mm

$P_2 = 65 \text{ mm}$

$P_3 = 50 \text{ mm}$

The measurements have been held with discharge current of 30 mA, chamber pressure of 1,12 mbar in argon and Langmuir probe with diameter 75μ m and length 5 mm.

TABLE 1. RESULTS FROM MEASUREMENTS WITH SINGLE CATHODE

Distance from	Floating potential [V]		
the axis of the	P ₁	P ₂	P ₃
reactor [mm]			
-28.3	2.9	1.4	0.9
-7.1	3.5	2.4	2.2
0	3.7	2.7	2.4
7.1	3.4	2.4	2.1
28.3	2.8	1.3	0.4

Distance from	Floating potential [V]		
the axis of the	P_1	P_2	P ₃
reactor [mm]			
-28.3	12.5	16.7	17.7
-7.1	13.3	19.1	20
0	13.5	19.2	20.2
7.1	13.2	19.1	20
28.3	12	16.4	17.3

TABLE 2. RESULTS FROM MEASUREMENTS WITH SECTIONAL CATHODE

The results from tables 1 and 2 are presented also in figures 4 and 5.

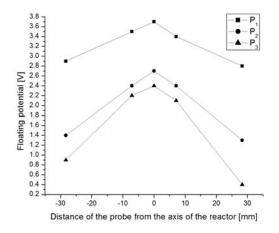


Fig. 4. Results from measurements with single cathode

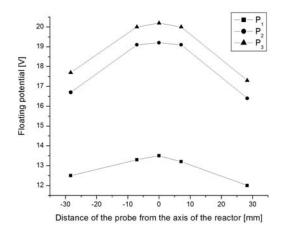


Fig. 5. Results from measurements with sectional cathode

IV. CONCLUSION

From figures 4 and 5 it is clear that the main goal of the reactor design is achieved. The floating potential distribution i.e. the plasma potential distribution with sectional cathode is uniform, over the cathode area, in radial direction. Moving the probe close to the walls of the reactor, the floating potential drops, which was expected. Yet, there are to be performed measurements in different gases and in particular oxygen, using different methods for approximation of plasma parameters, in order to collect

data, which after processing, in future will help us for optimization of technological processes.

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Space Reconnaissance. System for Space Control

Petar Radenkov Stoyanov, Dimcho Yordanov Dimov and Darin Mihaylov Mihov

Abstract – The article justified the need for the space countries to monitor space is explained. Sources for open information of the orbital characteristics of satellites are given. The main tasks for control of space as a specific sort of intelligence activities are defined. A structural schematic for a System of control of space is proposed. The composition, functions and correlation of laser-optical and radar complexes and the means for calculation and management are thoroughly described.

Keywords – space control, laser-optical, radar, space technologies

I. INTRODUCTION

Every space country that wants to safeguard its status in the scientific and the defensive meanings reaches the understanding of the necessity to monitor space. Space objects have already been well categorized, they are available for systematic surveillance and due to that it is possible for them to be explored with details and independently. A base for these explorations is the trajectory characteristics of satellites. Dividing space apparatuses by height, incline and eccentricity of their orbits we can determine the point of launch and the type of purposes for each of the defined classes of satellites. The features of each of the targeted groups (parameters of orbit, the quantity and location of apparatuses functioning at the same time, time periods of functionality and characteristics of the ending of their functioning) can later be compared to features that satellite systems must have for resolving issues for both civilian and military purposes.

Open sources for the orbital characteristics of soviet satellites were mostly the official messages of the telegraphic agency of the Soviet Union - TASS (now for Russian satellites - the messages of information and telegraphic agency of Russia – ITAR-TASS) for their launches into orbit. These messages contain the parameters of the initial orbit of every satellite - period of rotation, incline, height of the apogee and perigee and since 1988 the type of the booster.

Also the united system of air and space defense of USA and Canada, as the analogous Russian system, while monitoring all objects in around Earth space publishes some of its data to the open media. Tables with the so called "two-lined orbital elements" are made public trough the Center for space flight, belonging to NASA and they are also weekly published in the World Wide Web.

P. Stoyanov is Assoc. Prof. Dr. in Space Research and Technology Institute - Bulgarian Academy of Sciences, Bl.1 Acad. Bonchev str., 1113 Sofia, Bulgaria, e-mail: pstoyanov@abv.bg

D. Dimov is Surveillance Expert in Bulgarian Air Traffic Services Authority – 1, Brussels blvd., 1540 Sofia, Bulgaria, e-mail: dimcho.dimov@bulatsa.com

D. Mihov is Student in University of Edinburgh, School of Informatics – Appleton Tower 11 Crichton str. EH8 9LE Edinburgh, UK, e-mail: dmmihov@gmail.com Analogous summaries for orbital elements of the artificial satellites are weekly published by the Royal astronomical institute in the United Kingdom that uses a web of stations for optical monitoring.

The tables of NASA and the British astronomical institute both contain more details than messages from ITAR-TASS and their constant renewal allows us to monitor the maneuverings of the satellites in orbit. Optical monitoring allows us to see not only the orbital parameters, but also to evaluate the size of the apparatus using its visible reflection and depending on its reflection, time and angle the sunlight is falling we can estimate its shape and orientation.

Data for the actions of satellites in the radio wavelengths is published by the so called "Katarian" group for monitoring, which is a non-formal group for people, whose hobby is radio monitoring from different countries, listening to and analyzing signals from different satellites.

Results from the pre-made analysis for the already mentioned sources is weekly published in periodical magazines - "Flight International", "Spaceflight" "Novosti Kosmonavtiki" and others. In the tables published we can find the international registry number, point of launch and general purpose of every space apparatus and also the type of the booster rocket. Often are published the orbital elements as well as the messages for the natural or deliberate bringing of the satellite out of orbit.

More detailed data specially made for the space programs of different countries is yearly published by independent experts from USA, Russia, the United Kingdom and others and every five years by the exploration services of the United States Congress.

It must be noted that all of the above sources are based on open non-secret information.

And this information proves to be enough to identify the launch of space systems and its analysis allows for the making of the characteristics and scale of civil and military space programs for different countries without jeopardizing national security.

This information though is severely less than the data needed to create a full picture of space. This is why all major space countries use their own national technological means for exploratory activities and reconnaissance of space. This can be accomplished by the creation of a System for control over space.

A. Structure and characteristics of the System for Space control.

Control over space is a specific kind of intelligence activity that includes the solving of a few main tasks:

- finding space objects;
- defining their space characteristics;
- recognition of the objects.

This control begins with the systematic monitoring of the hemisphere, finding space objects and defining their trajectory parameters. After this they are photographed or receiving of optical images which allow defining the appearance and parameters of motion around the center of mass. The next stage of control is defining and categorizing of the reflection characteristics of the space object in the decimeter, centimeter and optic band. In the final stage is recognizing the object, defining its purpose, belonging and technical characteristics.

The structural schematic of such a System for space control is shown on Figure 1.

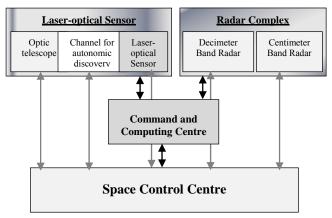


Fig. 1. The structural schematic of Space Control Center.

From the schematic we can see that the System for control of space is composed of:

- a laser-optical component;
- a radio lactation component;
- means of calculation and management.





Fig. 2. Optical telescope of the laser-optical component.

The laser-optical component is placed at great heights as a rule, usually at a mountaintop where the atmosphere is much cleaner and nights with a clear cloudless sky exceed the ones in the valleys.

The main tool of the laser-optical component is the optic telescope with a precisely pointed blende (figure 2). It is situated in a tower with an open roof during working times.

Precisely this telescope working in as an optic-electric system allows us to receive images of space objects as a

reflection of the sunlight. The surveillance of the space object with the telescope secures the receiving of information to recreate the target's orbit. After computer analysis the data are collected by the Space Control Center (SCC).

The optical telescope is controlled by a program created in advance and monitors objects previously selected by the SCC. This means that it tracks already discovered and familiar objects in space.

Other than the big telescope in the laser-optical component is also situated the apparatus for the passive Chanel for autonomous discovery of space objects. The optic means respond automatically to the appearance of unfamiliar objects in the sky, they define their characteristics and compare them with the catalogue for space objects. Besides this if necessary the means of this channel free the optical telescope when too many targets are requested for monitoring.

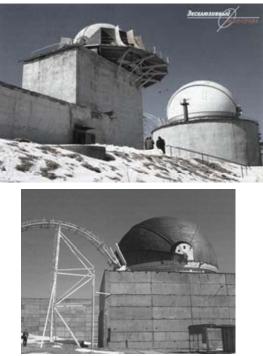


Fig. 3. Optical telescope (above) and passive channel for automatic discovery (down).

The apparatus of the passive channel for automatic discovery automatically processes the received information and sends it to SCC.

A main disadvantage in the described optic means is the barriers cause by the characteristics of the weather and the daylight. They can only work night times with no clouds.

This disadvantage can be compensated by the laseroptical locator. Unlike the passive channel that processes the reflected by object sunlight the active channel beams its own laser and receives and processes the reflected by it signal.

The zone of effect of the laser-optical locator is the upper hemisphere, limited by a minimal angle of the position by 10° in passive mode and 30° in active mode.

This is how the laser-optical component gets optic coordinate and non-coordinate information with an extremely high information for the objects in space.



Fig. 4. Apparatus for the laser-optical locator.

Usually in a close proximity to the laser-optical component is situated the other main element for the System for control over space - the radar complex. It includes two types of radar stations - working in a decimeter and centimeter wavelengths. The area of effect of this component is the upper hemisphere and the radius of effect is around 3500 km.

The modern radar of the decimeter band includes a transmitting-receiving antenna grid that electronically scans the beam and aperture with size of 20x20 m (figure 5)

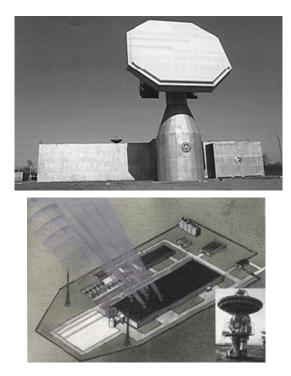


Fig. 5 Main plan and antennal system of the radar component.

Radar of the centimeter band usually includes a few (maximum 5) spinning parabolic antennas that work on the principles of the interferometer due to which the elements of the orbit of space objects is measured very precise.

The System for space control works by interactions from all channels in the given order. The radar of the decimeter band finds the object and measures its orbital characteristics. The data is used to point the radar in the centimeter band which precisely measures the position of the space object. In the meantime the data from the decimeter radar is transmitted to the passive channel for automatic discovery that defines the shape of the object with the reflected sunlight. In the end we get a picture of the object in all necessary bands.

The control of the laser-optical and radar apparatuses is done by the Command-computing center which is connected with the Center for Space Control where all the acquired information is transmitted to be analyzed and categorized. The Center maintains a computerized renewable catalogue of all objects in space, draws trajectories of movement, draws diagrams of their current position, future orbital routes and predicts times and general positions of important objects entering the Earth's atmosphere. Since 1957 more than 24000 space objects have been categorized many of which have entered and burned up in the Earth's atmosphere. It is estimated that there are currently around 8000 space objects in orbit that are being monitored by the Systems for space control.

By open source data the Russian System for control over space is situated at the top of the mountain Chipal near the station Zelenchukskaia in Karachevo - Cherkaska area. The analogous US center is in the mountain Cheyene, Colorado Springs, Colorado State.

II. CONCLUSION

The main general conclusions can be made:

- All powerful space countries build their own national Systems for control over space;
- Those Systems are composed of an elaborate complex of laser-optical and radar receivers and an electrically computing apparatuses for control and management. As a structure they are analogues to different countries with their differences being of technical and technological differences depending on the capabilities of the country;
- The Systems for control over space discover, define the parameters, recognize and monitor all space objects in orbit.

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The Impact of Resistor Mismatches and Op-amp Limited GBW on the Output Impedance of the Howland Current Source for EIT Applications

Ali Heidari, Mehran Zanganeh, Manoochehr Nahvi and Stoyan Nihtianov

Abstract - Electrical impedance tomography (EIT) has been the focus of many studies in recent years and has achieved significant progress in solving medical and industrial problems. An important part of most EIT systems is the current source, because its characteristics have considerable impact on the performance of the EIT systems. The most commonly used current sources in EIT is based on the Howland-topology implemented with discrete components. This paper presents a system level analysis of this type of AC current source for implementation in standard CMOS technology. Although the resistor mismatch and op-amp gainbandwidth product have significant impact on the performance of this type of current sources, we can hardly find any analytical analysis of these effects. Such analysis will be presented here. It will be shown that resistor mismatches of only 0.1% can cause the output impedance of the current source to drop down to 200 k Ω , with a current magnitude in the milliamp range. We shall also present a simple relation between the required minimum output impedance and the amplifier gain-bandwidth (GBW).

Keywords – AC current source, Gain-bandwidth, Resistor mismatches.

I. INTRODUCTION

EIT has gained considerable interest in medical and industrial applications due to its speed, simplicity and total cost [1]. This imaging technique produces impedance distribution maps, and images, using a set of peripheral measurements collected on the surface of the process under investigation, while geometrically different current patterns are passed through the subject. Figure 1 shows the general structure of an EIT system.

In an EIT system typically the electrodes are in electrical contact with the object, and alternating currents are applied to the electrodes based on a specific measurement strategy [2]. The resulting electrical potentials are measured, and the process may be repeated for various current patterns. The measurements collected by the hardware are then utilized by EIT software to reconstruct the tomography images.

An important part of most EIT systems is the current source, as its performance has a considerable impact on the measurement precision, and hence on the tomographic

S. Nihtianov and A. Heidary are with Technical University of Delft, The Netherlands. E-mail: s.nihtianov@tudelft.nl

images. The current source specifications vary among industrial and medical applications. In medical EIT the range of human tissues conductivity and also patient safety is a limiting factor for the design of the current source. In this case the generated current is typically with 0.1-5 mA amplitude for the load range of $100\Omega - 10k\Omega$ [1]. Typical values for industrial applications are given in [1]. In these applications, the current amplitude is much higher, for example 30mA, as reported in [3]. The current source is required to have stable characteristics over the desired load impedance range and a frequency range from about 100Hz up to 1 MHz.

We will show that resistor mismatches have significant effect on the output impedance of the Howland current source. As resistor trimming is very expensive in IC technology, we need to have complete analysis of its effect and to design the layout so that to meet the matching requirement. Another very important and challenging parameter to reach high output impedance of the current source is the gain-bandwidth (GBW) of the used op-amp. We will show a simple relation between the required minimum output impedance and the amplifier GBW.

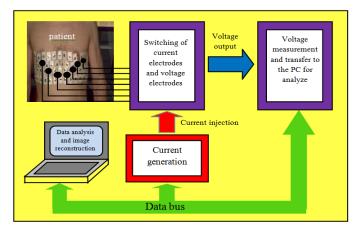


Fig. 1. A schematic of medical EIT with electrode array attached to the patient's body.

II. THE CURRENT SOURCE

Due to the influence of the current source performance on the quality of the measured data set and the reconstructed images in EIT systems, the current source is considered an important element. In EIT a current source with high accuracy and stability over both: the load impedance range and the frequency range, is highly desirable. The current source should have much higher

A.Heidary, M. Zanganeh and M. Nahvi are with Faculty of Engineering, Guilan University, Rasht, Iran. E-mail: a.heihari@tudelft.nl

output impedance with respect to the load in the whole desired frequency range. This is more crucial for the multi-frequency EIT [4,5] and wideband EIT system [6,7].

In general, there are two main types of current sources for EIT systems: voltage-controlled current sources, and supply current sensing current sources [1]. A Howlandbased current source, which is the focus of this paper, is of the former type.

Various factors can influence the output impedance, which will lead to current magnitude change. In this paper we will focus on the impact of resistor mismatches, amplifier limited gain and amplifier limited bandwidth. Since the final goal in this project is designing an integrated version of the current source, conducting a complete analysis of the current source is necessary. This is in contrast to discrete implementation where even after designing printed circuit board (PCB), it is still possible to amend the circuit and use resistors with fine tuning and other modifications.

III. HOWLAND CURRENT SOURCE

The most common current source architecture for an EIT system is the Howland topology [8]. A circuit diagram of a Howland current source is shown in Fig. 2. Assuming an ideal op-amp, the load current, I_L can be expressed by Eq. 1.

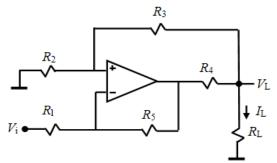


Fig. 2. Howland current source.

$$I_{L} = \frac{V_{L}(R_{2}R_{5} - R_{1}(R_{3} + R_{4}))}{R_{1}R_{4}(R_{2} + R_{3})} - \frac{V_{i}(R_{2}R_{5} + R_{3}R_{5})}{R_{1}R_{4}(R_{2} + R_{3})}$$
(1)

Since the circuit should be a current source, its load current should be independent of the load voltage. This means that the first term in (1) should be zero, which therefore leads to the following criterion:

$$R_2 R_5 = R_1 (R_3 + R_4) \tag{2}$$

With an ideal op-amp and the criterion given by (2), an infinite output impedance can be achieved. It is quite obvious that this is not achievable due to resistor mismatches and op-amp imperfections such as limited gain and limited bandwidth.

Another important factor which can cause significant current magnitude change in high frequencies is the parasitic capacitances parallel with the load resistance. These parasitic capacitances are formed by the electrodes applying currents through a medium for measurements purposes. The main part of such a capacitor can be removed by a general impedance convertor [8]. This subject will not be covered in this paper.

IV. CIRCUIT IMPERFECTIONS AND THEIR EFFECTS ON THE OUTPUT IMPEDANCE OF THE CURRENT SOURCE

In this section the impact of: resistor mismatches, limited gain of the amplifier, and finally the limited bandwidth on the current source output impedance, will be analytically expressed and analyzed. It must be noted that other non-idealities including noise, offset and electrode parasitic capacitances will not be given here.

a) Resistor mismatches

As it has been mentioned above, in order for the circuit shown in Fig. 2 to acts as a current source, it is necessary to meet the criterion expressed by Eq. 2. However, due to resistor mismatches, it is impossible to meet this equation. In a discrete implementation we may use a potentiometer to adjust the resistors value. However resistor trimming, for instance laser trimming, [9] is very expensive task in integrated circuit technology and therefore usually avoided.

$$R_{o} = \left(\frac{\partial I_{L}}{\partial V_{L}}\right)^{-1} = \frac{R_{1}R_{4}(R_{2} + R_{3})}{R_{2}R_{5} - R_{1}(R_{3} + R_{4})}$$
Using Eq.
1, the output
resistance can
be derived as:
(3)

Under Eq. 2 and an input voltage with magnitude of $V_{im}=1V$, to have a load current of $I_{Lm}=1mA$ the resistors in Fig. 2 must be selected as $R_1=R_3=R_4=R_5=1k\Omega$, $R_2=2k\Omega$.

For the purpose of calculating the impacts of the resistor mismatches, resistors are chosen randomly with a normal distribution with a mean and standard deviation equal to typical resistor values and mismatches, respectively. This can also be done with a circuit simulator such as Cadence in Monte-Carlo analysis. However, Monte-Carlo analysis is very time consuming.

Based on the design kit of 0.7 μ m standard CMOS technology, mismatches of 0.1% can be achieved by a high ohmic poly resistor in a very careful layout design while using a significantly large area. Under these restrictions the output resistance was calculated in Matlab for 10,000 samples and the resulting histogram is depicted in Fig. 3.

As can be seen from Fig. 3, in some samples the output resistance can be as small as $200k\Omega$ and approximately 10% of the samples have an output resistance lower than $500k\Omega$. This means that if an output impedance has to be greater than $500k\Omega$, at least 10% of the samples will not pass the test. Also, 13% of the samples have an output resistance larger than $5M\Omega$, which is not shown in the figure for clarity. An important conclusion here is that if low frequency output impedance larger than $500k\Omega$ is

required, then for having an yield larger than 90%, resistor trimming is unavoidable.

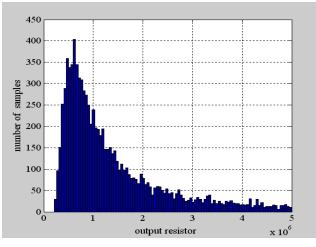


Fig.3. Output resistance histogram with circuit resistors mismatches of 0.1%

Based on Eq. 1 and Eq. 3, in Fig. 2 it is quite obvious that increasing the resistor value in the current source reduces the output current and increases the output resistance to the same extent.

b) Limited gain

Assuming limited op-amp gain for the Howland current source in Fig. 2, the load current can be determined as:

$$I_{L} = V_{L} \left(\frac{aR_{2}(R_{1}+R_{5}) - (R_{2}+R_{3})(R_{1}(1+a)+R_{5}) - R_{4}(R_{1}(1+a)+R_{5})}{R_{4}(R_{2}+R_{5})(R_{1}(1+a)+R_{5})} \right) - (4)$$

$$V_{i} \left(\frac{aR_{5}(R_{1}+R_{5})}{R_{4}(R_{1}+R_{5})(R_{1}(1+a)+R_{5})} \right)$$

Therefore the output impedance can be expressed as:

$$Z_{O} = \frac{R_{4}(R_{2} + R_{3})(R_{1}(1+a) + R_{5})}{aR_{2}(R_{1} + R_{5}) - (R_{2} + R_{3})(R_{1}(1+a) + R_{5}) - R_{4}(R_{1}(1+a) + R_{5})}$$
(5)

For the same condition stated by (2), $(R_1=R_3=R_4=R_5=1k\Omega, R_2=2k\Omega)$, the Eq. 5 can be simplified as below:

$$|Z_o| = \frac{3(|2+a|)}{8} K\Omega \approx \frac{3|a|}{8} k\Omega \tag{6}$$

Using this equation, to have an output resistance greater than $1M\Omega$, the amplifier gain needs to be larger than 2660, which is very simple to meet at a low frequency but achieving such a gain is quite difficult at higher frequencies.

From this analysis it is quite obvious that the low frequency gain of the amplifier in the current source of Fig. 2 is not challenging at all. For instance the DC gain of 10^4 leads to an output resistance larger than $3M\Omega$, which is more than enough for all EIT applications. This result is very important since it can relax one restriction in our opamp design. Therefore, even with one cascoded stage, the required low frequency gain can be achieved. However, since it needs to drive a resistive load (Fig. 2), a buffered op-amp is needed.

c) Limited bandwidth

As it has been explained in the previous section, a low frequency gain of 10^4 is more than enough. However, as we know the frequency response of a stable op-amp can be written as:

$$a = \frac{a_0}{1 + j f/f_D} \tag{7}$$

For frequencies much higher than f_D , the gain magnitude |a|, can be approximately written as:

$$|a| \approx \frac{a_0 f_D}{f} = \frac{GBW}{f} \tag{8}$$

Combining Eq. 6 and Eq. 8, result to:

$$|Z_o| \approx \frac{3GBW}{8f} k\Omega \tag{9}$$

Therefore, for instance, if we want to achieve $200k\Omega$ output impedance at 500 kHz, according to Eq. 9 this means that the GBW of the op-amp needs to be more than 500 MHz.

We repeated the calculation of Section 3.a with resistors mismatches of 0.1% but with more realistic opamp characteristics ($a_0=10^4$, GBW=10⁸). For this condition the dominant pole f_D (f_D = GBW/ a_0) is located at 10⁴ Hz. This means that after this frequency, the gain will drop 20 dB for each frequency decade. Therefore no significant change of output impedance is expected up to 10 kHz. However at higher frequencies the gain lowering impact will be significant. Figure 5 shows the histogram of 10,000 samples in the aforementioned condition at 10 kHz and 500kHz, respectively. As it can be seen at 10 kHz the histogram is quite similar to that shown in Fig. 3, with ideal op-amp. However, all cases with an output resistance larger than 3.7 M Ω in Fig.3 is folded back to 3.7 M Ω which is set by Eq. 9. Moreover, at 500 kHz the output impedance is in the range of 75 k Ω , on which the resistor mismatches have an insignificant impact.

V. CONCLUSION

The output impedance of the Howland current source was assessed in terms of resistor mismatches and op-amp limited GBW. It has been shown that with resistor mismatches as low as 0.1%, which is achievable with a very careful layout design in standard CMOS technology, the output impedance of Howland current source can go down to $200k\Omega$ in some samples. In fact, about 10% of the samples can have an output impedance lower than $500k\Omega$. This means that if an output impedance higher than $500k\Omega$ is necessary, during the test at least 10% will not pass. It is also shown that the Howland output impedance is related to the amplifier low frequency gain with a very simple equation (Eq. 6) which is valid for both high and low frequencies. As an example, according to our results, for an output impedance larger than $1M\Omega$, the amplifier gain just needs to be larger than 2660. Although this is easily achievable at a low frequency, achieving this at a high frequency is a real challenge. It was also shown that to achieve an output impedance greater than 500 k Ω at frequency of 200 kHz, a GBW greater than 500 MHz is required.

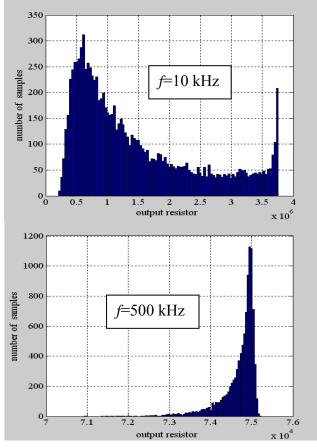


Fig. 4. The histogram of the output resistance while supposing 0.1% resistors mismatches, a0=104 and GWB=100MHz in 10 kHz and 500kHz.

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Experimental Study of Constant Fraction Discriminators

Mityo Georgiev Mitev, Stoyan Zhivkov Nikolov, Ludmil Todorov Tsankov and George Mitev Mitev

Abstract – **Practical circuits of constant fraction** discriminators are designed and studied experimentally. They are suitable for operation over wide amplitude range of pulses with nanosecond duration. The results of the experiments are described and the areas of application are outlined.

Keywords – Constant fraction discriminator (CFD), time measurements, delay line, muon detection.

I. INTRODUCTION

Precise determination of event occurrence moment is of utmost importance in time measurements. The resulting output signal must undergo amplitude normalization in order to be postprocessed in a logic circuitry. Accurate detection of an initial moment is dependent on amplitude fluctuations and shape variations of an input signal [2], [3]. To minimize the influence of these factors several schemotechnical approaches are applicable – fixed threshold circuit, zero crossing detector (with double signal differentiation) or a constant fraction discriminator (CFD) [6].

In CFD circuits the initial moment detection is independent of the input amplitude and is minimally influenced by the rise/fall time of the input signal. These circuits apply a strictly defined proportion of the input amplitude as a threshold level – an optimal level is generated for each input pulse in correspondence to its amplitude.

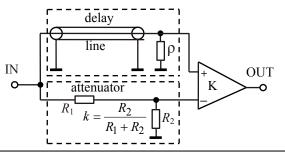


Fig. 1. Structure of a constant fraction discriminator	

To put this principle into practice the input pulse is

M. Mitev and S. Nikolov are with the Department of Electronics and Electronics Technologies, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: mitev@ecad.tu-sofia.bg, nayots@abv.bg

L.Tsankov is with the Department of Nuclear Engineering, Faculty of Physics, University of Sofia, 5, J. Bouchier blvd, BG-1164 Sofia, Bulgaria, e-mail: ludmil@phys.uni-sofia.bg

G. Mitev is with the Institute for Nuclear Research and Nuclear Energy, Nuclear Electronics Laboratory, Bulgarian Academy of Sciences, 72, Tzarigradsko Shausse blvd., 1784 Sofia, Bulgaria, e-mail: g_m_mitev@yahoo.com.

passed through two parallel channels – direct and delaying (fig. 1). In the direct channel an attenuator with a coefficient k reduces the amplitude of the pulse to a level corresponding to the ratio between the threshold and the initial amplitude. In the delaying channel the amplitude of the signal remains unchanged but a time delay is introduced. The value of this delay is calculated to ensure the delayed signal reaches the threshold level at the same time the direct signal is at its peak. A valid output is generated by the comparator K when the amplitude difference between the signals from the two channels changes its sign [7].

Constant fraction discriminators can operate in a wide dynamic range of input amplitudes (up to 1:1000) providing high precision of transient detection (\pm 30 ps) [5]. These top-level features make the CFD broadly used and a preferred choice with signals of strongly varying amplitudes.

II. INPUT ATTENUATOR AND DELAY LINE

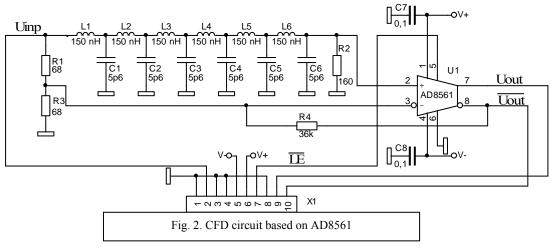
Usually, the attenuation coefficient is set to 2 and is not of critical importance to circuit operation. The input impedance formed by the parallel connection between the attenuator and the characteristic impedance of the delay line must be equal to the characteristic impedance of the input signal cable. Thus, a proper termination of the line is achieved and no parasitic reflected signals are allowed. In the case described here cable impedance is 75 Ω .

The CFD circuits presented in the paper are used with signals from plastic scintillators. The latter are characterized by a very short scintillation time (few nanoseconds). Due to this physical property the delay lines are designed as 6-stage lumped parameter LC circuits with 4,3 ns and 9 ns total delay and characteristic resistance of 160 Ω .

III. CFD FOR OPERATION WITH BIPOLAR INPUT PULSES

In some cases the time measurement circuits are used with both positive and negative inputs. A schematic solution operating in such a bipolar mode is shown in fig. 2. The fast AD8561 comparator is powered by positive and negative supply voltages. The intrinsic delay of the comparator is 7 ns. and the CFD circuit is designed for pulses of approximately 10 ns. rise/fall time. The passive elements introduce 9.2 ns delay. The characteristic resistance of the line is 160Ω .

The input attenuator (R1 and R2) is calculated to terminate a 75Ω -input signal cable. With resistor R4 a



positive feedback is introduced creating a 5 mV hysteresis to enhance the noise immunity of the circuit.

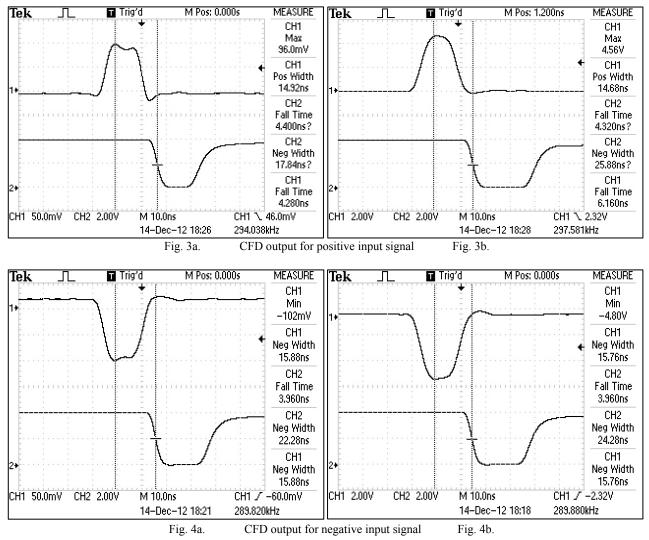
The circuit is tested under both positive and negative input pulses with 15 ns duration. The input amplitude is varied in wide range – from 100 mV to almost 5 V. Under these conditions the delay between the input and the output remains constant. In fig. 3a and 3b oscillograms are shown for positive input pulses with amplitudes 96mV and 4.56V. There is no meaningful difference between the two delays.

Circuit operation with negative input pulses is depicted in fig. 4a and 4b – the corresponding amplitudes: -102 mV

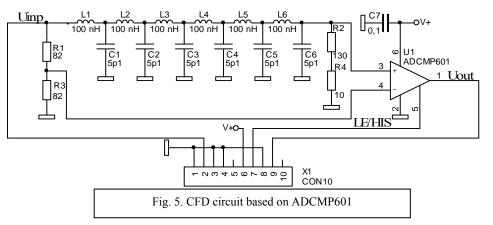
and -4.80 V. Again, it can be clearly seen that the delays between the normalized outputs and the inputs are independent of the input amplitudes.

Additional advantage of this circuit is the presence of a complementary output. Thus, it is suitable for joint operation with low-voltage differential (LVD) logic to enhance the overall noise immunity.

The CFD described above is implemented as a separate module with dimensions 15x25 mm.







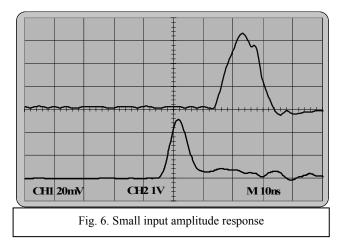
IV. CFD FOR OPERATION WITH POSITIVE INPUT PULSES

In a case when only positive input pulses are present a CFD can be based on the faster ADCMP601 comparator. Its intrinsic propagation delay is under 3.5 ns and its rise/fall time is under 4 ns. An interesting feature of this IC is the capability of hysteresis control via the current through pin LE/HIS without need of external positive feedback. This makes the IC applicable with even shorter pulses.

A schematic diagram of CFD with ADCMP601 is given in fig. 5. The delay line is calculated to provide 4.3 ns and wave resistance 140 Ω which enable the circuit to operate with shorter input rise/fall times – approximately 5 ns. The attenuator of the circuit in fig. 5 is designed to terminate a 75 Ω -coaxial cable.

The oscillogram in fig. 6 shows the capability of the circuit to operate properly with small input amplitudes (positive only). The input pulse is bell-shaped, its amplitude is approximately 50 mV, duration – 10 ns.

The circuit is implemented as a separate module with geometrical and electrical configurations identical to those of the first one. This ensures the interchangeability of the both modules.



V. EXPERIMENTAL RESULTS WITH REAL-LIFE SIGNALS

The CFD circuits presented in the paper are designed to operate in the time measurements channel of the extensive air shower (EAS) detection system 0 which is constructed within the framework of the BEASA project 0. The system incorporates scintillation detectors UPS-923A type consisting of plastic scintillators and fast XP1912 photomultiplier tubes. The individual detectors in the cluster are located at a distance of 20 m. between one another. This configuration requires fast pulse amplifiers to be added between detector outputs and their CFDs [1] and the individual delays in the time channels to be accurately equalized.

The schematic diagram of the pulse amplifier used is shown in fig. 7. AD8055 op amp with 300MHz bandwidth and 1400V/ μ s slew rate is used. The circuit is designed for voltage gain A_u = -1. This way the negative pulses from the PMT anode are transformed into positive which then can be processed by a ADCMP601-based CFD circuit.

The input impedance of the amplifier is 50 Ω to ensure proper termination of the signal cables from the detectors. The output feeds a 75 Ω -communication cable to the CFD.

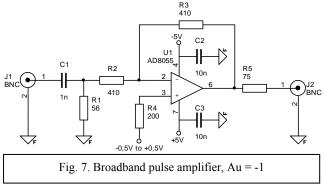


Fig. 8 shows an oscillogram of the amplifier output for a small stream of muons detected. The signal amplitude is approximately 110 mV and its duration - 8 ns. The same figure shows the output of the CFD based on ADCMP601.

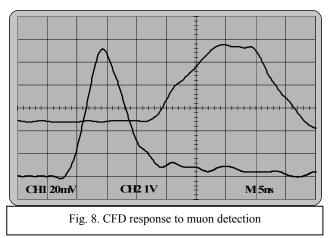
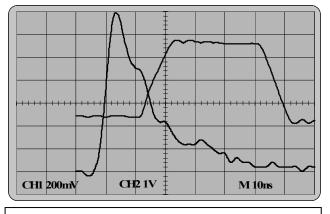
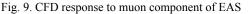


Fig. 9 presents an oscillogram of a signal which probably results from a secondary muon stream during EAS. The amplitude of the signal is significantly large (1400 mV), the duration is increased (above 15 ns). The tail of the pulse is wave-shaped which corresponds to several almost





simultaneous interactions between muons and the scintillator. The output of the CFD in this case shows identical delay to that in fig. 8. This suggests that the developed CFD circuit allows a very high accuracy in determination of the event occurrence time.

VI. CONCLUSION

The CFD prototypes developed and experimentally studied in the present work provide precise time measurements of pulse signals with nanosecond duration and wide amplitude range. The first circuit appears to be slower but ensures broader capabilities for compliance with the subsequent logic circuitry because of its LVD interface.

The second one based on the ADCMP601 comparator enables dynamic hysteresis control to adjust system sensitivity. This CFD circuit is faster and is applicable with input signals of smaller rise/fall time and duration.

ACKNOWLEDGEMENTS

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Indoor Localization System for Lighting Control

Marin Berov Marinov, Borislav Todorov Ganev and Georgi Todorov Nikolov

Abstract – The localization of people and objects in different environments is an essential prerequisite for many applications in navigation, robotics, machine control and monitoring. The limiting factor for many applications is the indoor environment in which the Global Satellite Systems work only partially or cannot function at all.

Currently radio frequency (RF) based methods are being increasingly implemented for indoor localization. They are relatively inexpensive to install, and are less subjected to the line-of-sight limitations affecting a significant number of other methods.

The research presented in this paper aims to evaluate the possibility for using relatively low-cost and easily expandable RF-based localization techniques for lighting control in warehouse environments. The implementation of the localization system utilizes the RSS of a ZigBee-based sensor network.

Keywords – Indoor localization, RSS, ZigBee, energy saving, lighting control.

I. INTRODUCTION

The task of locating and navigating people and devices in indoor environments is becoming increasingly relevant in solving different problems in the field of automation.

The global satellite positioning systems have excellent performance for outdoor positioning, but a rising number of applications require good localization capabilities in all sorts of environments. So, indoor localization has become a focus of research and development over the last two decades. Following the logic of satellite navigation development, currently efforts are being focused on improving service quality of indoor environments. Improving the quality and safety of indoor localization and navigation has the potential for opening many new capabilities in the field of automation and energy saving technologies.

Although a number of basic principles of localization and navigation can be used both outdoors and indoors, essential differences between these two environments lead to significant differences in significant differences in the

M. Marinov is with the Department of Electronics and Electronics Technologies, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8, Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: mbm@tu-sofia.bg

B. Ganev is with the Department of Electronics and Electronics Technologies, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8, Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: b_ganev@tu-sofia.bg

G. Nikolov is with the Department of Electronics and Electronics Technologies, Faculty of Electronic Engineering and Technologies, Technical University - Sofia, 8, Kliment Ohridski blvd., 1000 Sofia, Bulgaria, e-mail: gnikolov@tu-sofia.bg

way they perform.

Major challenges to indoor localization and navigation are:

- rapid environmental changes due to the presence of people and transport vehicles
- multipaths due to reflections from walls, ceilings and equipment
- Non-line-of-Sight (NLoS) conditions
- Fast changing signal attenuation and scattering due to the changing density of objects (especially in warehouse environments)
- High precision needed for some applications.

There are also some aspects which facilitate the indoor localization:

- restricted spaces
- constant geometrical constraints by which a reduction in the accuracy requirements can be achieved
- less strict requirements for the dynamic parameters of the system due to the lower speed of operation in indoor spaces
- Negligible or no impact produced by unfavorable weather effects [1].

Numerous studies indicate that, unlike the outdoor localization and navigation in indoor environments, there is no universal solution based on a dominant technology [1, 2, 3]. Modern systems typically require specialized infrastructure including fixed base stations and mobile nodes.

In a detailed investigation Mautz divides the approaches for indoor positioning into 13 main groups in terms of accuracy, coverage and measuring principle (Table 1). The majority of technologies are based on electromagnetic waves and only a few ones - on mechanical (ultrasound) waves. Here the connection between systems using shorter waves and achieving higher accuracy results is clearly observed [1, 2].

TABLE 1. OVERVIEW OF INDOOR POSITIONING TECHNOLOGIES [1].

	Technology	Typical Accuracy	Typical Coverage (m)	Measuring Principle
1	Cameras	0.1mm	1 – 10	angle measurements from images
2	Infrared	cm – m	1 – 5	thermal imaging, active beacons
3	Tactile & Polar Systems	µm — mm	3 - 2000	mechanical, interferometry
4	Sound	cm	2-10	distances from time of arrival
5	WLAN / WiFi	m	20 - 50	fingerprinting
6	RFID	dm – m	1 – 50	proximity detection, fingerprinting
7	Ultra Wideband	cm – m	1 – 50	body reflection, time of arrival

8	High sensitive	10 m	ʻglobal'	parallel correlation
	GNSS			
9	Pseudolites	cm – dm	10 - 1000	carrier phase
				ranging
10	Other Radio	m	10 - 1000	fingerprinting,
	Frequencies	m		proximity
11	Inertial	1 %	10 - 100	dead reckoning
	Navigation			-
12	Magnetic		1 - 20	fingerprinting and
	Systems	mm – cm	1 - 20	ranging
13	Infrastructure		building	fingerprinting,
	Systems	cm – m		capacitance

Currently radio frequency (RF) based methods are being increasingly implemented. They are relatively inexpensive to install and are subjected to a lesser degree to the line-ofsight limitations that affect a significant number of other methods.

By the RF technologies the most frequent positioning principle uses the measurement of the strength of the received signal (RSS) [1, 8]. Such RF based approaches assume that there are some fixed nodes with known location which act as beacon points in order to localize other mobile nodes with unknown location.

The research presented in this paper aims to evaluate the possibility for using relatively low-cost and easily expandable RF-based localization techniques for lighting control in warehouse environments. The implementation of the localization system utilizes the RSS of a sensor network based on the ZigBee standard.

II. REASONS FOR THE IMPLEMENTATION OF LIGHTING CONTROL SYSTEM

The systems for indoor localization and navigation are already used for the optimization of logistics solutions and transportation tasks in complex warehouse environments.

In this work a more specific application related to energy-efficient lighting control in warehouses is considered. According to the proposed solution, illumination levels in the different warehouse zones are controlled depending on the presence or absence of vehicles or operators in the corresponding areas.

In storage environments with conventional lighting control, lighting is usually left on permanently, regardless of whether logistics activities are performed or not in the warehouse area. This leads to unnecessary energy expenditure for lighting.

For assessing the energy saving potential for lighting, statistical data are used for the energy consumption of one square meter of storage area [13]. Further assessment has been carried out for establishing the typical percentage values of the activity-occupied warehouse area in relation to the total warehouse area by means of the multi-moment observation technique for activity sampling [4]. For this assessment a simplified model of the storage environment has been used (fig.1).

On the basis of multi-moment observations for activity sampling, it is possible to determine with a statistical accuracy of 95% that the percentage of areas occupied by logistics activities most often fluctuates within the range of 35-40%. Only rarely (<10% of the performed observations) are the achieved levels within the range of 60-65%. Even if

we take this worse case scenario as a basis for calculations, it can be assumed that the potential for energy saving is definitely over 35%. A number of recent studies show that the installation of sensors and high efficient lighting systems can save between 30-70% on electricity consumption for lighting [13].

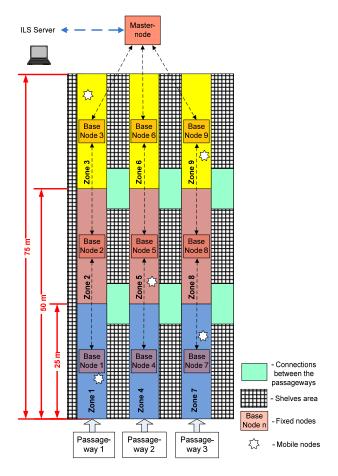


Fig. 1. Model of the storage environment for the multi-moment activity sampling

In other words, typical lighting costs of $3-3.5 \text{ euros/m}^2$ per year will get a potential lighting cost saving in the range of $1-1.25 \text{ euros/m}^2$ per year. For example, for a typical warehouse of about 10 000 m² the saving potential will be in the range of 10-12,000 euros, and will steadily increase with the rise of electricity prices. These considerations are also important for the selection of appropriate technology for solving the problem of localization, which is discussed in the next chapter.

III. LOCALIZATION SYSTEM ARCHITECTURE

We use a location estimation technique using RSSI in a ZigBee standard based sensor network.

An approach has been chosen where in each passageway between the storage racks a number of fixed sensor nodes with known positions are mounted. With these the location of the mobile nodes can be determined.

The mobile node is a wireless device which sends packets to the neighboring fixed nodes in the relevant zone and also in the neighboring zones. These fixed nodes measure the received signal strength (RSS) and send the data to the master node. There are usually many mobile nodes and that is why each data packet also contains the corresponding mobile node ID. The master node forwards the data to the Indoor Location Server (ILS), which estimates the position of the mobile node.

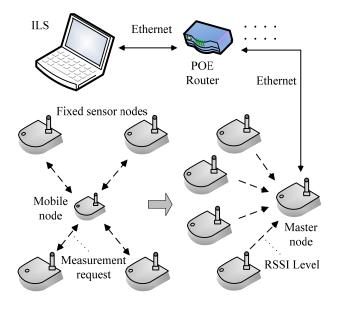


Fig. 2. Localization system based on RSS measurement in a ZigBee sensor network

A. Fixed sensor nodes placement

In this configuration one fixed receiver for each zone is provided. Depending on the accuracy required for the positioning and additional requirements of the particular task, the size of the zone can be chosen. In this implementation the requirements for localization accuracy are comparatively low, and this is why areas with an approximate length of 25 m and a width of about 2.5 m have been selected.

B. Data collection

This system aims to perform position estimation using only information from sensor nodes of a certain constant number. The threshold value of RSSI is set for each sensor node. Then a sensor node transmits a packet to the master node only when the received signal from a mobile node exceeds this value. In this way, the quantity of transferred data can be controlled by changing this threshold value.

The following two kinds of messages exchanged in this system have been defined:

Messages for requested measurement

These are messages for the need of measuring the received mobile node signal which has been sent to the fixed sensor nodes. The message is then transmitted by broadcasting. To identify the measurement request a sequence number is included in the message.

Messages for received signal strength

These are messages for reporting RSSI to a master node from the fixed sensor node. They contain the ID of the mobile node and sequence number.

IV. LOCALIZATION SYSTEM IMPLEMENTATION

A. Hardware

The all nodes have been implemented based on PINGUINO-OTG. The main features of this hardware module are:

- PIC32MX440F256H 80 MHz microcontroller
- 256KB Flash and 32KB RAM
- Li-Ion rechargeable battery power supply option with build in on board charger
- Reliable work in industrial temperature range.

All devices (fixed, mobile and master nodes) have been implemented based on the ZigBee MRF24J40MA module. MRF24J40MA is a 2.4 GHz IEEE 802.15.4 radio transceiver module. It has an integrated antenna and supports ZigBee and MiWi protocols. The module has a 4wire SPI interface and it can be connected to the PIC32-PINGUINO-OTG through the UEXT connector.

Because the mobile node is battery powered, the connection with fixed node is not established continuously. Few times in a second, the mobile node is trying to connect with fixed node, and sends its ID, a sequence number and RSSI level. Then it is going in sleep mode.

Fixed sensor node contains two MRF24J40MA modules, one for connecting with the mobile node, and other to connect with master node, and previously fixed sensor nodes. Both modules work continuously. They give also additional information for their state, so if there are problems with some fixed sensor node, they can be found.

In the master node have been added one Ethernet controller with SPI interface ENC28J60, and has its own IP and MAC address. It takes data from attached fixed sensor nodes, and sends it to ILS through Ethernet. The node can be powered using standard wall adapter, or via Ethernet, using build in "Power over Ethernet" (PoE) function (TPS23750). PoE provides both data and power connections in one cable, so the equipment does not require a separate cable for each need [14]. The device consumes very little power, and is classified in Class 1 - very low power device, with consumption of 0.44 to 3.84W.

B. Software

There are two main families of RF based algorithms: range-free ones and range-based ones. Range free algorithms need no prior knowledge of the level of the received signal strength. By contrast, range-based algorithms need an initial calibration for beacon signal strength and location. Range-based algorithms are further divided into several categories, the principal ones being RSSI map-based and path-loss model-based algorithms [6, 7, 8, 10].

By the localization system implementation we use the RSSI map based algorithm. For the position estimation the following procedure is used:

• The fixed sensor nodes are arranged in the warehouse area and their positions are saved in a database on the ILS-Server. The threshold values for the RSS are set to each sensor node.

- A message for measurement request is transmitted to the fixed sensor nodes from a given mobile node.
- Each sensor node measures the RSS by receiving the message for measurement request. If the RSSI exceeds the previously defined threshold value, the fixed sensor node transmits the mobile node ID to the corresponding master node.

A typical method using RSSI mapping is the k-nearest neighboring training based algorithm. In the kNN algorithm, a data set of fixed node RSS values at different sample points is used to train the algorithm and to get the RSSI signature map [9, 12].

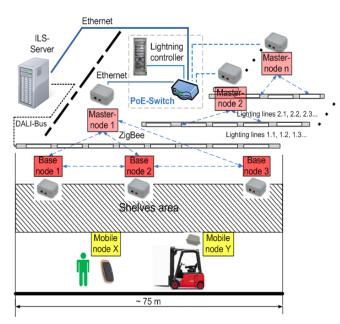


Fig. 3. Overview of the localization system main components

V. CONCLUSION

In this paper we have proposed a localization system using RSSI in a sensor network based on the ZigBee standard has been implemented.

The system was tested in a real site with over $8,000 \text{ m}^2$ warehouse space. Tests have been conducted for over 2 months. They confirm the supposed potential energy saving potential of over 40% and that the choice of the implementation technology was suitable.

The relatively low cost of radio frequency applications and their strength in overcoming limitations of other techniques suggests that the RSSI based equipment and algorithms are suitable for indoor localization applications, such as lighting control.

The test results have shown that it is necessary to take steps to streamline communications between the fixed sensor nodes to ensure a long-term stable operation of the system.

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