FPAA PROTOTYPING OF SIGNAL CONDITIONING CIRCUIT FOR INDUCTIVE DISPLACEMENT TRANSDUCER

Filip Todorov Koparanov, Mihail Hristov Tzanov, Emil Dimitrov Manolov

Department of Electronics, Technical University – Sofia, 8 Kliment Ohridski Str., 1000 Sofia, Bulgaria, phone: +359 2 965 3269, e-mail: edm@tu-sofia.bg

The paper presents the results from the design and investigation of FPAA based signal conditioning circuit for Inductive Displacement Transducer (IDT). The design utilizes Simulink behavioral model of the signal conditioning circuit based on dual half-wave rectifiers. The synthesized FPAA prototype is simulated and practically examined employing WA200 IDT sensor. The obtained results confirm the efficiency of the proposed solution. The discussed circuit is applicable in the development of switched-capacitor signal conditioning blocks for ASICs and SoCs.

Keywords: FPAA, Inductive Displacement Transducer, Signal conditioning

1. INTRODUCTION

The time-to-market is a very critical factor for ASICs and SoCs design. The time-to-market problems can be avoided applying contemporary computer-aided design resources and programmable integrated platforms [1].

Computer-aided design resources are utilized to predict the behavior of a system that is to be developed. They reduce the risk of unintended system behavior through virtual testing before developing the actual hardware.

The programmable platforms ensure fast prototyping and practical investigation of the designed circuit and systems as well as possibilities for dynamically reconfiguration and programming at work. The Field Programmable Analog Array (FPAA) of Anadigm Inc. (Mesa, AZ, USA) is widely utilized platform for practical prototyping and examination of analog and mixed-signal circuits. The internal structure of FPAA chips is based on a switched-capacitor circuitry, which assures possibilities for configuration and programming of different functional blocks. Applying FPAA the researcher can work at a functional level, basing the design on the pre-classified software and hardware components. This allows creating complex analog circuits in a fraction of the time instead using traditional discrete components [2]. Consequently, the use of FPAA ensures easy implementation and quick reconfiguration of the examined prototypes. The basic advantage of this approach is the possibility for simple conversion of the synthesized FPAA prototype into integrated switched-capacitor circuit [3].

This paper presents the results from the design and examination of FPAA signal conditioning circuit for Inductive Displacement Transducer (IDT). The design is based on the Simulink (The MathWorks Inc., Natick, Massachusetts, USA) behavioral model of the signal conditioning circuit developed and examined in [4]. The synthesized working FPAA prototype is practically tested and the results explicitly confirmed the effectiveness of the applied solution. The obtained results are

applicable in the development of switched-capacitor signal conditioning blocks for ASICs and SoCs.

2. SIMULINK MODEL OF THE SIGNAL CONDITIONING CIRCUIT

Fig.1 shows the Simulink model of the signal conditioning circuit for IDT proposed in [4]. The signal conditioning circuit is utilized to extract the information for the displacement from the signals at the outputs of the IDT, which is connected in full-bridge configuration. The model is based on dual half-wave analog rectifiers. The input signal (displacement of the core *D*) changes between 0 mm and 200mm. The two measurement signals MS(+) and MS(-) (see Fig.1) are fed to the half-wave rectifiers, which reject one of the alternating cycles of the signals. Consequently at the outputs of the rectifiers a half-wave signal appears. The two signals are to be subtracted from each other in the Subtract block. The output of the Subtract block is a half-wave voltage, which amplitude is directly proportional of the displacement D. The subsequent low-pass filter forms a DC voltage signal. This voltage is multiplied by Slope constant and after the Y-intercept constant is subtracted in order to obtain the displacement *D* as an output DC voltage.

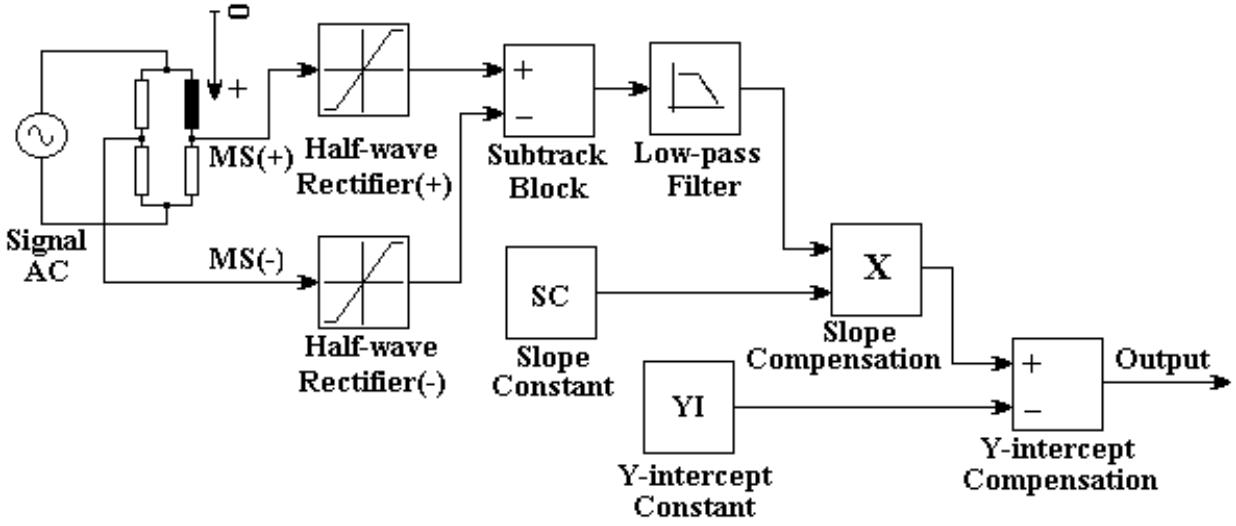

Fig.1. Simulink model of signal conditioning circuit for IDT

3. FPAA IMPLEMENTATION OF THE SIGNAL CONDITIONING CIRCUIT

Fig.2 presents the proposed FPAA implementation of the signal conditioning circuit utilizing AN221E04 chip of Anadigm and based on the above described Simulink model. Fig.3 demonstrates the results from simulation the circuit by means of functional simulator of Anadigm. (The applied excitation AC signal is 2.5V RMS, 4.8 kHz, sinusoidal).

The output sinusoidal signals MS(+) and MS(-) of the IDT sensor are fed to the two unity gain input cells (see Fig.2). The two half-wave Rectifier Hold blocks reject the positive cycle of the signals (see Fig.2) and at each output (see Fig.3) negative half-wave signal appears with amplitude

(1) $$A_{ms-}[mV] = 2500\sqrt{2}K,$$

for Rectifier Hold (-) and

$$A_{ms+}[mV] = 2500\sqrt{2}(K + 0.001 \cdot S \cdot D + 0.001 \cdot Z), \quad (2)$$

for Rectifier Hold (+).

In the presented formulas K is the constant of the inductive voltage divider, Z is the zero point tolerance of the IDT in mV/V, S is the sensitivity of the IDT in mV/(V.mm) and D is the displacement in mm.

The signals at the outputs of the Rectifier Hold blocks are subtracted from each other (see Fig.2) and two subsequent low-pass filters with cut-off frequency of about 500Hz (in Fig.3 is shown the signal after first filter) deliver a DC voltage:

$$U_{DC}[mV] = \frac{A_{ms+} - A_{ms-}}{\pi} = \frac{2.5\sqrt{2}(S \cdot D + Z)}{\pi}. \quad (3)$$

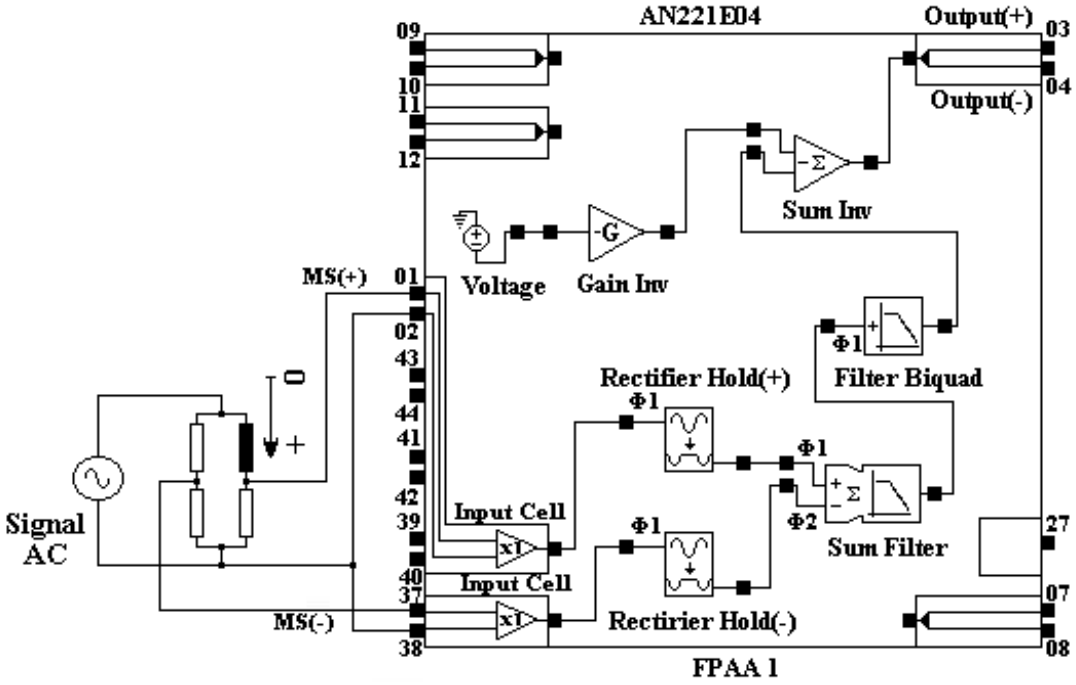

Fig.2. FPAA implementation of the signal conditioning circuit

Then the displacement D can be determined solving Equation (3):

$$D = \frac{\pi U_{DC}}{2.5\sqrt{2} \cdot S} - \frac{Z}{S} = SC \cdot U_{DC} - YI, \quad (4)$$

where SC is the slope factor and the YI is the y-intercept.

Equation (4) is implemented by multiplying U_{DC} by SC and subtracting the coefficient YI in the SumInv block (see Fig.2). The values of SC and YI are computed in advance and multiplied by 10 in order to ensure 10mV of output voltage corresponding to 1mm of displacement. SC is settled as a gain at the lower input of the SumInv block. The value of y-intercept YI is settled with Voltage reference and GainInv blocks. Finally, at the differential output, between Output(+) and Output(-) (see Fig.2), the displacement D is obtained as an stable DC voltage between 0V and 2000mV with 10mV corresponding to 1mm of displacement (see Fig.3).

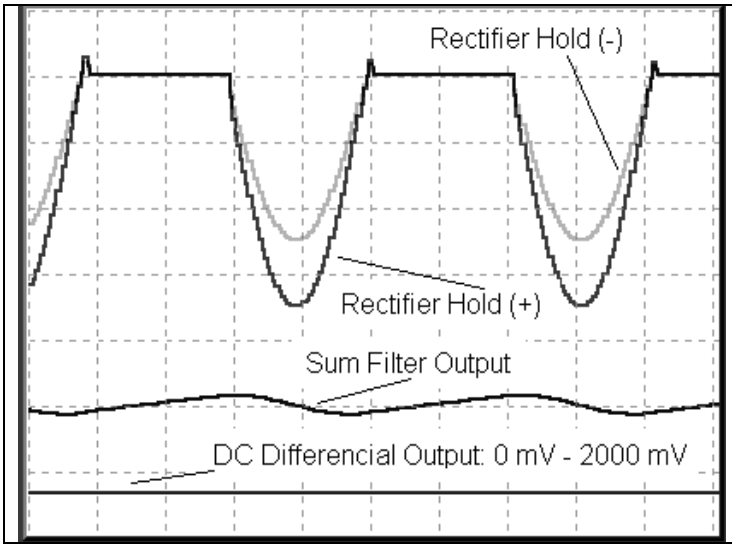

Fig.3. Results from functional simulation of the FPAA signal conditioning circuit.

Table 1 shows the configuration information for utilized FPAA circuit.

Table 1. Configuration information for FPAA circuit, Clock A=250kHz

I/O Modules

Name	Options	
InputCell	I/O Mode	*Input*
	Input	*Differential*
	Input Amplifier	*Off*
	Anti-Alias Filter	*Unity Gain Stage*
	Input Line for Cell 4 Select	*A*
OutputCell	Mode	*Bypass*
	Status	*On*

Configurable Analog Modules

Name	Options		Parameters	
RectifierHold	Rectification	*Positive Half Wave*	Gain	*1.00*
	Input Sampling Phase	*Phase 1*		
SumInv	Input 3	*Off*	Gain (UpperInput)	*1.13*
			Gain (LowerInput)	*22.3*
GainInv			Gain	*0.52*
Voltage	Polarity	*Negative (-3V)*		
SumFilter	Output Changes On	*Phase 1*	Corner Frequency [kHz]	*0.500*
	Input 1	*Non-inverting*	Gain 1 (UpperInput)	*1.00*
	Input 2	*Inverting*	Gain 2 (LowerInput)	*1.00*
	Input 3	*Off*		
FilterBiquad	Filter Type	*Low Pass*	Corner Frequency [kHz]	*0.499*
	Filter Topology	*Automatic*	Gain	*1.00*
	Input Sampling Phase	*Phase 1*	Quality Factor	*1.00*
	Polarity	*Non-inverting*		

4. EXPERIMENTAL RESULTS

The discussed signal conditioning circuit is examined by using AN221K04 FPAA Evaluation Board from Anadigm Inc. This board allows programming of FPAA integrated circuit AN221E04 via the serial port of the personal computer. IDT WA200 sensor (Hottinger Baldwin Messtechnik Gmbh, Darmstadt, Germany) with working displacement between 10mm and 200mm, S=0.4mV/(V.mm) and Z=4 mV/V is joined to the inputs MS(+) and MS(-) of the circuit. The excitation signal for the primary winding is 2.5V RMS, 4.8 kHz, sinusoidal. In these conditions when the displacement D is between 10mm and 200mm the DC voltage at the output of the signal conditioning circuit is expected to be between 100mV and 2000mV, i.e.

$$U_{OUT}[mV] = 10\left[\frac{mV}{mm}\right] \cdot D[mm]. \quad (5)$$

The practically obtained measurement results correspond to the expectations according to Equation (5). For example, when the displacement D is 100mm, the signal at IDT sensor output between MS(+) and MS(-) is 110mV RMS and at the differential output of the signal conditioning circuit 1000mV stable DC appears.

The most important advantage of the applied approach is the possibility for interactive fine tuning of the FPAA block parameters of the implemented prototype. This allows realizing precise compensation of the inexactness and the specifics of the employed IDT and FPAA.

5. CONCLUSION

The paper presents the results from design and investigation of FPAA based signal conditioning circuit for Inductive Displacement Transducer (IDT). The design utilizes Simulink behavioral model of a signal conditioning circuit based on dual half-wave rectifiers. The FPAA prototype of the synthesized circuit is simulated and practically approved by employing WA200 IDT sensor. The results validate entirely the effectiveness of the selected approach for sensor conditioning circuit implementation. The developed FPAA solution is appropriate to be utilized in the design and implementation of ASICs and SoCs.

6. ACKNOWLEDGMENTS

The research presented in this paper was co-funded by the Internal Competition Project of TU-Sofia, 2008.

7. REFERENCES

[1] Moretti G., *Platform-based design: Blocks and buses lead the way*, EDN, 8/21/2003, http://www.edn.com/article/CA316049.html

[2] www.anadigm.com

[3] Ganesan, S., R.Vemuri. *Technology Mapping and Retargeting for Field-Programmable Analog Arrays*, Proceedings DATE-2000, Paris, 2000, Mar., pp.58-64.

[4] Tzanov M. H., F.T. Koparanov, E. D. Manolov, *Simulink Modeling of Signal Conditioning circuit for Inductive Displacement Transducer*, Proceedings of the Seventeenth Int. Conference ELECTRONICS-ET2008, 2008, (in the same issue).