SIMULINK MODELING OF SIGNAL CONDITIONING CIRCUIT FOR INDUCTIVE DISPLACEMENT TRANSDUCER

Mihail Hristov Tzanov, Filip Todorov Koparanov, Emil Dimitrov Manolov

Department of Electronics, Technical University – Sofia, 8 Kliment Ohridski Str., 1000 Sofia, Bulgaria, phone: +359 2 965 3269, e-mail: edm@tu-sofia.bg

This paper presents the developing and examining a Simulink model of signal conditioning circuit for Inductive Displacement Transducer (IDT). To this aim the basic specifications of IDT WA200 sensor are studied and Simulink behavioral model is proposed. The two most popular methods for signal conditioning of IDT output signal are described and Simulink model based on dual half-rectifiers is synthesized. The models are utilized to study and predict the performance of the integrated IDT sensor interfacing block. The obtained results are applicable in the design and verification of ASICs and SoCs.

Keywords: Simulink, Inductive Displacement Transducer, Signal conditioning

1. INTRODUCTION

Computer simulations are an integral part of the entire contemporary design process in electronics. They are utilized to predict the behavior of a system that is to be developed. To achieve this, a system model of the real system is created. This model is then employed to predict actual system performance and to help in making design decisions. The most important goal of computer-aided simulations is to reduce the risk of unintended system behavior through virtual testing before developing the actual hardware. Virtual testing permits access to the innermost nodes of a system, which can be difficult if not impossible to observe in physical prototypes. This type of testing also allows analysis of the impact of component tolerances on overall system performance [1].

The IDT is an electro-mechanical transducer, the input to which is a physical movement of the transducer core, and the output is a change in magnetic coupling between the internal windings. Usually the IDT output voltage is measured using suitable conditioning electronics, which is implemented as separate unit. The output of the conditioning electronics is a stable DC voltage which is proportional to the core position [2]. But if the IDT is a part of a system, based on ASIC or SoC, it is more appropriate to integrate the conditioning electronics within the chip. With regard to this new technical solutions are necessary to be developed and investigated.

The paper presents the design and examining a Simulink model of signal conditioning circuit for Inductive Displacement Transducer (IDT). Basic specifications of IDT WA200 sensor (Hottinger Baldwin Messtechnik Gmbh, Darmstadt, Germany) and two of the most popular methods for signal conditioning of its output signals are studied. Simulink (The MathWorks Inc., Natick, Massachusetts, USA) models for the transducer and for a generalized conditioning circuit are

proposed. The models present the functional behavior of the components. They are utilized to predict the performance of the IDT conditioning circuits and allow examining their basic operational characteristics using simulations.

2. SIMULINK MODELING OF THE INDUCTIVE DISPLACEMENT TRANSDUCER

Fig.1 shows both types of IDT (Displacement probe and Plunger). The measuring principle is based on an active quarter bridge, which can be utilized in full-bridge or half-bridge mode. Fig.2 depicts the general electrical wiring diagram of IDT in full bridge connection, which is employed in the presented work. For the WA200 IDT sensor the working displacement is between 10mm and 200mm. The key parameter is the gain or "sensitivity" *S* of the sensor, which is the nominal or expected RMS output voltage change per millimeter of core displacement per RMS input voltage. The recommended stimulus signal for the primary winding is 2.5V RMS, 4.8 kHz, sinusoidal. For the discussed sensor the nominal sensitivity is 0.4 mV/(V.mm), the deviation from the nominal sensitivity is ±1%, and its zero point tolerance *Z* (voltage offset when the core is at zero position) is ±8 mV/V [3]. Consequently, in the real transducers, the coefficients *S* and *Z* deviate from their ideal values and vary between 0.396 mV/(V.mm) and 0.404 mV/(V.mm) for *S*, and between -8 mm/V and +8 mm/V for *Z*.

Fig.1. Both types of IDT

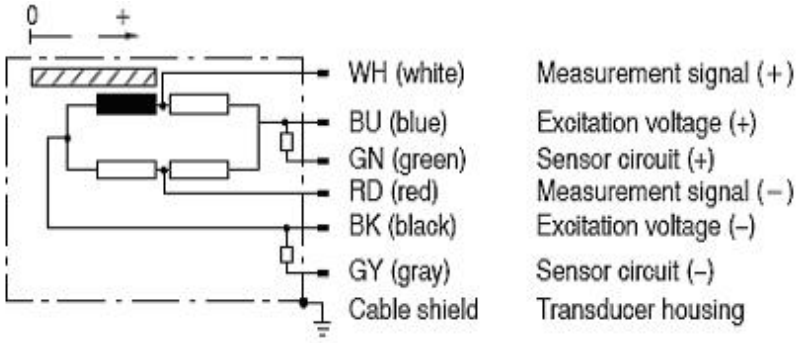

Fig.2. General electrical wiring diagram of IDT, full bridge mode

Based on the described specification parameters, the AC voltage at the *Measurement signal (-)* output (see Fig.2) can be expressed as:

$$u_{ms-}[V] = 2.5\sqrt{2}K\sin(2\pi ft), \quad (1)$$

where $2.5\sqrt{2}$ is the amplitude of the excitation signal in V, *K* is the constant of the inductive voltage divider, *f* is the linear frequency of the excitation signal in Hz, and *t* is the time in s.

When the core is at zero position, the expression for *Measurement signal (+)* output (see Fig. 2) is:

$$u_{ms+}[V] = 2.5\sqrt{2}(K + 0.001 \cdot Z)\sin(2\pi ft), \quad (2)$$

where *Z* is the zero point tolerance in mV/V.

When the core is displaced Equation (2) changes as follows:

(3) $$u_{ms+}[V] = 2.5\sqrt{2}(K + 0.001 \cdot S \cdot D + 0.001 \cdot Z)\sin(2\pi ft),$$

where *S* is the sensitivity in mV/(V.mm) and *D* is the displacement in mm.

For a full bridge configuration the information for the displacement *D* is embedded in the difference between the *Measurement signal (+)* and *Measurement signal (-)* outputs:

(4) $$u_{diff}[mV] = 2.5\sqrt{2}(S \cdot D + Z)\sin(2\pi ft),$$

where *S* is in mV/(V.mm), *Z* is in mV/V and *D* is in mm.

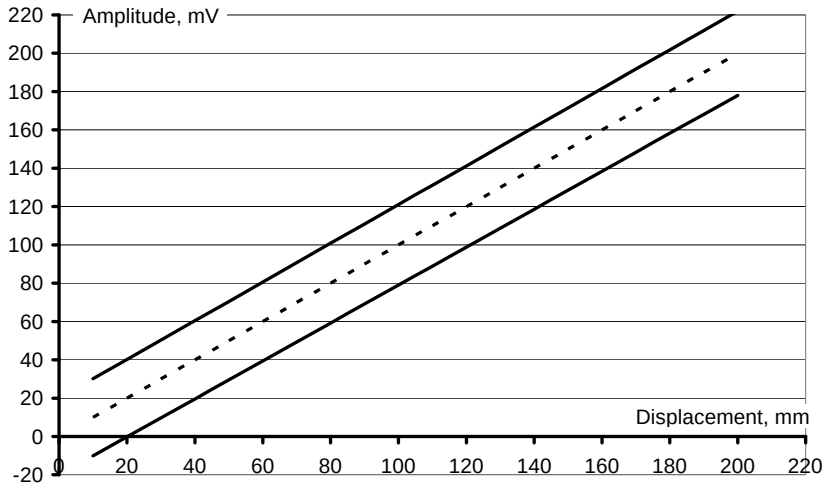

Fig.3. Transfer characteristics of IDT WA200.

Fig.3 illustrates the transfer characteristics of the IDT WA 200. The characteristics are straight lines with a slope, which depends on the value of *S*, and y-intercept, which depends on the value of *Z*. The two solid lines show the worst case scenarios for 2.5V RMS excitation voltage: the upper line is for *S*=0.404 mV/(V.mm) and *Z*=8 mV/V; and the bottom line - for *S*=0.396 mV/(V.mm) and *Z*= -8 mV/V. The dashed line in the middle depicts the ideal characteristic: *S*=0.4 mV/(V.mm) and *Z*=0 mV/V.

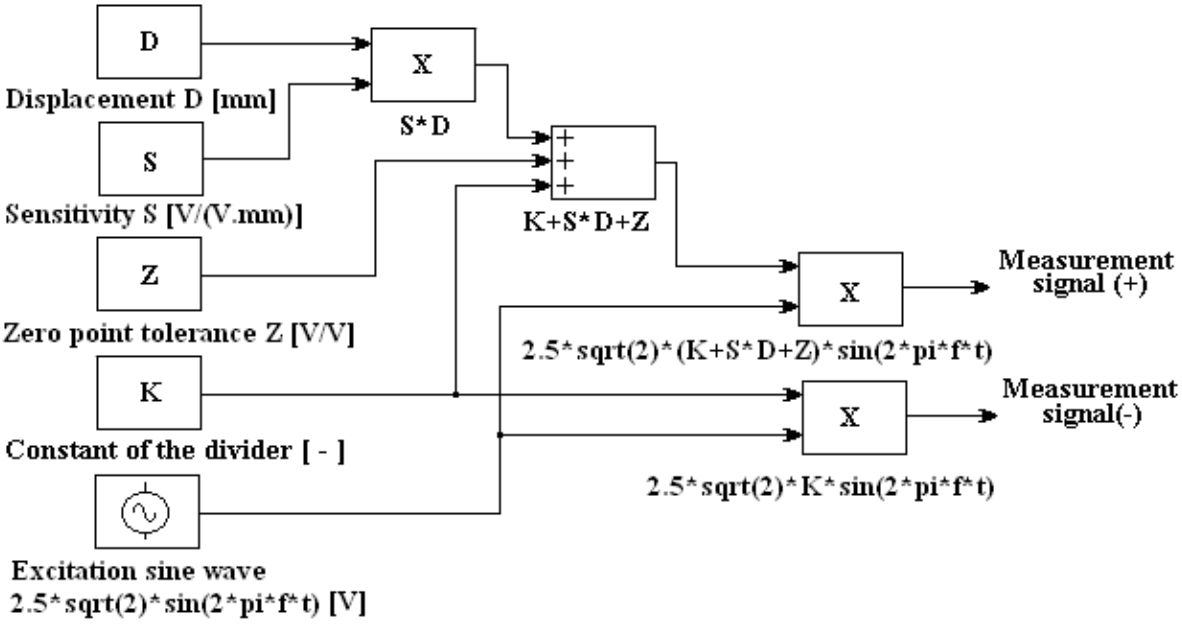

Fig.4. Simulink model of the IDT WA200 transfer characteristic.

Fig.4 proposes a Simulink model of the IDT WA200 transfer characteristic. The model is based on Equations (1) and (3). The simulation results for S=0.4 mV/(V.mm) and Z=0 mm/V are shown on Fig.5. The input signal (which represents the displacement D) varies from 10 to 200 units. As a result, the information signal appears with amplitude directly proportional to the displacement.

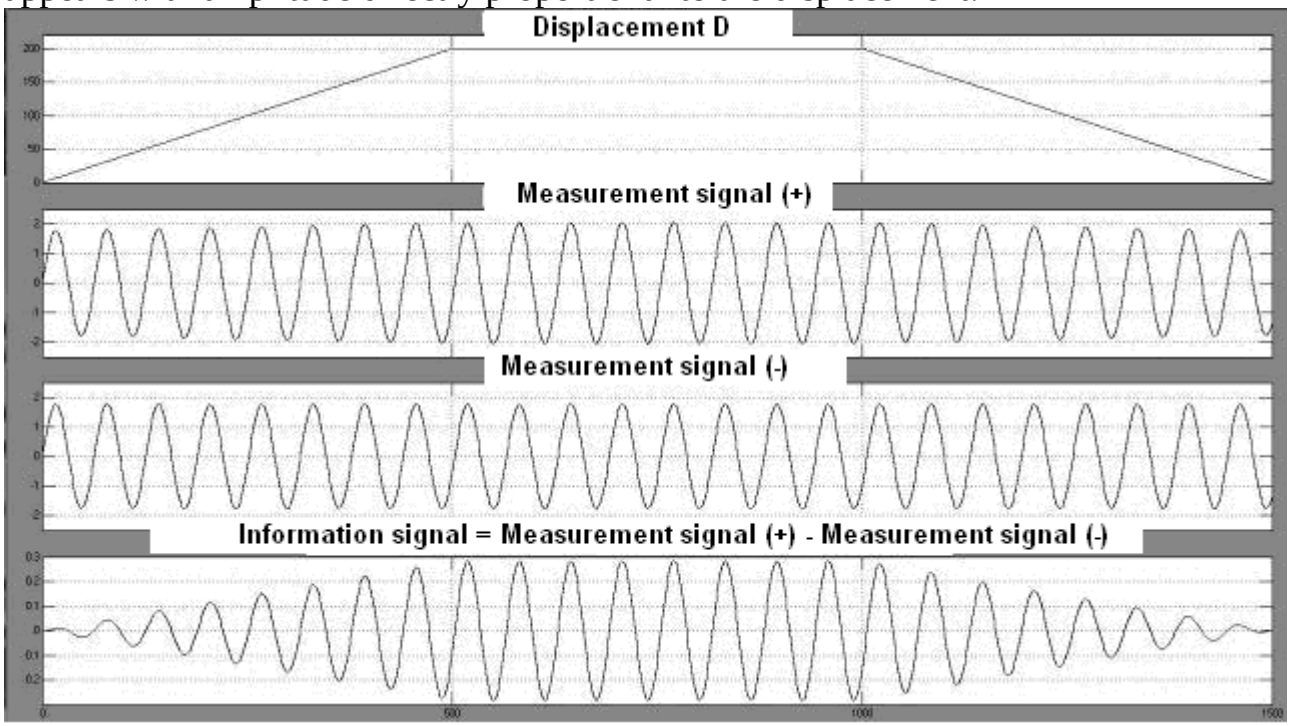

Fig.5. The input (Displacement) and differential output signals for the Simulink model of IDT WA200.

3. SIMULINK MODEL OF THE SIGNAL CONDITIONING CIRCUIT

The signal conditioning circuit is utilized to extract the information for the displacement from the signal at the outputs of the IDT. To achieve that, the value of the amplitude of the u_{diff} voltage (see Equation (4)) should be determined first. After that, displacement D can be computed.

Two basic methods for determining the displacement D are examined in [4]. The first method employs analog rectifiers and low-pass ripple smoothing filters to process the output voltage. The second method utilizes a demodulation approach in which the differential output of the IDT is sampled at a high frequency (about 20 samples per cycle of the 4.8 kHz excitation oscillator). The samples are converted to an integer data sequence, which is then processed by a demodulation algorithm. The comparison of the results from the investigations of both methods demonstrates that the method utilizing analog rectifiers exhibits better performance parameters and sensitivity [4].

The Simulink model for the signal conditioning circuit based on analog rectifiers is proposed on Fig.6. Fig.7 presents the results from simulations of the sensor block, which consists of IDV sensor and signal conditioning circuit. The input signal (displacement D) changes between 0mm and 200mm. The two *Measurement signals* (see Fig.6) are fed to the half-wave rectifiers, which reject the negative cycle of the signals and at each output positive half-wave signals appear that are to be subtracted

from each other in the Subtract block. The output of the Subtract block is a positive half-wave voltage with an amplitude A_{OUT} equal to:

(5) $$A_{OUT}[mV] = 2.5\sqrt{2}(S \cdot D + Z).$$

The subsequent low-pass filter delivers a DC voltage with a value of:

(6) $$U_{DC}[mV] = \frac{A_{OUT}}{\pi} = \frac{2.5\sqrt{2}(S \cdot D + Z)}{\pi}.$$

Then the displacement D can be determined solving Equation (6):

(7) $$D[mm] = \frac{\pi U_{DC}}{2.5\sqrt{2} \cdot S} - \frac{Z}{S}.$$

Equation (7) is implemented by Slope compensation and Y-intercept compensation blocks (see Figure 6). The coefficients for the Slope and Y-intercept compensation are determined in advance and are included as constants. The goal is to obtain the displacement D as an output DC voltage with 10mV corresponding to 1mm of displacement.

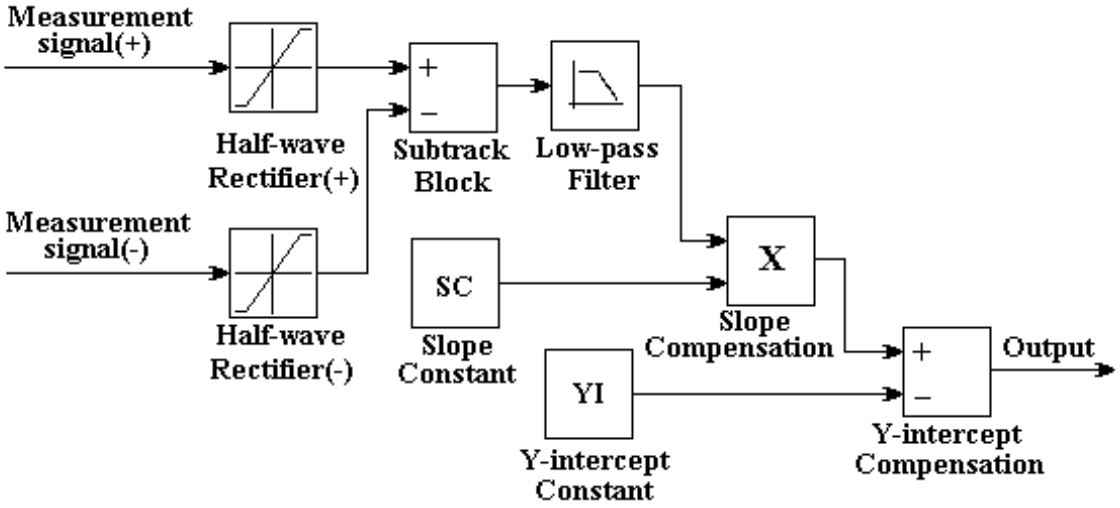

Fig.6. Simulink model of signal conditioning circuit

The developed models permit in-depth analysis of the behavior of the signal conditioning block for different values of the sensitivity S, the zero point tolerance Z and of combinations thereof. For instance, based on the simulations, the pass-band cut-off frequency of the low-pass filter was determined experimentally to be 500 Hz. In this case the output voltage settles at a correct value within 16 cycles of the excitation signal, i.e. about 3.3 ms after the moment of the changing the core position (see Fig.7).

4. CONCLUSION

This paper presents a systematic process for developing and examining of Simulink models for Inductive Displacement Transducer (IDT) and signal conditioning circuit. Using the basic specifications of WA200 transducer a Simulink model was developed, which represented very closely the functional behavior of the sensor. Second, a Simulink model based on dual half-wave rectifiers was developed to simulate the behavior of the signal conditioning circuit. The results from the

simulations of sensor block, which consists of IDT and sensor conditioning circuit, confirmed the effectiveness of the proposed models. The obtained results can be directly utilized in the design and verification of different signal conditioning circuits for ASICs and SoCs.

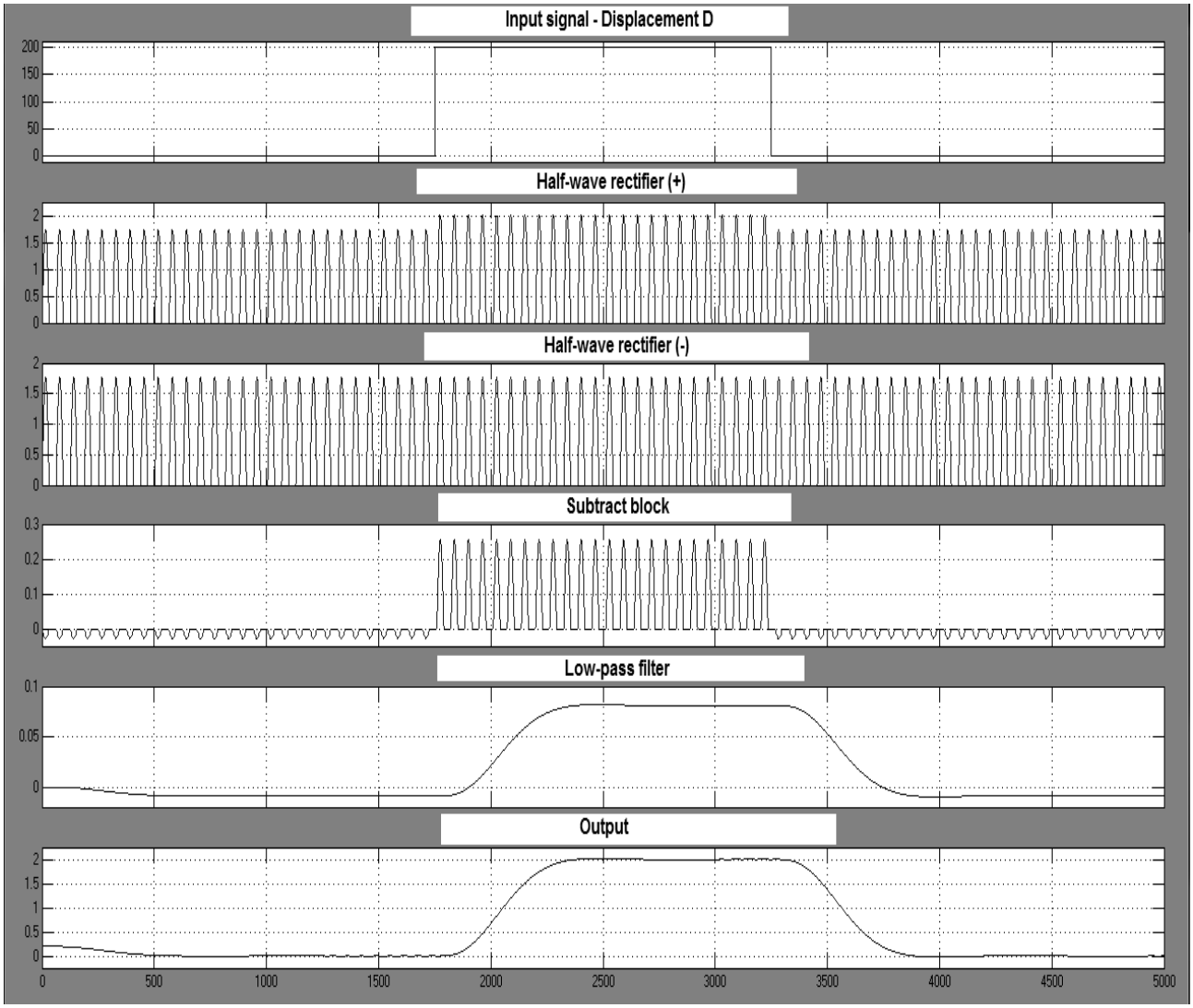

Fig.7. Results from simulation of the sensor block

5. ACKNOWLEDGMENTS

The research presented in this paper was co-funded by the Internal Competition Project of TU-Sofia, 2008.

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