DEVELOPMENT OF PARAMETERIZED CELL OF SPIRAL INDUCTOR USING SKILL LANGUAGE

Vladimir Emilov Grozdanov[1], Diana Ivanova Pukneva[1], Marin Hristov Hristov[2]

[1]Smartcom, 7th km, Tzarigradsko Chausee Blvd, 1784 Sofia, Bulgaria, Phone: +359 24009189, E-mail: vladimirgrozdanov@gmail.com, diana_pukneva@smartcom.bg
[2]Department of Microelectronics, Technical University of Sofia, 8 Kliment Ohridski St., 1797 Sofia, Bulgaria, phone: +359 29652220, e-mail: mhristov@ecad.tu-sofia.bg

In this paper is presented a method to facilitate the process of design RF circuits and systems using standard industrial CAD system CADENCE. Parameterized cell of square spiral inductor is proposed. It is created using built in Cadence language – SKILL. The use of a standard cell where the geometry parameters of the inductor can be set and change whenever necessary makes the design of inductors and their application in bigger circuits faster and easier and allows much more flexibility. In addition Spectre model is integrated in it, based on the well-known physical model of spiral inductor. Physical verification rules that extract the real parameter from the layout are also written in order to make the parameterized cell complete.

Keywords: CAD, Microelectronics, SKILL, p-cell, inductors

1. INTRODUCTION

Cadence® SKILL is a high-level, interactive programming language based on the popular artificial intelligence language, Lisp [1]. Because it supports a more conventional C-like syntax, users can learn to use it quickly, and expert programmers can access the full power of the Lisp language. SKILL is the command language of the Cadence environment. Whenever a menu or bind-key is used Cadence software triggers SKILL functions to complete the task. SKILL is easy to use not only to perform simple computations, but also to solve complex design tasks. This built in language allows personalization, improvement and enhancement of CADENCE environment and functionality.

A parameterized cell, or *pcell* for short, is a graphic, programmable cell that allows creation of a customized instance each time the cell is placed. Thus, whenever the pcell is invoked an instance with different parameter can be placed. The pcell which is created is called a *master*. A master is the combination of the graphic layout that is drawn to make a cell and the parameters assign to it. Generally pcells can be created graphically as a master cell using CADNECE menus, and then compiled and stored in the database in the form of a SKILL procedure. But this method is rarely used. The easiest and more flexible way is to build up the pcells by directly coding them using SKILL language.

In the used AMS 0.35 um Si CMOS technology most of the devices (i.e. transistors, resistors, and capacitors) are offered as pcells. Unlike them spiral inductors are offered only as fixed geometry with certain values of inductance, operating

frequency. This limits their usability and application, when design RF integrated circuits with the given technology. In order to surmount this drawback, in this paper is presented a parameterized cell of square spiral inductor. The use of inductor as prepared, standard cell makes the design of spiral inductors and circuits for RF applications, which need inductors to function properly, faster and easier.

2. PARAMETERIZED CELL OF SPIRAL INDUCTOR

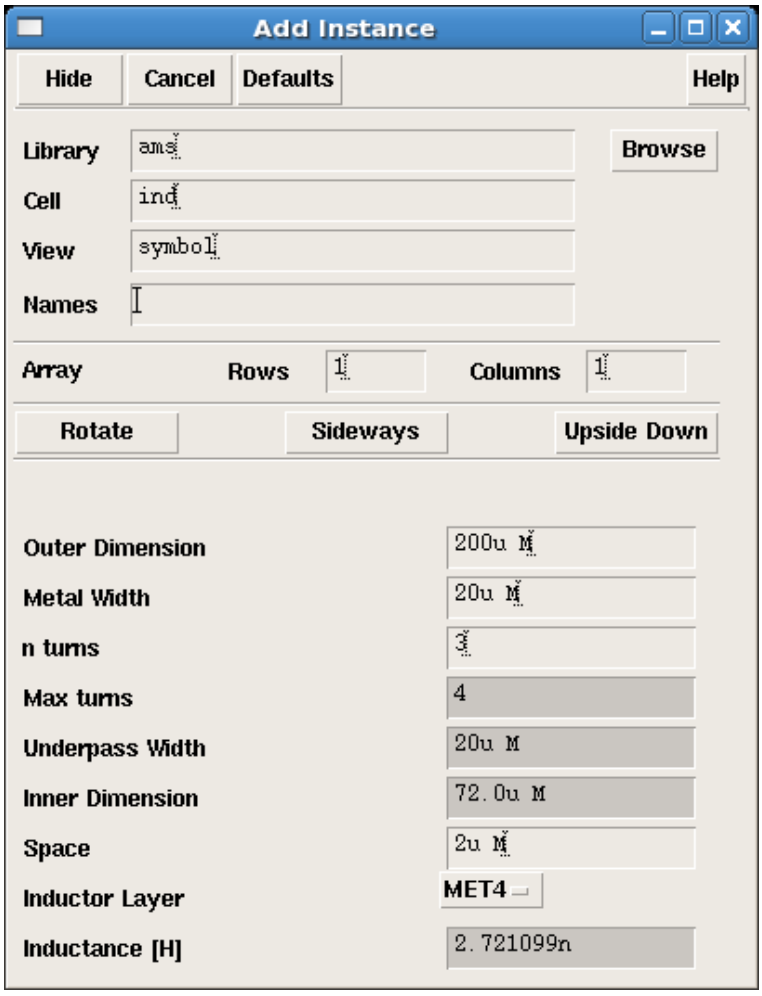

Fig. 1. CADENCE graphical user interface showing the CDF parameters of square spiral inductor

In most of the advanced technologies inductors are created by defining their geometry parameters. The same methodology is used in the proposed pcell. The following geometry and technology parameters are used to describe the inductor: outer dimension of the square inductor (*dout*), metal width of the spiral turn (*w*), space between adjacent turns (*s*), number of turns (*n*), maximum number of turns (n_{max}), inner dimension of the spiral (*din*), inductor layer – metal layer on which the spiral is created (layer) and underpass width (*wu*) – the width of the metal that connects the exit of spiral from the innermost turn. This set of parameters is attached to the pcell as CDF (Component Description Format) parameters and gives a full control over the geometry of the inductor. They will be used in the schematic view to create the symbol of spiral inductor which can be used for simulation purposes or in the layout view for automatic generation of spiral inductor layout.

In Fig. 1 is shown CADENCE graphical user interface used to invoke created parameterized cell of the spiral inductor, where the geometry parameters can be set.

The form is pre-filled with default values, which can be changed by the designer. Most of the described parameters are editable. Designer can choose the value of outer dimension, metal width and space, number of turns or which metal layer will be used to create the spiral inductor. As long as there is a limited number of metal layers (only four in the given technology), the layer parameter is defined as pull-down menu of choices (metal2, metal3 and metal4). Depending on the selected metal layer the underpass metal layer is defined automatically. Some of the parameters (highlighted in dark grey shades) are calculated based on the other parameter. For example, underpass width is set to be equal to metal width or the inner dimension is calculated from the outer dimension for the given space and number of turns.

Inductor parameters recalculated interactively, whenever a value is changed in one of the editable parameters fields. This is done using built-in SKILL procedures called *callbacks*. Every change in the value of editable parameter value triggers a callback function, which uses specific formulas to calculate the dependent parameter values. Maximum number if turns parameter is informational only. It shows what is the maximum possible number of turns for a spiral with the given outer dimension, metal width and space.

Inductance of the spiral is calculated using modified Wheeler formula (1) [2]:

$$L_{mw} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho}, \quad (1)$$

where ρ is density parameter given with the ratio between outer and inner dimension - $\rho = \frac{dout}{d_{in}}$, while K_1 and K_2 coefficients, which depend on the form of the spiral inductor.

For a square spiral they are 2.34 and 2.75, respectively.

```
(
 (dout  "string" "200u")
 (w     "string" "20u")
 (n     "float"  3.0)
 (nmax  "float"  4.0)
 (wu    "string" "20u")
 (din   "string" "72.0u")
 (s     "string" "2u")
 (layer "string" "MET4")
 (L     "string" "7.226069n")
)
```

Fig. 2. Fragment of SKILL code which set up default values for inductor pcell

In addition each and every CDF parameter has limitations defined by its callback function. This is made to restrict the input only to correct values. The first time, when inductor pcell is invoked the form is pre-filled with default values set with the following code (Fig. 2).

3. SCHEMATIC VIEW OF INDUCTOR PCELL

When the form from Fig. 1 is filled with the desired values and the symbol is placed in the schematic parameters *cdsParam* from Fig. 3 are replaced with outer dimension, metal width, space, number of turns and inductance name and values entered.

Thus, with addition of a model, inductor with the specified geometry can be investigated using different circuit simulator integrated in CADENCE. In order to do that a model described in the input language of Spectre circuit simulator is created. It is based on the physical model of spiral inductor [3] shown in Fig. 4.

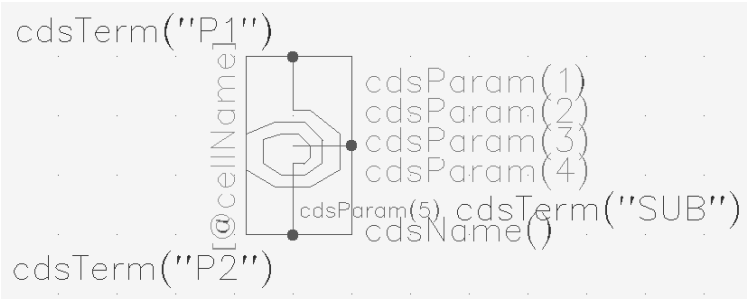

Fig. 3. Symbol view of the inductor pcell

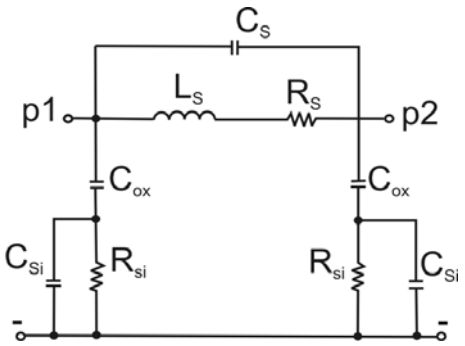

Fig. 4. Physical model of spiral inductor

The input data for the model are the CDF parameters of the cell – geometry parameters, layer, and inductance value. For every metal layer from the list of choices in the model is set metal thickness and metal conductivity. Resistances and capacitance from the model are calculated in the model using the equations published in [4].

4. LAYOUT VIEW OF INDUCTOR PCELL

In Fig. 5 is presented CADENCE graphical user interface used to visualize the generated layout of the square spiral inductor pcell.

The layout created from the cell for the given geometry parameter can also be seen. The inductor is drawn on the selected layer (i.e. 4th metal layer). This layer determines the type of vias used, the layer of the underpass and the layer for definition of terminals. Standard technology via cells are used in the pcell. The underpass layer is automatically selected as one layer below layer on which the inductor turns are created. The terminals are placed on the same layer as the inductor turns.

Additionally when the layout of the pcell is created a guard ring is drawn around the inductor. Its coordinates depend on d_{out} and w parameters. The ring is created using p+ diffusion, metal1 and contacts between diffusion and metal1. In addition some other inductor recognition shapes on different layers are added to the layout in order to facilitate inductor extraction and verification.

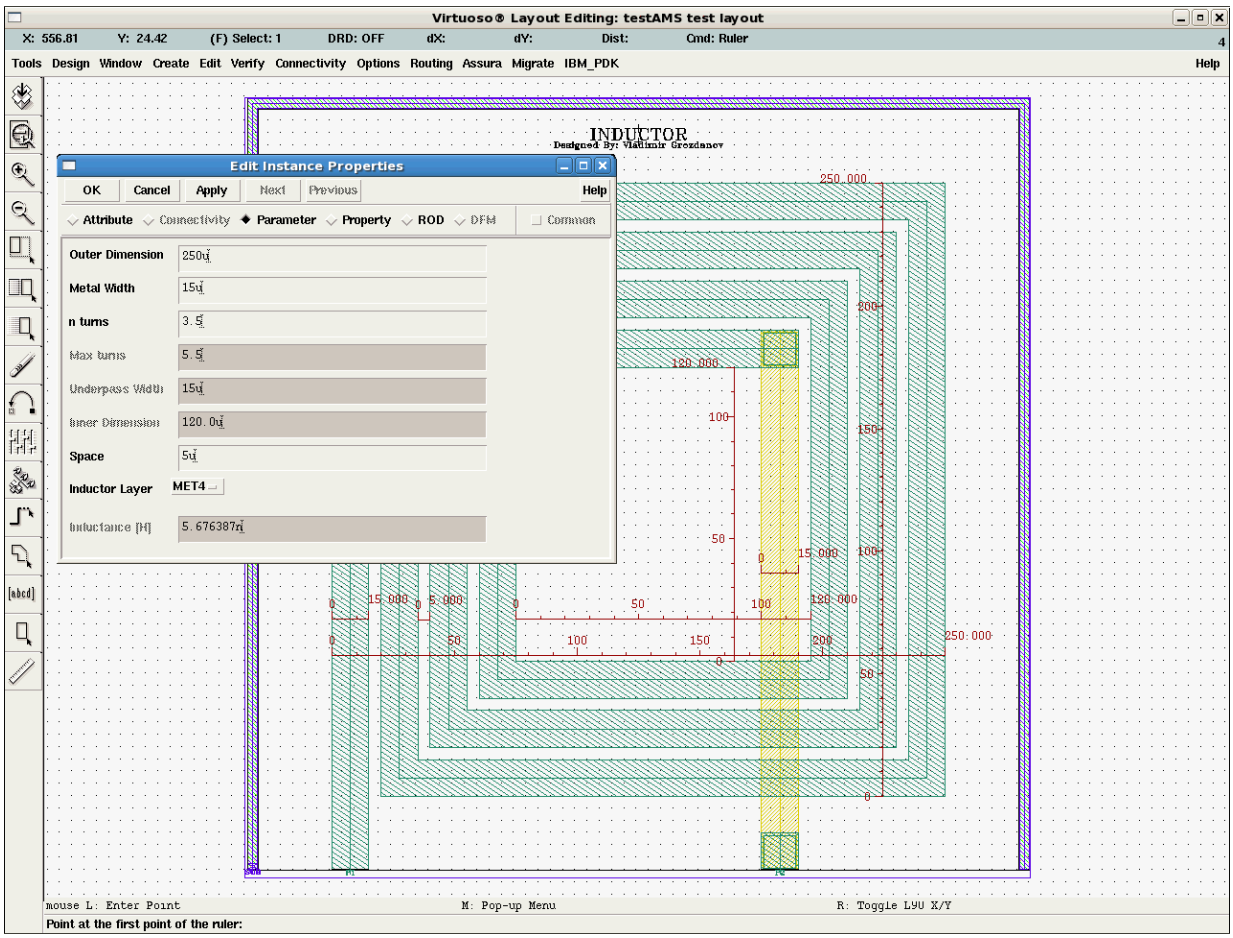

Fig. 5. Layout view generated from the inductor pcell and CADENCE graphical user for the layout view

In order to complete the design cycle with the proposed pcell of spiral inductor, extraction rules are written for it. These rules are coded for Calibre LVS, physical verification of Mentor Graphics, which is easy to integrate in CADENCE design environment. Extraction code uses Calibre built-in SVRF (standard verification rule format) language [4].

Tools like MATLAB can be used to optimize the geometry parameters of spiral inductors [5]. With the proposed pcell such optimized values can be entered directly in CADENCE and used to facilitate the design process.

5. CONCLUSIONS

In this paper is presented parameterized cell of square spiral inductor. SKILL language is used to create the pcell in CADENCE environment for AMS 0.35 um Si CMOS technology. The cell can generate automatically the layout of inductors with the desired geometry parameters. It has symbol view and model attached to it, which can be used to study inductor parameters with simulation. Extraction rules files are also written and can be used for physical verification of the pcell.

In the future, it is possible to continue with the optimization of the presented pcell with addition of octagonal form and support for not only single layer inductors, but also double or multilayer devices.

6. ACKNOWLEDGEMENT

The research presented in this paper is part of a project supported from fund "Scientific Research" at Ministry of Education and Science, contract №BY–TH 115/3 2005.

7. REFERENCES

[1] Cadence® Design Systems, Inc., SKILL Language User Guide, September 2005.

[2] Mohan, S., M. Hershenson, S. Boyd, and T.H. Lee, "Simple Accurate Expressions for Planar Spiral Inductances", IEEE Journal of Solid-State Circuits, vol. 34, No. 10, Oct. 1999, pp.1419-1424.

[3] Yue, C. P., S. S. Wong, Physical Modeling of Spiral Inductors on Silicon, IEEE Transactions on Electron Devices, March 2000, Vol. 47, No. 3, pp. 560-568

[4] Mentor Graphics Corp., Standard Verification Rule Format Manual, June 2003

[5] Gadjeva, E. D., V. P. Durev, M. H. Hristov, D. I. Pukneva, Optimization of Geometric Parameters of Spiral Inductors Using Genetic Algorithms, Proceedings of 13th International Conference MIXDES 2006, Gdynia, Poland, June 2006, pp. 514-517, ISBN 83-922632-1-9.