SPICE SIMULATION OF THE CONTROL SYSTEM FOR FREQUENCY REGULATED TRANSISTOR RESONANT INVERTER

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The paper subject of research is synthesis and SPICE simulation of a system for frequency control and regulation of series resonant transistor inverter. A characteristic feature of the system is the tracking of an only one synchronization signal. That is the current in the resonance loop. This approach is extremely preferable when the heat station (HF coupled transformer, tank capacitor and inductor) is distanced from the energy unit. Adaptive dead time control is incorporated in the system, which is a function of the current through the switches at the moment of commutation. The control system automatically limits its minimal working frequency, supporting a minimal commutation lead time of transistors, before the zero-crossing of the current through them. This ensures ZVS in the whole frequency range.

Keywords: Transistor resonant inverters, Spice simulation, Control system

1. INTRODUCTION

The contemporary power MOSFET and IGBT transistors replace successfully the thyristors in the inverters for induction heating. The specifics of the power transistor commutation require some changes in the modes of operation of these inverter classes. The works of several authors is devoted to this topic. A comprehensive investigation of the modes of operation of the series bridge transistor inverters is made in [1]. The present paper is devoted to a variant of a system for frequency control and regulation of this inverter class. The aim of this work is to propose a more inexpensive variant of the self-oscillating system, considered in [2]. The voltage controlled oscillator incorporated in the widespread PLL integrated circuit 4046 [3] is used for the frequency control. The adaptive dead time is realized according to the principle, developed in [4].

2. PRINCIPLE OF OPERATION AND SIMULATION OF THE POWER CIRCUIT AND THE CONTROL SYSTEM

The circuit of the full bridge transistor series resonant inverter is shown in Fig. 1. The dependent voltage controlled voltage sources Eg1-Eg4 serve as drivers for the power transistors Q1-Q4. Their gain GAIN=3 matches the signal levels of the logical elements in the control system with the signal levels at the transistor gates. The resistor Rcs and the dependent voltage source build the current feedback – Vcs. The

resistor divider RQ1, RQ4 (RQ2, RQ3) forms a positive pulse Q14 (Q23) according to the potential Ndc, when the upper transistor Q1 (Q2) is turned-on. Q13 (Q23) is negative with respect to Ndc, when a lower transistor Q4 (Q3) is turned on. Q13, Q23 and Ndc are the leading signals for the adaptive dead time circuit [4].

The circuit of the voltage controlled oscillator VCO and the driver of control and synchronizing pulses is shown in Fig. 2. The signals, formed by this circuit, are shown in Fig. 3a and Fig. 3b.

The even (odd) power transistors (V(QP)/V(QN)) commutate by each rising pulse of V(CLK) and a standard minimal dead time V(Rdt:2) is formed (Fig. 3e). The signal V(start) enables the work of the Gate drive pulse distributor (Fig. 4). The signal V(E_adt)=0 enables the work of the circuit, forming the adaptive dead time (Fig. 5). Its function is seen from the simulation results shown in Fig. 3d.

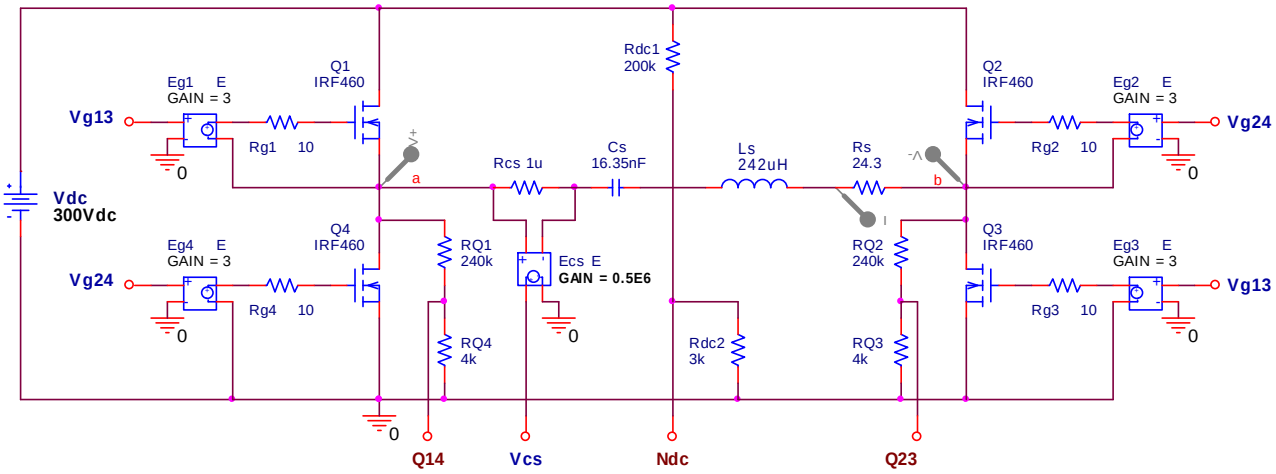

Fig.1. Full bridge transistor series resonant inverter

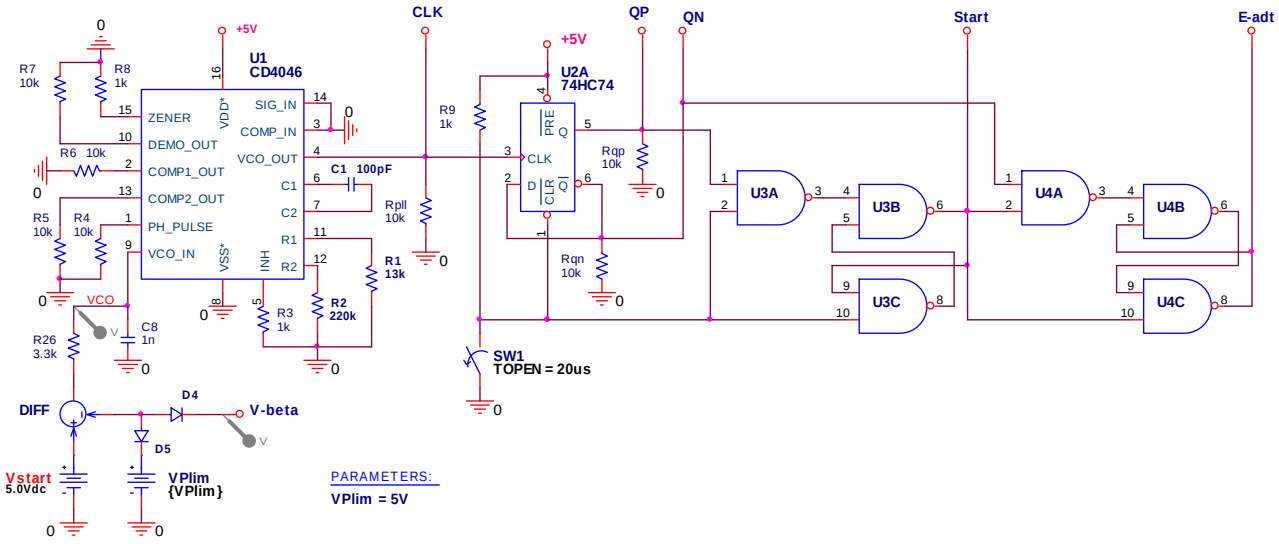

Fig.2. Voltage controlled oscillator VCO and driver of control and synchronizing pulses

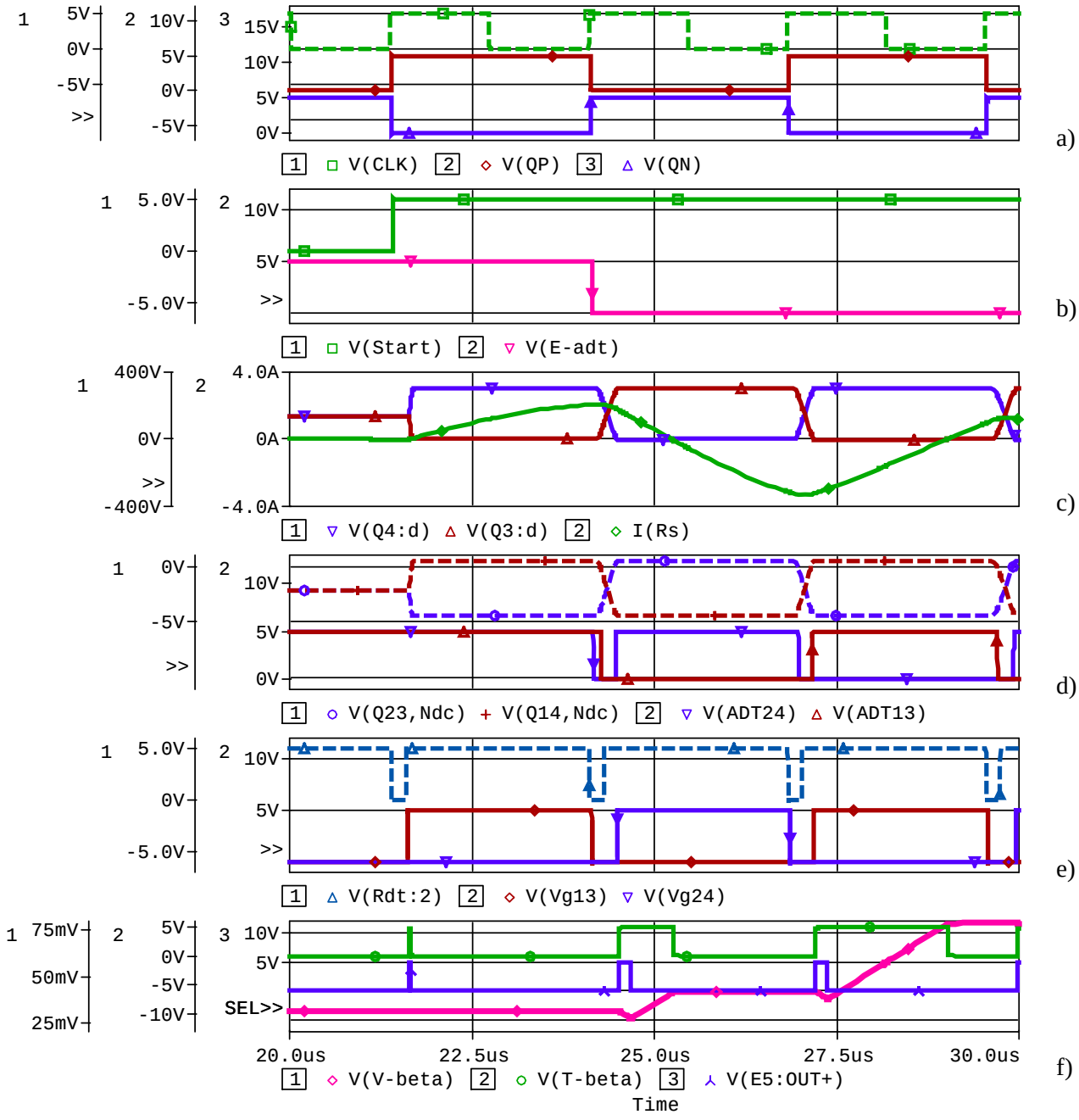

Fig.3. Principle of work of the system for control and regulation

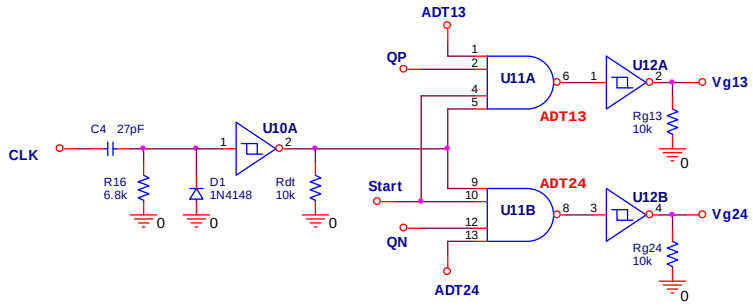

Fig.4. Gate drive pulse distributor

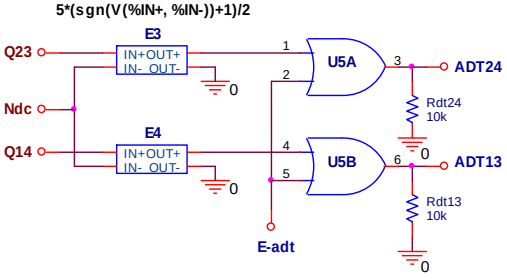

Fig.5. Adaptive dead time

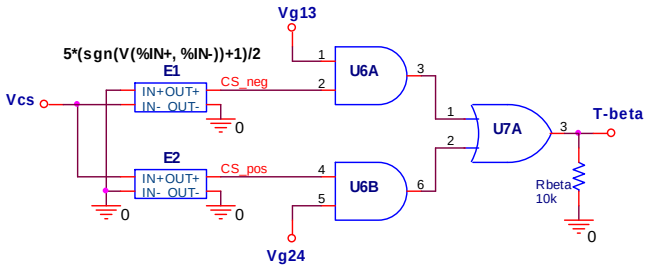

Fig.6. Lead time

The leading commutation of the power transistors (V(Q4:d)/V(Q3:d)) is seen in Fig. 3c according to the changing of polarity of the resonant current I(Rs). For this time interval, the pulse V(T-beta), is formed from the circuit for lead tracking (Fig. 6). This pulse is presented in Fig. 3f. It is applied to the input of the leading time regulator T-beta (Fig. 7).

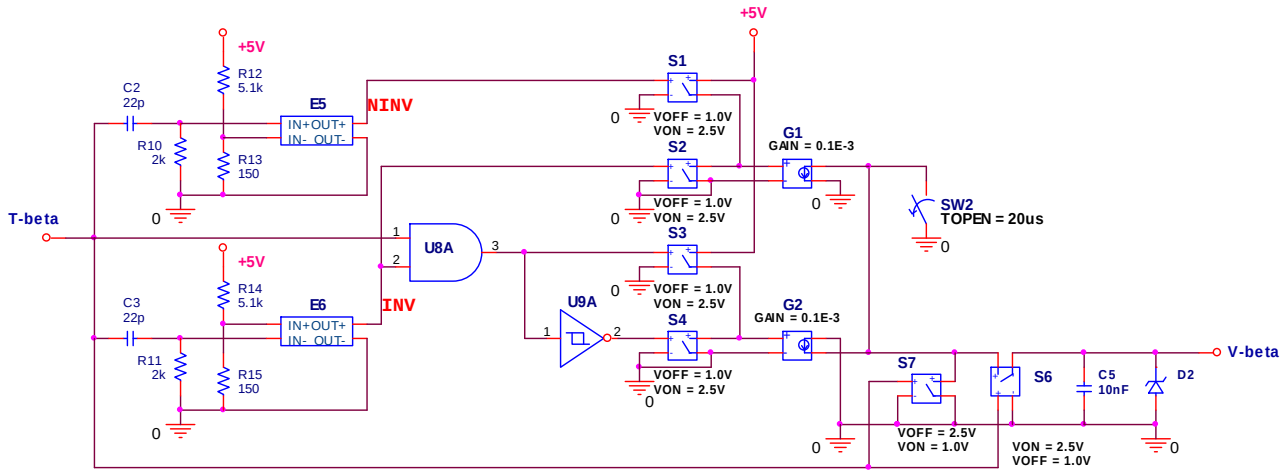

Fig.7. Regulator of the lead time T_{beta}

The work of this regulator is according to the principle of double integration. Reference signals of opposite polarity are formed at the outputs of E5 and E6 which duration is a half of the desired leading time. Only the positive pulse is shown in Fig. 3f (V(E5:OUT+)). The measured lead time, together with the reference time, commutate the current sources G1 and G2. During the reference pulse V(E5:OUT+), the capacitor C5 discharges and for the remaining of the measured lead time (V(T-beta)-V(E5:OUT+)) C5 charges. Outside of the measured lead time, C5 is switched off from the regulator circuit by the dependent switches S6 and S7. The voltage on C5 –V-beta, applied to the differential summer DIFF through the diode D4, regulates the frequency of VCO (Fig. 2). If the measured lead time is exactly equal to the doubled reference time, V-beta will remain unchanged. If T-beta is more than the doubled reference time, V-beta arises. As a result, the frequency of VCO decreases.

3. Result of the Simulation of Transients

The series resonant circuit Cs Rs Ls is sized for the working frequency 80 kHz, power 3 kW for quality factor Q = 5 and power supply Vdc = 300 V.

The variations on the time of the following quantities are shown in Fig. 8: the load power Pac, the load current I(Rs), the voltage V-beta, regulating the lead time, and the voltage, regulating the frequency of the VCO. By the start V-beta=0 and V(VCO)=Vstart (Fig.2).

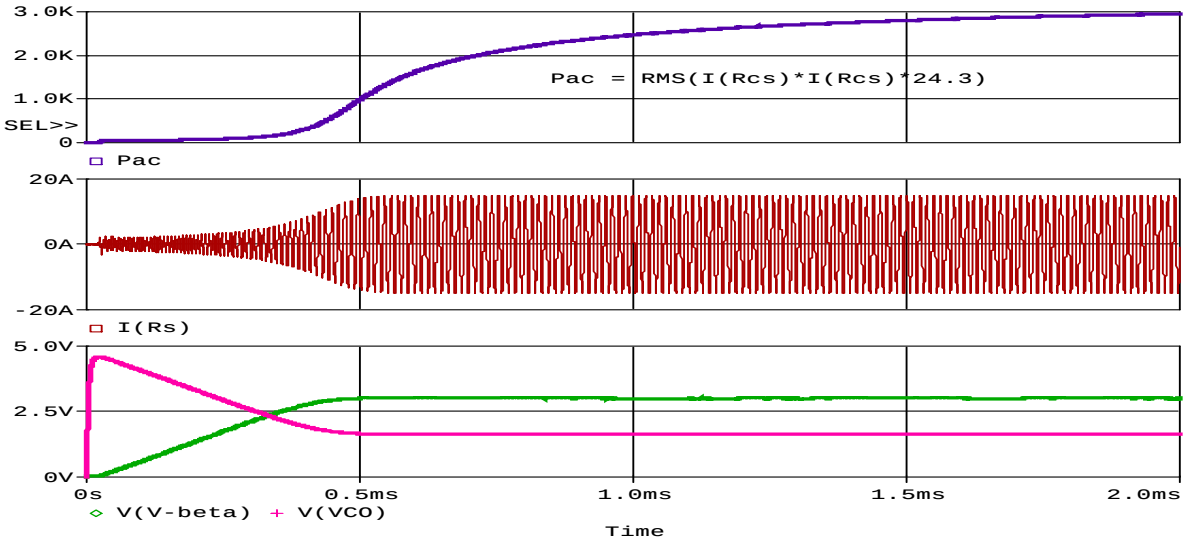

Fig.8. Transients

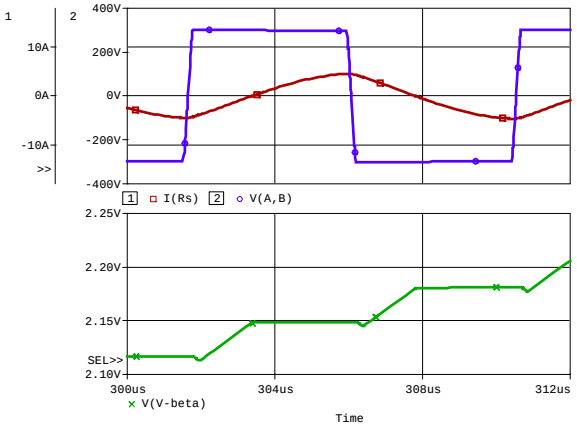

Fig.9. Beginning of the transients

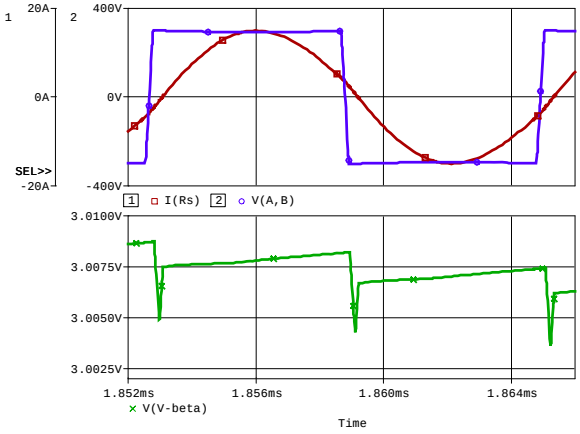

Fig.10. Ending of the transients

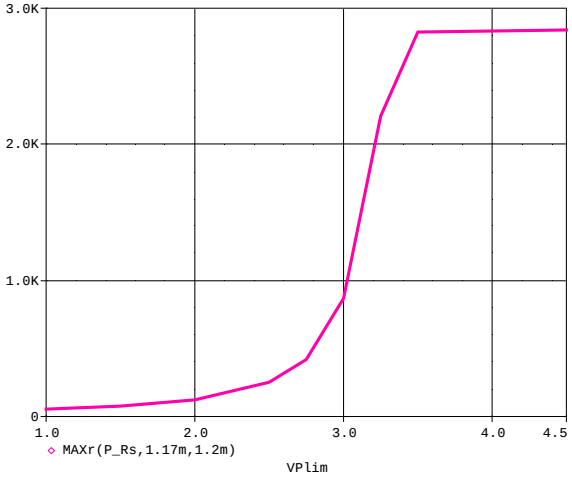

Fig. 11. Results of the parametric analysis

The inverter works by a large detuning and V-beta begins to increase (Fig. 9). This leads to decreasing the working frequency, respectively the lead time. The voltage V-beta is shown in Fig. 10 at the end of the transient process, in the state of a weak over-regulation (the measured lead time is less than doubled reference time).

The transient is simulated for the voltage VPlim=5V, which does not limit the load power. If VPlim<5 V , the load power could be limited at the lower level than the nominal one. The results of this parametric analysis are shown in Fig. 11.

4. CONCLUSION

Synthesis and SPICE simulation of a system for frequency control and regulation of series resonant transistor inverter has been performed in the paper. Adaptive dead time control is incorporated in the system, which is a function of the current through the switches at the moment of commutation. The control system automatically limits its minimal working frequency, supporting a minimal commutation lead time of transistors, before the zero-crossing of the current through them. This ensures ZVS in the whole frequency range. The simulation results for the transients are presented. Using parametric analysis, the dependence of the load power on the limiting voltage is investigated.

5. ACKNOWLEDGEMENT

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6. REFERENCES

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