BEHAVIORAL MACROMODELING OF VOLTAGE FEEDBACK AMPLIFIERS

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This paper presents a new voltage feedback amplifier macromodel at behavioral level. It accurately models basic differential-mode and common-mode electrical characteristics, the input offset voltage and current, the differential-mode and common-mode amplification, the input voltage noise, the output voltage swing, short-circuit current and the input and output impedances. For creating the model, simplification and build-up techniques known from modeling operational amplifiers have been adapted. Model parameters are extracted for the OP177F from Analog Devices as an example. To confirm the validity of the proposed macromodel, simulation results are compared with the manufacturer's data and with the behavior of the SPICE-based macromodel OP177F/AD from the standard library. The proposed behavioral macromodel leads to a low analysis time, with higher accuracy and a better convergence in comparison with other op amps methods of modeling.

Keywords: analog circuit design, voltage feedback amplifier, behavioral modeling, simulation.

1. INTRODUCTION

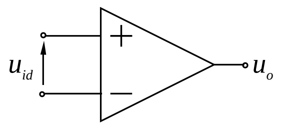
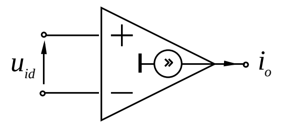
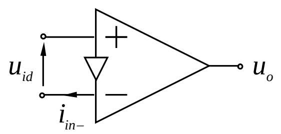
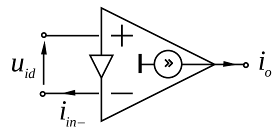
In the past decade, circuit simulation has taken on an increasingly important role within analog circuit design. The most popular simulation tool for this is PSpice, which is available in multiple forms for various computer platforms. However, to achieve meaningful simulation results, designers need accurate models of many system components. The most critical of these are realistic models for operational amplifiers (op amps), the active devices that drive modern designs. The main types of op amps used in practice, according to the transfer function, are presented in Table 1. Nowadays many producers offered voltage feedback amplifiers (VFAs), current feedback amplifiers (CFAs) and drive-R – amplifiers (or diamond transistors) as monolithic integrated circuits, while operational tranconductance amplifiers (OTAs), are generally presented as a part of complex electronic circuits. VFAs are very often used for realization of various electronic circuits and are presented in the PSpice standard libraries with simulation macromodels from different level of complexity. More than of CFAs and drive-R – amplifiers used *device- (transistor-) level models*, called micromodels. Typically, micromodels are used in the actual design process of ICs.

Verifying a complete analog system via transistor-level simulation is an extremely difficult process and can often become infeasible due to the limitation of simulation capacity. A similar difficulty is encountered when high-level design is performed for the whole system. For these reasons, compact macromodels of analog blocks, and in particular, op amps are desired which can be substituted in place of the actual transistor-level netlist to speedup the simulation without sacrificing any of the required accuracy.

One method to decrease simulation time and improve the convergence, without a significant loose of information, is by using behavioral macromodeling technique.

Macromodeling is a way of providing macroscopic models of the corresponding microscopic (microelectronic) circuits [1]. The use of behavioral macromodeling for op amps has been well known for a few years. Behavioral models are realized by using structural macromodeling, the C code modeling, AHDL (Analog Hardware Description Language) and finally the Analog Behavioral Macromodeling (ABM) build in PSpice A/D simulators [2].

Table 1. Basic types of operational amplifiers

	Input parameter - <u>voltage</u>	**Input parameter - <u>current</u>**
Input parameter - <u>voltage</u>	Voltage Feedback Amplifier – VFA (Voltage Controlled Voltage Source, VCVS)  $u_o = A_d u_{id}$	Operational Transconductance Amplifier – OTA (Voltage Controlled Current Source, VCCS)  $i_o = S_d u_{id}$
Input parameter - <u>current</u>	Current Feedback Amplifier – CFA (Current Controlled Voltage Source, CCVS)  $u_o = i_{in-} Z = A_d u_{id}$	Drive - R – Amplifier or Diamond Transistor (Current-Controlled Current Source, CCCS)  $i_o = k_I i_{in-} = S_d u_{id}$

Several behavioral macromodels for op amps have been developed and reported in the literature [3-6]. The behavioral macromodels proposed in [3] can significantly reduce the model complexity while still capturing the dominant linear and nonlinear response of the circuits, such as frequency characteristics, THD and gain compre-ssion. These Volterra-based models are presented as the nth order nonlinear transfer function but ignores the most of the second-order effects of op amps, such as input offset voltage/current, CMRR, accurate input/output impedance, noise, temperature effects, etc. There is another behavioral macromodel [4] developed by Wilson, Kilic, Ross, Zwolinski, and Brown, which simulates dc transfer function with different types of fault conditions. The macromodel is implemented with ADHL (for example with MAST language). The main advantage of the MAST modeling is that the language is integrated in the SABER simulator that needs no more to be recompiled and/or linked with the new model. The drawback is the leak of portability to the PSpice like simulators. The behavioral SPICE based macromodels of op amps, presented in [5] and [6] are based on a frequency domain description of the input-output transfer functions. They accurately models the frequency variations of the open-loop gain, the CMRR, the PSRR and the input/output impedance, by a direct specification of their Laplace domain expressions with all theirs dominant poles and zeros. These macromodels with a suitable choice of parameters and elements can be used for analog circuit simulations, but not confirm to the architectures of a broad class of op amps, such as current feedback amplifier (CFA), operational tranconductance amplifier (OTA) and drive-R – amplifier. Without any doubt behavioral macromodels for basic types op amps (voltage feedback amplifiers, current feedback amplifiers, tranconductance amplifier and drive-R – amplifiers), are necessary for simulating complex electronic systems. However, powerful behavioral models have not been available yet. In this paper and in [10] are introduces new behavioral models for basic types of op amps. For realization of proposed macromodels the ABM technique is used, because it's a serious competitor of the C code and AHDL modeling techniques, as it assumes a comparable accuracy, with a simpler and easier modeling procedure. The models presented in this paper are defined as a hierarchical blocks and can adequately present the typical electrical performances for dc, ac and transient responses, as well for a given op amp macromodels provides an essentially pin-for-pin correspondence with the actual device.

2. VFA MACROMODEL DEVELOPMENT

"*Perfection is achieved, not when there is nothing more to add, but when there is nothing left to take away*." Antoine de Saint-Exupery.

The technical requirement for effective models is generally agreed when is developed the simplest model possible. Simple models have a number of advantages. They can be developed faster, are more flexible, require less data, run faster and it is easier to interpret the results since the structure of the model is better understood. As the complexity increases these advantages are lost [7].

The proposed macromodels of op amps are developed following the design method based on a Top-Down analysis approach and applying simplification and build-up technique, known from modeling operational amplifiers. The process of model building and testing can be broken down into three steps: structure the model, build the model and validate the model [8].

The circuit diagram of the new VFA model is shown in Fig. 1, where the different stages are presented with ABM elements and passive components. The model parameters are given without concrete numerical values. During the modeling of a particular IC the numerical values are obtained by datasheet parameters for the actual device. The macromodels description of the current feedback amplifier (CFA) and drive-R – amplifier are presented in [10].

The equivalent circuit of the VFA model, shown in Fig. 1, is subdivided into three stages. *The input stage* consists of ideal independent current and voltage sources (Vio, Iib+, IiB- and Iio), linear controlled sources (Ecm, Gcm1, Gcm2, FN0, GN0, FN1, GN1 and HN), resistors (Rid, Ricm+, Ricm-, Rcm, RN0, RN1 and RX1), capacitors (Cid and CN1), as well inductor Lcm. The input stage represents basic linear differential-mode and common-mode electrical characteristics. In particular, the following exploitation parameters are modeled: *input offset voltage* (U_{io}), *input offset current* (I_{io}), *input bias current* (I_{iB}), *differential input resistance* (R_{id}), *common-mode input resistance (R_{icm}), common-mode rejection ratio (CMRR) versus frequency and noise voltage spectral density ($\overline{S}_U$).*

The differential input resistance R_{id} and capacitances C_{id} is measured between inverting and non-inverting pins of the input voltage source $EAMP1$ and produced by the elements R_{id}, R^{+}_{cm}, R^{-}_{cm} and C_{id}.

(1) $$R_{id} = R_d \parallel \left(R^{+}_{cm} + R^{-}_{cm}\right)$$

The common-mode input resistance R_{icm} is provided by the elements R^{+}_{cm} and R^{-}_{cm}.

(2) $$R_{icm} = R^{+}_{cm} \parallel R^{-}_{cm}$$

Input currents of the inverting and non-inverting pins is generated by current sources I^{+}_{B}, I^{-}_{B} and I_{io}, connected to node in+ and in-, respectively.

(3a) $$I_{in+} = I_{iB} + \frac{I_{io}}{2}$$ and

(3b) $$I_{in-} = I_{iB} - \frac{I_{io}}{2}.$$

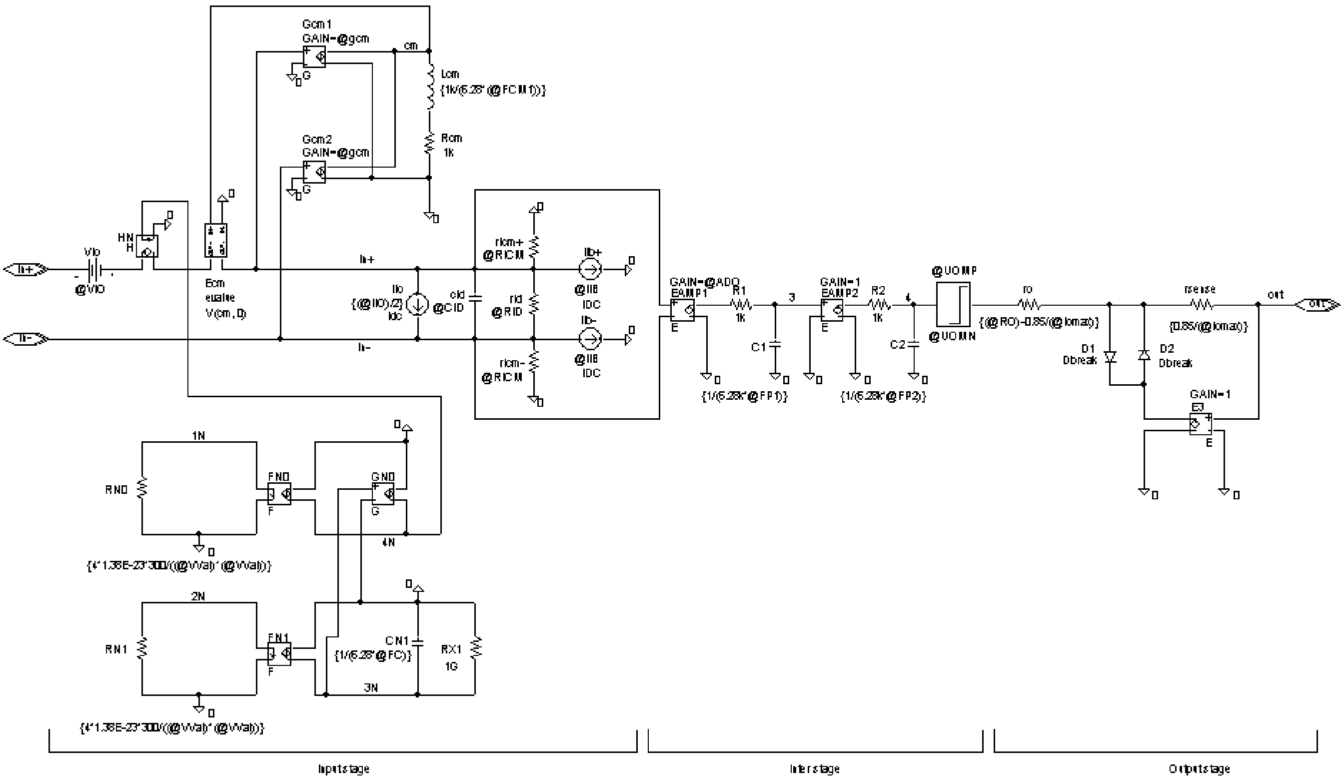


Fig. 1. Equivalent circuit of the voltage feedback amplifier macromodel.

The noise performance of VFAs has been represented on the basis of the definition of noise characteristics and analysis of IC datasheets. As it is shown in Fig. 1, the equivalent circuit of the input stage including noise generators that simulate the thermal (white) noise and 1/f noise (Flicker noise) of an actual VFA. The polynomial current-controlled voltage source HN reflects the error voltage from the additionally defined noise voltage stage (HN device convert the noise current into a voltage). The noise stages of the model consists two resistors RN0 and RN1 that generate white noise current, two current-controlled current sources FN0 and FN1, which are measure noise currents and RX1-CN1 - group defining the corner frequency of the 1/f noise. The *VVal* parameter used in the formula for the resistor value defined level of the white noise generated by the circuit. The rms voltage $\bar{e}_{N_o} = VVal$ is the white noise of the op amp per $\sqrt{Hz}$ and can be found by

(4) $$\bar{e}_{N_o} = \sqrt{\bar{e}^2_{N,DS} - \bar{e}^2_{N,\mathrm{Res}}}$$

where the rms voltage $\bar{e}_{N,DS}$ is the datasheet value of the white noise per $\sqrt{Hz}$ and the rms voltage $\bar{e}_{N,\mathrm{Res}}$ is the white noise generated by large-value resistors commonly used in macromodels.

The Flicker noise effect is modeled by resistors RN0 and RN1, and RX1-CN1 – group. The white noise currents from resistors RN0 and RN1 is injecting into a capacitor CN1 and this will produce a noise voltage that decreases with frequency as the capacitor shunts the noise current. Injecting a current into an ideal capacitor does not provide dc path for connecting node, so a large-valued resistor RX1 is used to provide dc path. The resistor $RX1 = 10^9\,\Omega$ will produces current noise less than $5.10^{-15}\,A/\sqrt{Hz}$ for any earthly temperature. Also the corner frequency FC is given in the formula for the capacitance CN1.

The middle stage represents the ac small-signal transfer function of the real op amp. The differential-mode voltage gain is provided by the linear voltage-controlled voltage source EAMP1. This voltage source with its dc gain Ado is controlled by the differential input voltage *V*(in+, in-). The poles and zeros that are necessary to precisely shape the magnitude and phase response of the model are presented by two frequency-shaping RC or RL stages (R1-C1-EAMP2, R2-C2-limit1 and Rcm-Lcm-Gcm1-Gcm2). Each of those frequency-shaping stages have unity dc gain making it easier to poles and zeros without changing the dc gain of the model. The differential-mode ac transfer function is

(5) $$\dot{A}_d = \frac{A_{do}}{\left(1 + j\dfrac{f}{f_{p1}}\right)\left(1 + j\dfrac{f}{f_{p2}}\right)},$$

where f_{p1} and f_{p2} is the $-3dB$ frequencies for the dominant and second pole of the VFA, respectively.

The CMRR versus frequency is produced by the elements Gcm1, Gcm2, Ecm, Rcm and Lcm. Empirically, a value of Rcm is chosen equal to $1k\Omega$. The current sources Gcm1 and Gcm2 are chosen linear one-port generators having the following equations:

(6a) $I_{G_{cm1}} = g_{cm} U(in+,\ 0)$ and

(6b) $I_{G_{cm2}} = g_{cm} U(in-,\ 0)$,

where $U(in+,\ 0) = U(in-,\ 0) = U_{cm}$ is the common-mode input voltage and g_{cm} is the transconductance of controlled sources Gcm1 and Gcm2. The current thus generated

$I_{G_{cm1}}$ and $I_{G_{cm2}}$, will flow through the resistor R_{cm} and inductor L_{cm}, towards the internal ground. In such a way the voltage $U(cm,\ 0)=(I_{G_{cm1}}+I_{G_{cm2}}).Z_{cm}=2g_{cm}U_{cm}Z_{cm}$ ($Z_{cm}=R_{cm}+j\omega R_{cm}L_{cm}$ − equivalent impedance at node *cm*) will depend upon the amplitude of the common-mode input voltage. The voltages generated at node cm are used for forming the equation of input voltage-controlled voltage source E_{cm} as follows:

(7) $U_{E_{cm}}=k_{1,E_{cm}}U(cm,\ 0)$.

For convenience, the coefficient $k_{1,E_{cm}}$ of the controlled source E_{cm} is selected equal to unity. Then the output voltage of the stage, predicted by the input common-mode voltage is

(8) $\dot{U}_4=2\dot{A}_d\dot{U}_{Ecm}=2\dot{A}_d g_{cm}Z_{cm}\dot{U}_{cm}$.

The common-mode gain can be found with the following equation:

(9) $$\dot{A}_{cm}=\frac{\dot{U}_4}{\dot{U}_{cm}}=2\dot{A}_d g_{cm}Z_{cm}.$$

The CMRR is the ratio of the differential-mode gain and common-mode gain, i.e.

(10) $$|CMRR|=\left|\frac{\dot{A}_d}{\dot{A}_{cm}}\right|=\frac{1}{2g_{cm}Z_{cm}}=\frac{1}{2g_{cm}R_{cm}\sqrt{1+\left(\frac{f}{f_{cm1}}\right)^2}},$$

where f_{cm1} is the $-3dB$ frequency for the dominant pole of the VFA.

The output stage of the VFA macromodel provides, proper dc and ac *output resistance* ($R_{o,DC}, R_{o,AC}$), *output voltage swing* (U_{omp} and U_{omn}) and *maximum output current* ($I_{o\max}$). The output stage consists of a voltage follower, realized with voltage-controlled voltage source Elimit, short-circuit current limiting stage (E3, D1-D2 and Rsense) and resistor Ro simulates output resistance which determines the behavior of the model when driving heavy loads. The parameters UOMP and UOMN of the voltage source Elimit produce the desired maximum voltage excursion.

3. The OP177F Macromodel

In this section, a numerical example is used to illustrate the development of the parameters of the VFA macromodel. For the example, the electrical characteristics and parameters of the OP177F VFA are used [9]. The OP177F is a ultra precision op amp consisting of bipolar input differential stage with low input offset voltage typically $10\mu V$ and high differential-mode gain with value 12,000 V/mV. In fact OP177 is typical representative of the precision voltage-feedback amplifier topology using the most contemporary op amps implementation. In Table 2 model parameters for the op amp OP177F are presented. The numerical values are obtained by data-sheet parameters for the actual device and by calculation using equations given above.

Table 2. VFA macromodel parameters

Input stage	Middle stage
$RID = 45M\Omega$	$ADO = 12.10^6$
$CID = 4pF$	$FP1 = 0{,}05Hz$
$RICM = 200G\Omega$	$FP2 = 10MHz$
$VIO = 10\mu V$	Output stage
$IIB = 1{,}2nA$	$UOMP = +12{,}5V$
$IIO = 0{,}3nA$	$UOMN = -12{,}5V$
$gcm = 50pS$	$Io\max = 25mA$
$FCM1 = 25Hz$	$RO = 60\Omega$
$RCM = 1k\Omega$	
Noise stage	
$VVal = 9{,}13nV/\sqrt{Hz}$	
$FC = 1{,}3Hz$	
$RX1 = 1G\Omega$	

Validation checks have been performed on the VFA macromodel (VFA_lin) developed through simulation modeling of the dc, ac and transient modes of operation of the real device. In Table 3 is given comparison between VFA_lin macromodel parameters, OP177F/AD macromodel from standard PSpice library and datasheet parameters. Notice that the average error between VFA_lin macromodel and datasheet parameters is not higher than 5%, which guarantee the correct degree of accuracy.

Table 3. VFA performance characteristics ($T_A = +25°C$, $V_{CC} = \pm 15V$ and $R_L \geq 2k\Omega$)

Parameter	Conditions	VFA_lin macromodel	OP177F/AD macromodel	OP177F data sheet
DC performance				
Input offset voltage	-	$10\mu V$	$25\mu V$	$10\mu V$
Input offset current	-	$0{,}3nA$	$1{,}5nA$	$0{,}3nA$
Input bias current	-	$1{,}2nA$	$1{,}83nA$	$1{,}2nA$
Open-loop voltage gain	-	$11{,}92.10^6$	5.10^6	12.10^6
AC performance				
–3 dB Small Signal Bandwidth	$A_U = +1$ $A_U = +10$	$611kHz$ $59{,}6kHz$	$1{,}23MHz$ $63kHz$	$600kHz$ $60kHz$
Dominant pole frequency	open-loop	$0{,}05Hz$	$0{,}127Hz$	$0{,}05Hz$
Second pole frequency	open-loop	$10MHz$	$10MHz$	$10MHz$
Noise performance				
Input voltage noise	$f = 1kHz$ $R_G = 0$	$10nV/\sqrt{Hz}$	$11{,}1nV/\sqrt{Hz}$	$10nV/\sqrt{Hz}$
Corner freq. for 1/f noise	$R_G = 0$	$1{,}3Hz$	$1Hz$	$1{,}3Hz$
Input characteristics				
Differential-mode input resistance	-	$45M\Omega$	$40M\Omega$	$45M\Omega$
Input capacitance	-	$4pF$	$4pF$	$4pF$
Common-mode input resistance	-	$200G\Omega$	$100G\Omega$	$200G\Omega$
CMRR	$U_{cm} = \pm 13V$	$140dB$	$130dB$	$140dB$
Pole frequency for CMRR	$U_{cm} = \pm 13V$	$25Hz$	$63Hz$	$25Hz$
Output characteristics				
Output voltage swing	-	$\pm 12{,}5V$	$\pm 14{,}23V$	$\pm 12{,}5V$
Short circuit current	$R_L = 0\Omega$	$25{,}11mA$	$16mA$	$25mA$

Output resistance	open-loop	60Ω	60Ω	60Ω

4. CONCLUSIONS

In this paper behavioral macromodel of VFA for the PSpice simulator based on the datasheet electrical characteristics has been presented. The macromodel is independent from the actual technical realizations and are based upon compromises regarding the presentation of exact op amp structures in the model. The proposed model allows simulating arbitrary user circuits with respect to the behavior in both frequency and time domains, including effects such as accurate input/output impedance, dc transfer function, ac small-signal characteristic, transient response under a wide range of conditions, CMRR versus frequency, noise and voltage/current limitation. The model are not capable of simulating PSRR, temperature effects, board parasitics, differences between package styles, distortion (harmonic, intermodulation), etc. One of aims of the further work is to explore the possibility of adopting this compact macromodel in behavioral languages such as VHDL-AMS.

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