# DESIGN OF HARMONIC SIGNAL GENERATOR FOR CAPACITIVE PRESSURE SENSOR MEASUREMENT

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*The harmonic signal generator utilizing sigma-delta modulation for capacitive pressure sensor measurement was designed in AMIS CMOS 0.7 μm technology. Harmonic signal generator is a one of important parts of complex measurement system for capacitive pressure sensor measurement. Whole capacitive measurement system is based on bandpass (BP) Σ-Δ modulation. Phasing of harmonic signal and digital sampling signal is main requirement for proper function of capacitive pressure sensor measurement utilizing BP Σ-Δ modulator. Harmonic signal generator was designed using VHDL. Synthesis of digital synchronization utilizing harmonic signal generator was accomplished in Cadence BuildGates and implemented in Cadence Silicon Ensemble.*

**Keywords:** sigma-delta modulation, sensors, analog-digital integrated circuits

## 1. INTRODUCTION

BP Σ-Δ modulators [1], [2], [3] are well suited for direct conversion of the digitally modulated signals (QAM, PSK) from the frequency to the digital output. Once the RF signal is digitized, most of the signal processing tasks like channel filtering, demodulation etc. can be easily done in the digital domain with high degree of programmability. Inducted noise and high sampling frequencies requires corresponding electronic technology as it is use in the implementation for GPS/GSM communication systems.

The binary flux from the BP Σ-Δ modulator output is downconverted by digital multiplier and in the LP digital filter transformed in the digital number. Whole structure represents bandpass sigma-delta analog to digital converter (BP Σ-Δ ADC). Coherency between input signal $f_c$ and sampling frequency ($f_s = 4f_c$) in the BP Σ-Δ ADC makes converter phase sensitive. Because of this fact two LP digital filters controlled by the $f_s$ shifted for $\pi/2$ represents a converter of the input vector into its digital representation.

The simple BP Σ-Δ modulator of the first generation was designed for integrated sensor system using CMOS 0.7 μm technology. The defined narrow band is advantage against offsets of modulator sub circuits such as OPA, delay stage and summator. The modulator is tuned at 62.5 kHz sampling frequency. It processes the signal with central harmonic frequency $f_c$ = 15 625 Hz. The Fig. 1 shows the capacitive pressure sensor where one branch is sensing branch and another is reference branch.

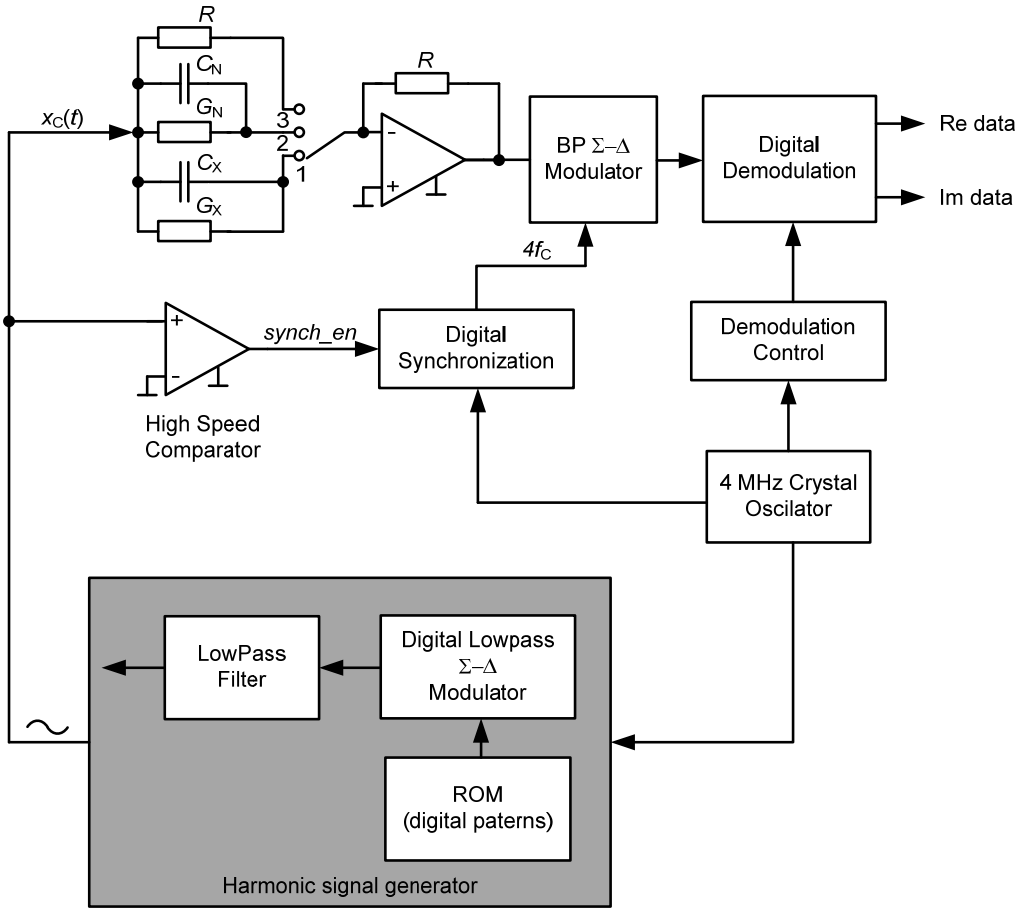



Fig.1. Capacitive pressure sensor measurement with BP Σ-Δ modulator

While the pressure influences the capacity $\Delta C_X$ the humidity impacts the conductivity $\Delta G_X$ of the sensing branch. Pre-processing circuit with BP Σ-Δ modulator converts it after synchronized down-conversion into its real and imaginary part. The binary flows are converted into digital number in two digital low pass (D-LP) filters. The digital resolution is proportional to the time window of the D-LP filter. The BP Σ-Δ modulator is controlled coherently with the input source frequency. The digital output values are determined by the quantized vectors in all three switch positions as follows

$$\begin{aligned} U_1 &= RU\left[j\omega\left(C_N + \Delta C_X\right) + G_N + \Delta G_X\right] \\ U_2 &= RU\left[j\omega C_N + G_N\right] \\ U_3 &= U \end{aligned} \quad . \qquad (1)$$

The phase shift of the processing block is suppressed by the subtracting operation. The difference of the digital values from the output of the LP filter in the position 1 and 2 normalized to the value measured in the position 3 is expressed by the formula. Here measured changes of capacity and resistance are obtained

$$\frac{U_1 - U_2}{U_3} = R\left(j\omega\Delta C_X + \Delta G_X\right) . \quad (2)$$

The BP Σ-Δ modulator is tuned on 62.5 kHz of sampling frequency as mentioned, it means that central frequency is

$$f_c = \frac{f_s}{4} = \frac{62500}{4} = 15625\,Hz . \quad (2)$$

## 2. DIGITAL SYNCHRONIZATION DESIGN

Phasing of harmonic signal with frequency $f_c$ and digital sampling signal with frequency $4f_c$ is main requirement for proper function of capacitive pressure sensor measurement utilizing BP Σ-Δ modulator. Digital synchronization for capacitive pressure sensor measurement is shown on Fig. 1. Digital synchronization utilizes harmonic signal generator which is based on digital lowpass Σ-Δ modulation. The output of harmonic signal generator is connected to high-speed comparator to generate *synch_en* signal to starting digital synchronization of harmonic signal and digital sampling signal.

### 2.1 Design of harmonic signal generator

The digital design has been used for simplicity of chip realization. The sine wave signal is generated by means of digital sigma-delta modulation. The output from sigma-delta modulator is connected to analog low pass filter. The output sine wave signal is obtained after high frequency filtering. The main clock frequency of digital part is 4 MHz. This frequency is common for all digital stages. Harmonic signal generator consists four blocks as can be seen in Fig. 2.

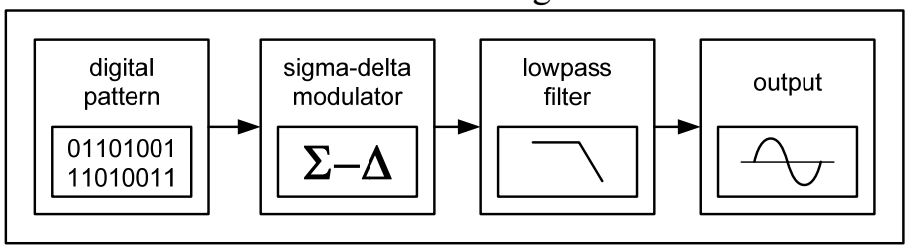



Fig.2. Block diagram of harmonic signal generator

The core of whole generator consists of Σ-Δ modulator. The first order Σ-Δ modulator is used for simplicity of design. The digital lowpass Σ-Δ modulator (Fig. 3) includes summator and substractor. The input and output signals are connected on it. The difference (sum) is connected to the register Σ. The value in this register is increased at each clock pulse. The register output is compared in comparator zero reference value. In case when register value is higher than zero, the comparator reverse into logic high, in other cases is zero. The comparator output is modulated sine wave signal. It could be filtered and analog signal could be obtained. The output is directly connected to the analog low-pass filter.

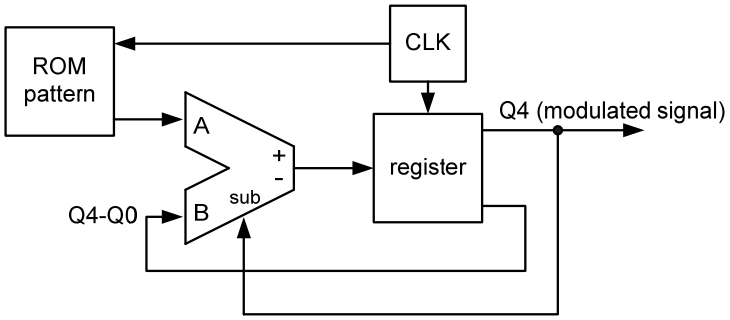



Fig.3. Block schema of digital lowpass Σ-Δ modulator

The digital lowpass Σ-Δ modulator is programmed in VHDL. The comparator has been replaced by MSB of register Σ for simplicity, because the decision level of comparator has been set at binary number 64, which is zero reference value. Thanks to this modification, the design is sign-less.

The last stage is low-pass filter. It is only analog part of the whole proposal. This filter has been designed separately. It has been chosen 4th order lowpass active Butterworth filter with cut-off frequency of 15 625 Hz. The filter makes analog signal from modulated signal.

## 3. Simulation Results

Digital bitstream of digital lowpass Σ-Δ modulator is shown in Fig. 4. Phasing of harmonic signal (sine wave) and digital sampling signal (clk_4x) is shown in Fig. 7. Signal clk_4x has frequency $f_s = 4f_c$ as is presented in Fig. 5. Clk_4x signal and sine wave signal are depending only on main clock signal frequency. The variation of main clock frequency has not impact on proper function of harmonic signal generator. Sampling requirement $f_s = 4f_c$ is satisfied.

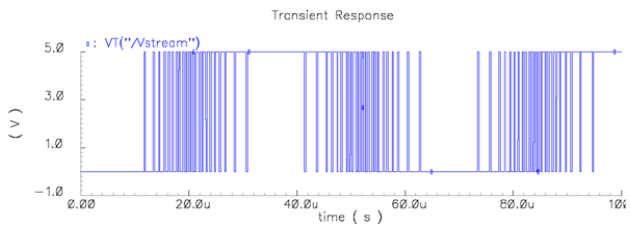



Fig. 4. Digital bitstream of digital lowpass Σ-Δ modulator

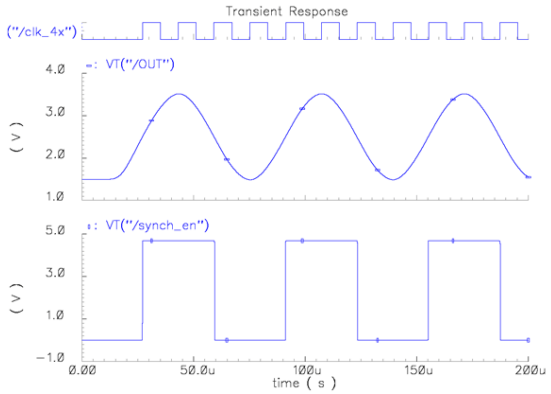



Fig. 5. Phasing of harmonic signal (sine wave) and digital sampling signal (clk_4x)

Detail view of high-speed comparator response on sine wave is shown in Fig. 6. Overall delay error $\tau_{err}$ of clk_4x is depending on high-speed comparator response and main clock signal. High-speed comparator is tuned on 0 s delay for typical

technology process case due to inserted voltage bias control. Overall delay error $\tau_{err}$ is primarily addicted on main clock frequency. For main clock frequency clk = 4 MHz is maximum overall delay error $\tau_{err} \approx 250$ ns.

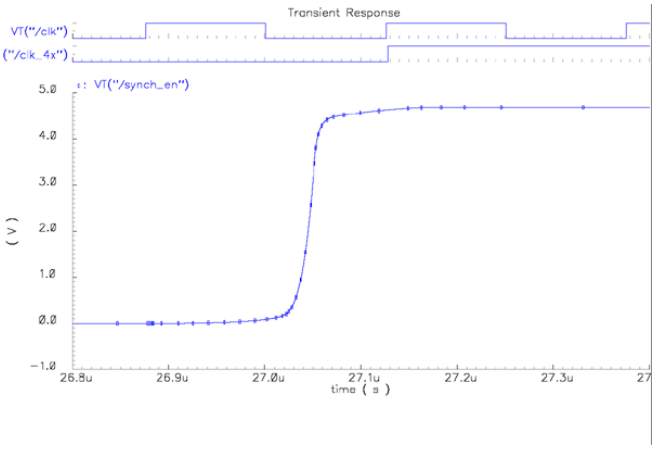



Fig. 6. Detail view of high-speed comparator response on sinus wave

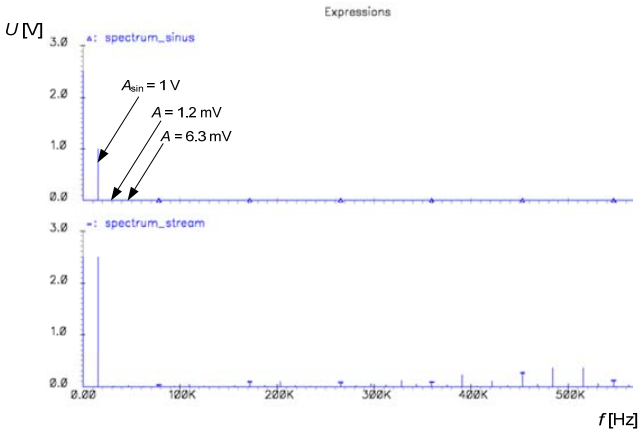
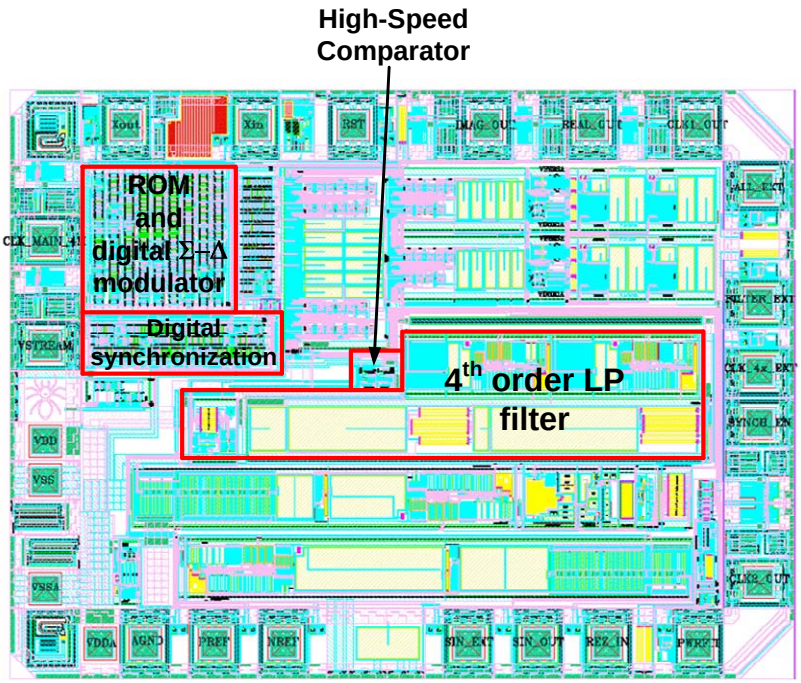



Fig. 7. Spectrum of sine wave and digital bitstream signal

Spectrum of sine wave and digital bitstream signal is shown in Fig. 7. Digital bitstream is filtered by 4$^{th}$ order lowpass active Butterworth filter to get sine wave signal with amplitude $A_{sin}$ = 1 V on frequency $f_c$ = 15.625 kHz. Total harmonic distortion of output sinewave is approximately 0,8 %.

## 4. CONCLUSION




The ASIC for capacitive pressure sensor measurement was designed and manufactured in AMIS CMOS 0.7 µm technology under the EUROPRACTICE project and its parameters are now under testing. The harmonic signal generator and digital synchronization block are most important parts of capacitive pressure sensor measurement. These parts with additional digital logic are described by VHDL language and synthesized in Cadence BuildGates. Maximum overall delay error $\tau_{err}$ is primarily addicted on main clock frequency. Overall delay error $\tau_{err}$ can be minimized by increasing of main clock frequency. In future work the ROM memory block in

harmonic signal generator could be replaced by synthesizable CORDIC algorithm to get high harmonic suppression. Utilizing high-order digital Σ-Δ modulator is another way to high harmonic suppression.

**ACKNOWLEDGEMENT**

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## 5. REFERENCES

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