OPTIMIZING THE NOISE PERFORMANCE OF AN INTEGRATED INTERFACE FOR CAPACITIVE SENSORS WITH A WIDE RANGE

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This paper presents the noise optimization of a time-based capacitive-sensors interface. It has been shown that increasing the frequency will increase the resolution. Therefore by analyzing charge-transfer speed, the maximum frequency for which the systematic errors are still within a certain limit have been calculated. Also it has been shown that, depending on the input-capacitance ranges, the use of either an OpAmp or an OTA as front-end amplifier can be advantageous. To decrease the noise of the comparator in the applied relaxation oscillator, a pre-amplifier with the minimum required bandwidth has been used. Moreover, to use the maximum dynamic range of the interface, this dynamic range can be set by the user for any value between 1 pF to 1 nF. The interface has been designed for implementation in 0.7μm standard CMOS technology. Simulation results show that for a 5 pF sensor capacitance with a parasitic capacitance of 50 pF and a measurement time of 60 μs, a resolution of 14.7 bits can be achieved.

Keywords: Capacitive sensor, interface, noise

1. INTRODUCTION

Capacitive-sensors elements can be applied in many applications as cascade sensors to measure a wide variety of signal such as, displacement, proximity, humidity, acceleration, liquid level, gas concentration and so on [1]. They can be integrated on a printed circuit board [2] or in a microchip [3] and offer non-contact sensing [2]. Inherently, capacitive sensors consume little power while their cross sensitivity to temperature is very low. In high precision application, such as displacement measurement in a closed loop system, in addition to a high resolution also a high measurement speed is needed. This can be achieved by a) decreasing the thermal noise by increasing the power, b) applying low-noise circuit technique and optimizing the noise behavior of the circuit, c) increasing the level of the drive signal, and d) using the all above mentioned technique. In earlier papers it has been shown that the interface circuits can be based on the use of relaxation oscillators, which offers the attractive features of simplicity and low-power consumption [4] to [7]. In this paper, we show how the noise performance of this interface circuit can be improved using optimized low-noise circuit technique. In the interface circuit three-signal auto-calibration is used. The input capacitance range can be set by the user for any value from 1pF to 1 nF. The interface has been designed for implementation in 0.7μm standard CMOS technology, and consumes less than 4 mW of power. Our simulation results show that with the proposed optimization, for a 5 pF sensor capacitance with a parasitic capacitance of 50 pF and for 60 μs measurement time a resolution of 14.7 bits can be achieved.

2. THE MAIN STRUCTURE OF THE INTERFACE

Figure 1(a), shows the main structure of the interface, including the components for three-signal auto-calibration.

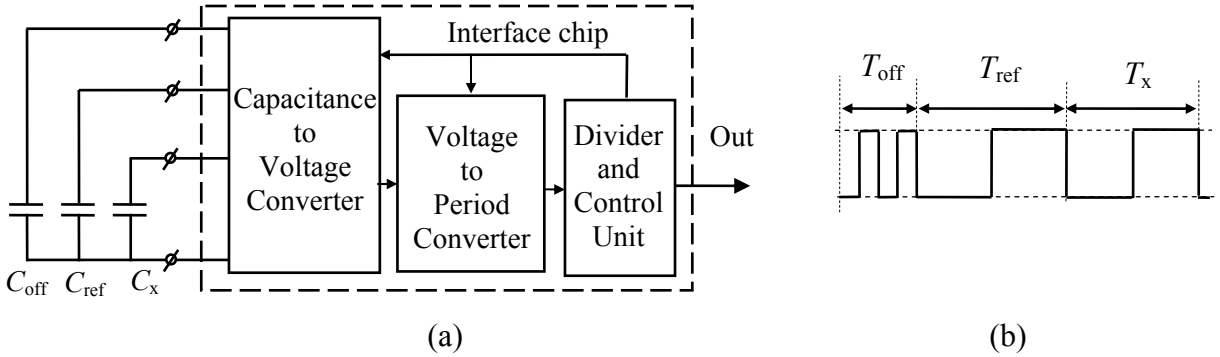

Figure 1: (a) The main structure of the interface and (b) the interface output signal

The interface output signal is shown in Fig. 1(b). According to the three-signal auto-calibration technique [5], a single measurement cycle consists of three phases: one for the measurement of the offset capacitor C_{off}, one for the reference capacitor C_{ref}, and a third one for the sensor capacitor C_x. The different time intervals T_{ref}, T_{off} and T_x, correspond to the output signals during the measuring of C_{off}, C_{ref} and C_x, respectively. The different periods of the output signal, can be read with a micro-controller. For identification purposes, the time interval T_{off} is split into two short periods [5]. Data can be read via a serial port (RS232) and can be analyzed, for instance, with a Labview program. Figure 2(a) shows the capacitance-to-voltage converter (CVC) [4],[5] which is "just" an amplifier for the excitation signal V_{drive}, but in this case we want to convert the capacitor value. Figure 2(b) shows some relevant signals. The drive voltage has levels of 0 V and V_{dd}. In phase 1, S_1 is closed and the drive voltage is sampled on C_x. In phase 2, the charge C_xV_{dd} is pumped into C_f which results in a jump $V_o = C_xV_{dd}/C_f$ of the CVC output voltage $V_{o,CVC}$.

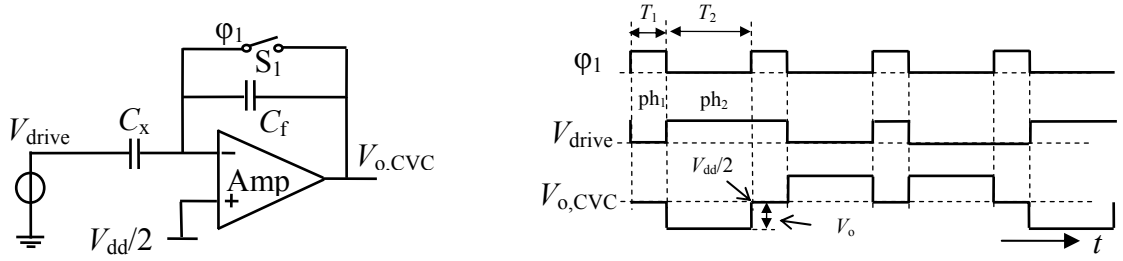

Figure 2: (a) The CVC and (b) some relevant signal

Figure 3(a) shows the voltage-to-period converter (VPC) [4],[5]. Also some related signals are shown in Fig. 3(b). The voltages V_1 and V_2 are block shaped with the levels of 0 V and V_{dd}. In phase 1, the charge of $Q_1 = V_{dd}C_{o1}$ of C_{o1} is pumped into integrator capacitor. Next, this charge is removed by the integration of I_{int}. In phase 2, the charge of

$Q_2 = V_{dd}C_{o2}+V_oC_S$ is pumped into integrator capacitor, where V_o represents the jump of the CVC output voltage $V_{o,CVC}$ as discussed before (Fig. 2(a)) This charge is also removed by the integration of I_{int}. Therefore, one complete measurement cycle, T_{msm}, amounts to:

$$T_{msm} = \frac{4\left(V_{dd}\left(C_{o1}+C_{o2}\right)+V_oC_S\right)}{I_{int}} \quad (1)$$

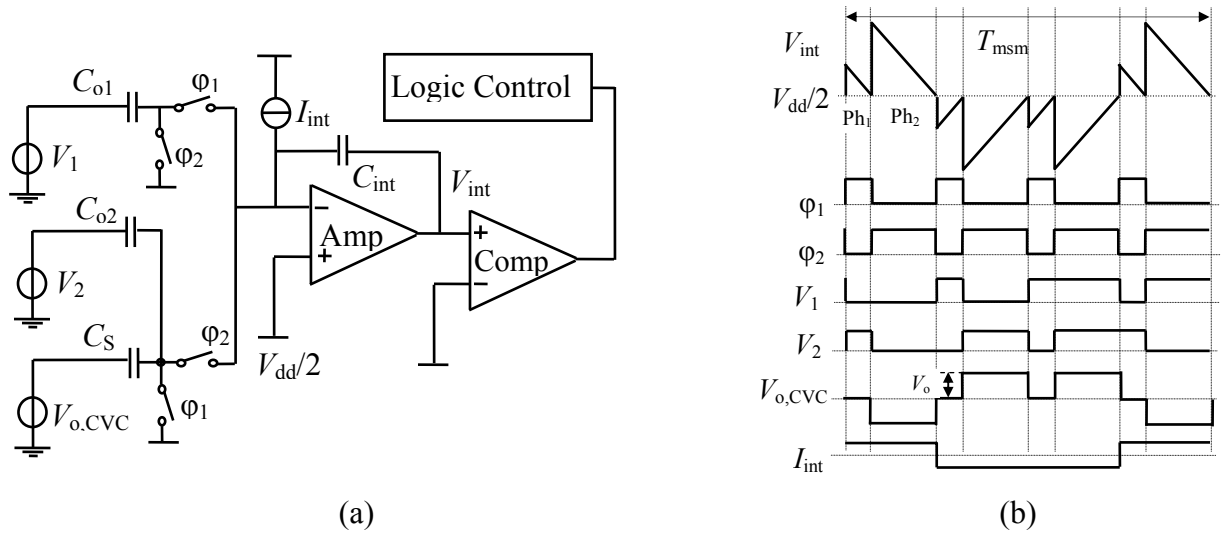

Figure 3: (a) The voltage to period converter and (b) some related signals.

3. OPTIMIZATION OF THE FREQUENCY TO MAXIMIZE THE RESOLUTION

Low-frequency disturbing signals, such as offset, temperature drift, parameter drift by aging etc., will be removed by the applied three-signal auto-calibration technique. In addition, interference coupled through the sensor connection cable and flicker noise can be removed with a special kind of chopper, according to the (+ - - +) principle described in [4], [5]. Increasing the interface frequency, results in a better suppression of out-of-band low-frequency disturbing signals, which increases the resolution. Moreover, it can be shown for thermal noise that increasing the frequency with a certain factor, for instance by increasing $I_{int,}$ with the same measurement time the signal-to-noise ratio will increase with the square root of that factor. Therefore increasing the frequency will increase the resolution. The maximum frequency will be limited by the required time to transfer the sampled charge in the CVC and the integrator with certain accuracy. When the same type of amplifier is used for both the CVC and the integrator, due to sensor and/or cable parasitic capacitances, the CVC will limit the maximum frequency.

Figure 4 shows the relevant part of the CVC, which is used to calculate the charge-transfer time constant. In this figure C_l is the sampling capacitor of the VPC, C_x and C_p represents the sensor and cable parasitic capacitance. When for the CVC amplifier an OTA is used, the charge transfer time constant $\tau_{CT(OTA)}$, will be:

$$\tau_{CT(OTA)} = \frac{C_f C_{in} + C_f C_l + C_{in} C_l}{g_m C_f} \quad , \tag{2}$$

where $C_{in} = C_p + C_x$ and g_m is the transconductance of the OTA.

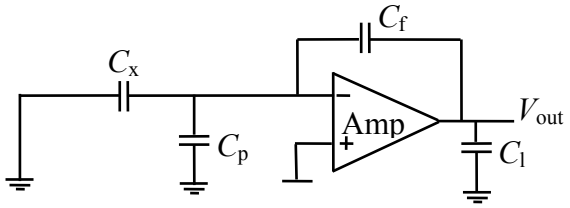

Figure 4: The relevant part of CVC to calculate the charge transfer time constant.

The value of feedback capacitor C_f is selected in such a way that for the maximum input capacitance $C_{x,max}$, the output voltage V_{out}, reaches its maximum value which is equal to the maximum output-voltage swing of the amplifier. When a rail-to-rail amplifier is used, the feedback capacitor C_f should be twice as $C_{x,max}$. Moreover, in most practical case $C_p >> C_{x,max}$. Therefore equation 2 can be approximated as:

$$\tau_{CT(OTA)} \approx \frac{C_{in}\left(C_f + C_l\right)}{g_m C_f} \tag{3}$$

As an alternative, an OpAmp can be used implemented with an OTA and a buffer stage as shown in the model of figure 5, which results in a CVC charge-transfer time constant $\tau_{CT(OpAmp)}$:

$$\tau_{CT(op\text{-}amp)} = \frac{\left(C_f + C_{in}\right)C_C}{g_m C_f} \approx \frac{C_{in} C_C}{g_m C_f} \tag{4}$$

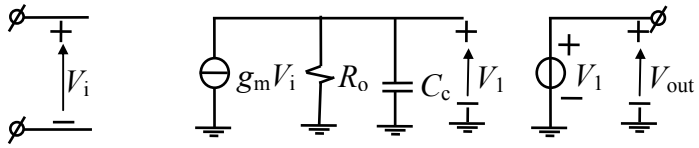

Figure 5: OpAmp structure, an OTA followed with a voltage follower.

Where, C_c represents the compensation capacitor. In our design, for any range of input capacitance we have:

$$\tau_{CT(op\text{-}amp)} \leq \tau_{CT(OTA)}. \tag{5}$$

For C_x<10 pF, the difference between the two charge-transfer time constants is small and because it's lower power consumption the use of an OTA is preferable. However for C_x>10 pF, the use of the OpAmp allows to apply higher frequencies..

The available time for charge transfer T_2 (Fig. 2(b)) should be large enough compared to charge transfer time constant, to achieve the required accuracy. To optimize the interface performance, for different ranges of C_x and C_p, we will include the option of changing in integrator current I_{int} (Fig. 3(a)). In this way, an optimal frequency of the excitation signal can be selected by two frequency-selection pins, FS0 and FS1.

4. COMPARATOR DESIGN TO MINIMIZE THE NOISE

In general, because of fast switching requirements, comparators have a wide-band input amplifier. Therefore, their input referred noise could be very high, which in our interface circuit could dominate the noise of the interface [6],[7]. Since any delay-related error of the comparator can be compensated by three-signal auto-calibration, we do not need a fast comparator. Therefore, our comparator includes a preamplifier with the minimum required bandwidth, followed by a regenerative comparator (Schmitt trigger). This preamplifier not only decreases the effect of comparator noise by increasing the slope of signal at the comparator input, but, it also filters the noise of the CVC and integrator amplifiers. Provision will be taken that, when the interface frequency is changed, the bandwidth of the pre-amplifier is changed too.

5. CAPACITANCE RANGES

The range of the input capacitance can be changed by changing the value of the feedback capacitor C_f (Fig. 2). The next stage (the voltage-to-period converter) could be optimized independent of the input capacitance range. However, as explained in section 3, optimization of the CVC amplifier for a wide range of input capacitance, for instance 1 pF to 1 nF, is almost impossible. Therefore, for optimal performance, the whole range is divided into three different C_x ranges: C_x< 1 pF, C_x< 10 pF and C_x < 1nF. In case of C_x< 1 pF, C_f is implemented internally. For the other two ranges the user has to connect an external capacitor C_f which value is optimized for his specific range. In this way the user can get the optimal noise performance of the interface.

6. SIMULATION RESULTS

The interface has been designed for implementation in 0.7μm standard CMOS technology. The simulation results show that the power consumption is less than 4 mW. Figure 6 shows the relevant part of the interface for noise analysis. In this design for a 5 pF sensor capacitor with parasitic capacitance of 50 pF, the total noise at the output of Amp3 in phase 1 and phase 2 (Fig.2) is 1.4 mV and 2.5 mV, respectively. These values are much larger than the input-referred noise of comparator. In this simulation, we supposed that the chopper can remove the low-frequency noise up to $f_{chopper}/2$. Moreover T_1=1.25 μs and T_{2max}=5 μs (Fig.2). Therefore, without divider (Fig. 1) the measurement time including three-signal auto-calibration amounts to 60 μs. For an output-voltage slope of Amp3 of 15 V/ μs, it can be calculated that the resolution amounts to 14.7 bit.

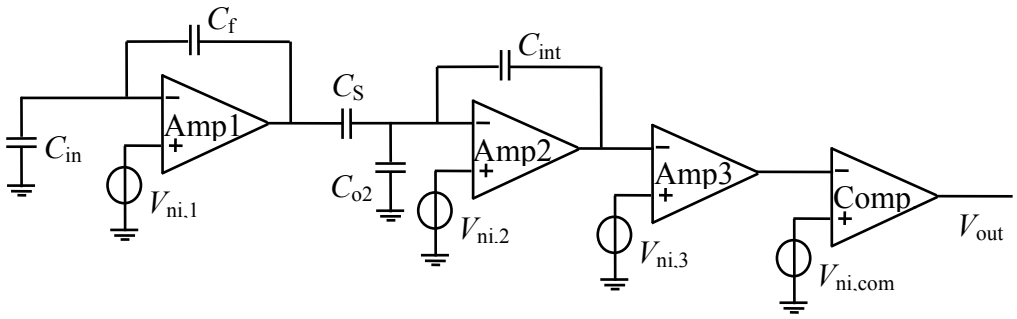

Figure 6: Related part of the interface for noise analysis.

7. CONCLUSION

The noise performance of an integrated interface for capacitive sensor has been optimized. It has been shown that increasing frequency will increase the resolution. The maximum frequency which can be applied without causing significant errors has been calculated. For the front-end amplifier an OTA or an OpAmp can be used. It has been shown that for input capacitances up to 10 pF, the use of an OTA is preferable. However, for larger capacitors, the use of an OpAmp is advantageous. We showed that adding a pre-amplifier with the minimum required bandwidth can decrease the effect of the noise of the comparator. The interface has been designed for implementation in 0.7μm standard CMOS technology. Simulation results show that, for a 5 pF sensor capacitance with a 50 pF parasitic and 60 μs measurement time and with 4 mW power consumption, a resolution of 14.7 bits can be achieved.

8. REFERENCES

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