INVESTIGATION OF DIGITAL PHASE DETECTORS

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This article deals to describe the simulation and the experimental investigation of the basic types of digital phase detectors and especially acquiring their phase-voltage response. This phase-voltage response represents the output voltage of the phase detector as a function of the phase difference between the digital input sequences. It is examined an exemplary implementation of specialized tester, intended for experimental analysis of phase detectors. It is described the significance for choosing the next block in the phase-locked loop system (the low-pass filter-integrator). It is also done an analysis and comparison of the results, obtained from both the simulation and experimental environment.

Keywords: Digital phase detector, Simulation, Phase-voltage responses

1. INTRODUCTION

Digital phase detector is a basic block in electronic systems using Phase-Locked Loops (PLL). It represents a device which compares two frequencies and forms an output signal proportional to their phase difference. There exist many types of phase detectors [1, 4]. They have different characteristics and there does not a universal one. When choosing a phase detector for practical application, it should be considered a number of factors such as the nature of the input signals, the linearity of the phase-voltage response, the range of the phase and frequency difference in which phase-voltage response is linear etc. There are two basic types of phase detectors: phase detectors for compared signals with identical form (called 'type 1') and phase detectors working on logical edge of the signals (called 'type 2'). In this article the phase detectors are shown with exemplary implementation of a low-pass filter which passes the signal component proportional to the phase difference.

2. SIMULATION INVESTIGATION OF DIGITAL PHASE DETECTORS

The method for simulation analysis [2, 3] is applied in the environment of the program product OrCAD PSpice and aims to present the phase-voltage response of the examined phase detector. It is used transient analysis by setting two input pulse sequences with a constant difference between their frequencies. This leads to a linear increase of the phase difference. The proportionality coefficient between the phase difference and the time (called 'phase step') depends on the frequency difference of the input sequences and it can be changed according to the desired representation accuracy.

2.1. Phase detector for regular input signals of type 1

The scheme of this phase detector is shown on Fig. 1. It is build by logical gate XOR. The output signal is a voltage proportional to the phase difference between the compared digital signals. A passive low-pass filter (R1, C1) is applied.

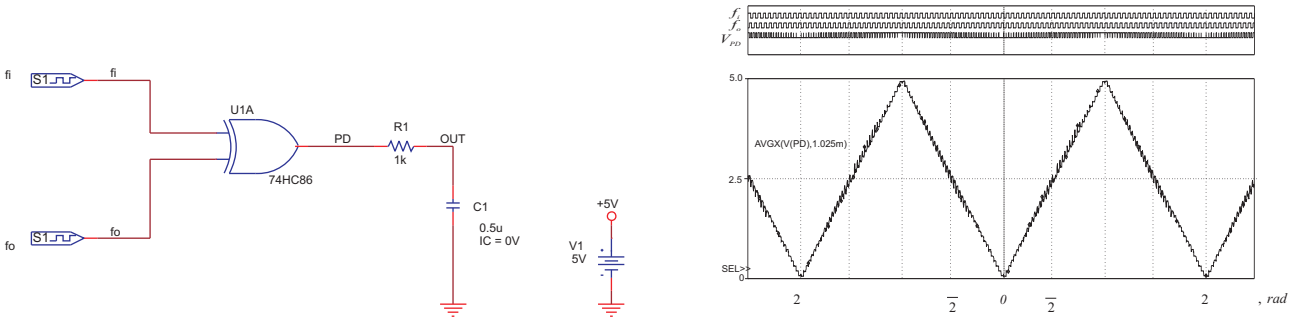

Fig. 1. Phase detector for regular input signals of type 1.

Simulation parameters are:

– 1.000 ms time period of signal f_o, with 0.5 ms time of impulse;

– 1.025 ms time period of signal f_i , with 0.5125 ms time of impulse;

– initial condition on capacitor C1 is set to 0V;

– end time of the analysis is set to 82ms, start time of the analysis is set to 0 s and the maximum time step is set to 100 µs.

2.2. Phase detector for regular input signals of type 2

This phase detector (Fig. 2) works on the rising edges of the compared signals f_i and f_o. After the input of f_i it is laid the forming group U2A÷U2C, U3A which produces short negative impulses by the rising edge of f_i. Thus the rising edge of f_i sets the flip-flop in '1', and the rising edge of f_o resets the flip-flop. The applied low-pass filter is the same as the preceding one.

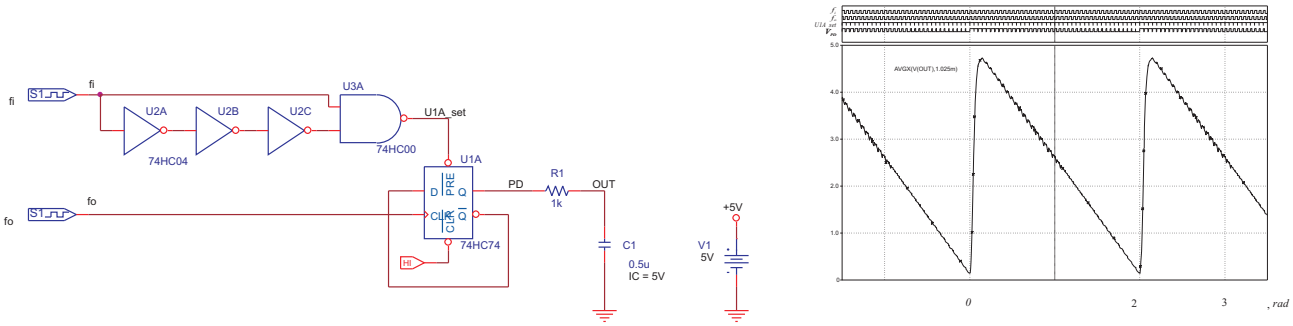

Fig. 2. Phase detector for regular input signals, type 2.

The simulation parameters are the same with the exception of:

– initial condition on C1 is set to 5V;

– initial condition of all flip-flops is set to '1'.

2.3. Digital frequency sensitive phase detector for regular input signals, working on one front of the compared signals

The scheme is shown on Fig. 3. The compared signals f_i и f_o, by their rising edges, set to '1' two separate D-flip-flops, U1A and U1B. A logical gate NAND (U2A) produces in its output '0', when both the flip-flops turn into '1', and it simultaneously resets them. The output of the first flip-flop (node Q1) will stay in logical state '1' during the time f_i outdistances f_o, and the output of the second flip-flop (node Q2) will stay in '1' during the time f_i falls behind towards f_o. The digital outputs operate the

so-called 'charge pump' (transistors T1 and T2) which causes division of the pump-up and pump-out circuit of the low-pass filter.

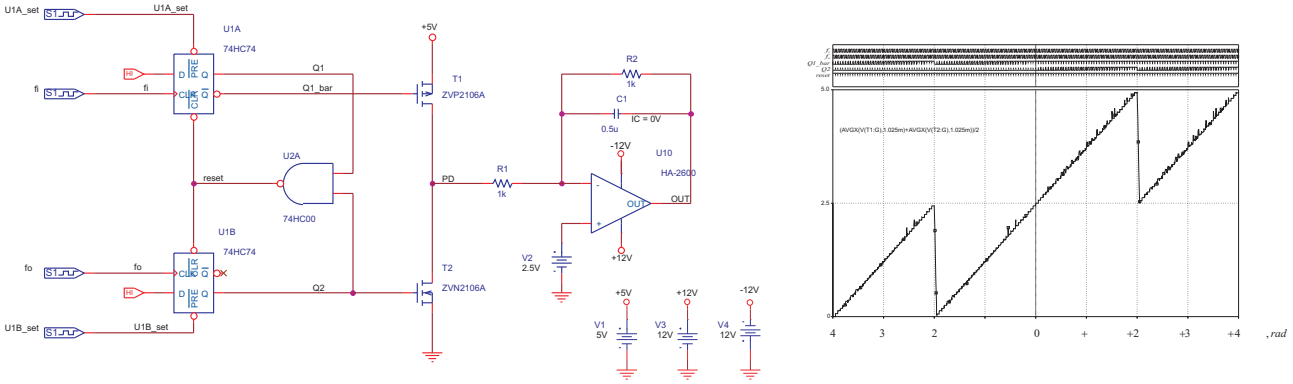

Fig. 3. Digital frequency sensitive phase detector, working on one front of the compared signals.

Simulation parameters are the same as these in the first phase detector, with an exception of:

– initial condition of all flip-flops is set to '0';

– level of the stimuli U1A_set and U1B_set is set to '1'

2.4. Digital frequency sensitive phase detector, working on both fronts of the compared signals

This detector (Fig. 4) represents a version of the preceding phase-frequency detector and it works consecutively on the rising and falling edges of the compared sequences. On the way of the compared signals controlled invertors (XOR) are laid and they switch over the active working fronts of the flip-flops.

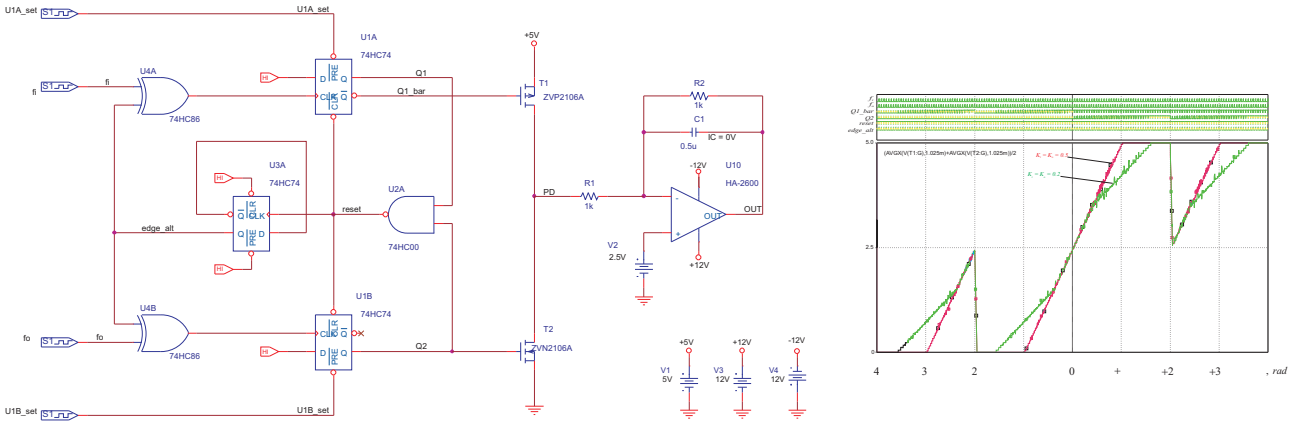

Fig. 4. Digital frequency sensitive phase detector, working on both fronts of the compared signals.

Simulation parameters are the same as these in the preceding phase detector but the initial condition of all flip-flops is set to '1'. Two analyses are performed – for duty cycles 0.5 and 0.2 respectively.

2.5. Phase detector for casual input signals, type 1

This phase detector (Fig. 5) produces an output signal only while logical '1' occurs on the input. If the input signal f_i is '0', the phase detector does not produce correction signals and the output of the filter stays in its former state.

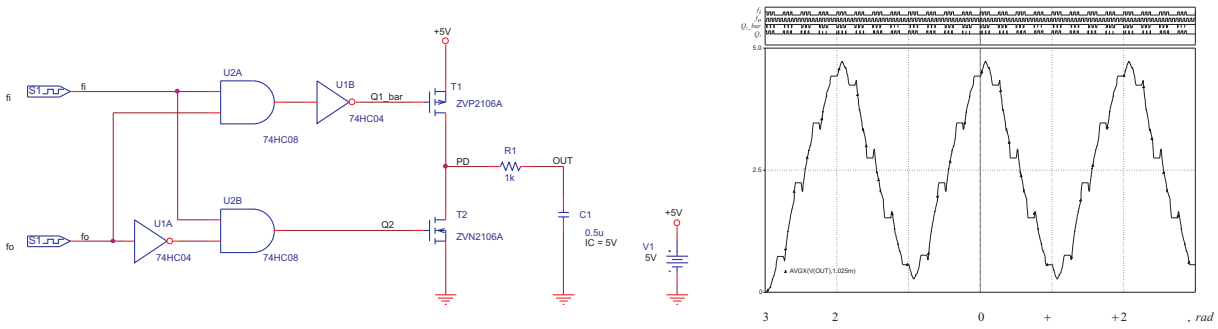

Fig. 5. Digital phase detector for casual input signals of type 1.

The simulation analysis is performed with a casual input signal f_i, and simulation parameters are the same as these in the phase detector from item 2.2.

2.6. Phase detector with an expanded linear range of work

Its scheme is shown on Fig. 6. It is implemented on the basis of insensitive to coincidence reversible counter, consisted of two separate counters (U1 and U2) and a subtractor U3 (ALU in subtraction mode). The digital code at the counter's output (one's complement code) is transformed into an analogue value by digital-to-analog converter working in one's complement code as well.

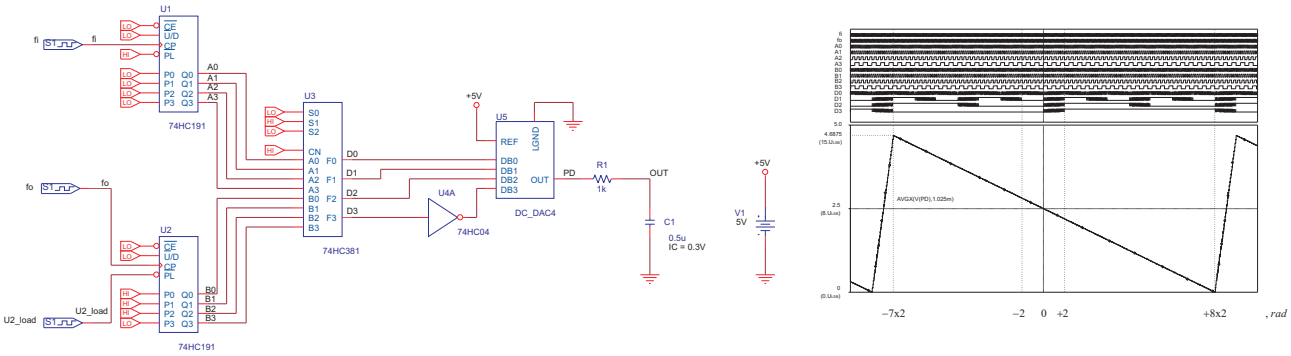

Fig. 6. Digital phase detector with an expanded linear range of work.

Simulation parameters are the same except for:

– initial condition on C1 is set to 0.3 V;

– initial condition of all flip-flops is set to '0';

– level of the stimulus U2_load starts with '0' for a time of 1 μs, afterwards it is set to '1' (this leads to initial parallel load of counter U2, which allows representation of the whole phase-voltage response by one simulation run).

3. EXPERIMENTAL INVESTIGATION OF DIGITAL PHASE DETECTORS

For the purposes of the experimental investigation of the phase detectors it is constructed a specialized tester whose block diagram and scheme are shown on Fig. 7. The tester enables acquiring phase-voltage responses of various phase detectors in a static mode (32 points in the range from -2π to +2π rad).

The generator produces digital pulses with frequency f_{osc}, which is 16 times higher than the frequency of the input signals f_i and f_o. The dephaser produces shifted (dephased) digital impulse sequences. It is implemented by 8-bit Johnson's counter (U4A, U5). The signal f_o is taken from its most-sighting output.

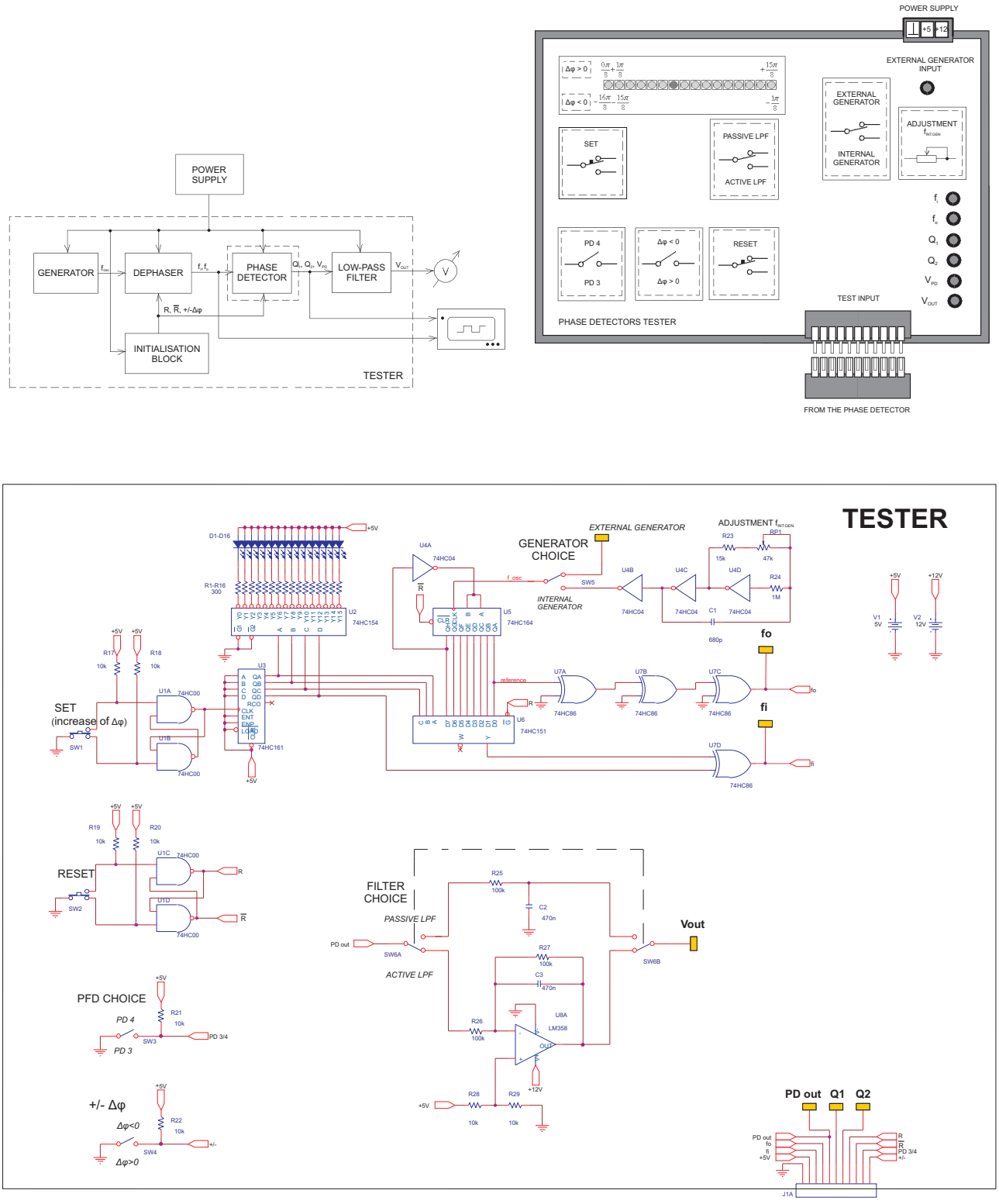

Fig. 7. Tester for experimental investigation of phase detectors.

The dephased signals come in the input of the multiplexer U6. It chooses which one of them will be 'passed' as f_i to the output, according to the set phase difference. This ensures a dephasing between f_o and f_i in the range from 0 to π rad. Dephasing in the range from π to 2π is obtained by additional inverting of the multiplexer's output frequency f_i. Setting of phase differences in the range from 0 to -2π is done by suitable initialization of the phase detectors witch is set by the initialization block.

The control of the dephaser is implemented by 4-bit counter U3, thus the set phase difference increases with π/8 in toward its previous value, after each pushing of the button 'Set'. For indication of the set Δφ is used a 4-bit binary decoder U2, driving the light emitting diode row (D1÷D16).

Each of the analyzed phase detectors is a separate device module which is plugged into the tester through a coupling.

4. CONCLUSIONS

In this article a simulation and experimental investigation of digital phase detectors is examined. The main point is analysis of their phase-voltage response. The analyzed detectors are accompanied by the next block of the PLL system (low-pass filter-integrator). Its type (passive or active) is of great importance and it is determined by the number of the detector's digital outputs, as well as by the capability for producing correction signal during f_i failure. When the digital output is just one (phase detectors 2.1, 2.2 and 2.6), the filter type does not matter. In the presence of two digital outputs the choice of filter type is determined by the capability of working with casual input signals. Frequency-sensitive phase detectors 2.3 and 2.4 do not have this ability, thus the acquiring of their correct phase-voltage response requires an active filter. In contrast, the phase detector 2.5 does not produce correction signals during f_i failure. In order to preserve the previous output state, the filter should be passive, without a parallel connected resistor to the capacitor C1.

In the simulation analysis, using a filter aggravates the linearity of the phase-voltage response. In order this to be avoided and simultaneously a good smoothness of the graph to be achieved, a mathematical averaging function AVGX is used. It is applied to the digital outputs of the phase detectors. It ensures a filtration by mathematical way and this allows eliminating of the filter. Again, the phase detector for casual input signals is an exception, because of the aforesaid reasons.

Analyzing and comparing the obtained results, it can be concluded that the acquired phase-voltage responses in both the investigations coincide each other, as well as the theoretical ones [1, 4].

The developed simulation and experimental setting for examination of phase detectors is designed for the purposes of the scientific investigations and for the educational process in the Department of Electronics, Technical University of Sofia.

5. REFERENCES

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