TEST GENERATOR FOR EXAMINATION OF PLL AND DDS SYSTEMS

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This paper describes a test generator for examination of digital and analog phase locked loop and digital synthesizers. In practice very often are used signals with various types of shapes and frequencies. For high precision signals mostly are used PLL and DDS generators. The device described in this paper is based on a digital synthesizer and a phase locked loop. With this test generator could be examined different types of phase detectors and low-pass filters which are the essence of every PLL. An algorithm is proposed for assessment of phase locked loops.

Keywords: (Generator, Phase Locked Loop, Direct Digital Synthesis)

1. INTRODUCTION

Analog Phase Locked Loops (PLL) are well studied and used very often in practice. It is almost impossible to generate high precision signals without phase locked loop. There are PLL based generators in many devices especially in communication appliances. A major difficulty in developing a new PLL is stability and initial adjustment of the system although there is a full and systematic theory in this field [1], [2], [3], [4].

This paper focuses on finding development method that assures an optimal solution for generators based on a PLL. A device and evaluation algorithm is proposed, which help to gather information about the behavior of PLL components. In most publications the authors emphasize on mathematical simulation and analysis. This paper shows how to investigate physical scheme solutions of phase detectors and low pass filters (the core of every phase locked loop). Investigation of phase to voltage response and dynamic response of these blocks in PLL aids for quick and easy development of reliable devices. Additionally the proposed device could be used to investigate some types of mathematical functions for synchronization of pulse sequences in delay locked loops, Frequency Locked Loops (FLL) and all Digital Phase Locked Loops (DPLL). Another way to generate mixed signals is Direct Digital Synthesis (DDS). A DDS loop is used as a reference clock to create pulse sequences which have high stability and easily adjustable parameters.

2. BLOCK DIAGRAM

Fig. 1 shows a block diagram of the proposed device. The reference clock generator is created with a direct digital synthesizer. Building this kind of generator is shown in [5]. The DDS which is used in this device can generate triangle, sinusoidal and pulse signals. The digital synthesizer output is connected to a filter-amplifier or a buffer for the digital sequences. The output signals of the DDS have very good

characteristics (high stability, wide bandwidth, high resolution, and fast response of the output parameters). The only drawback of the DDS approach is that maximum signal frequency can not exceed one half of the DDS working frequency.

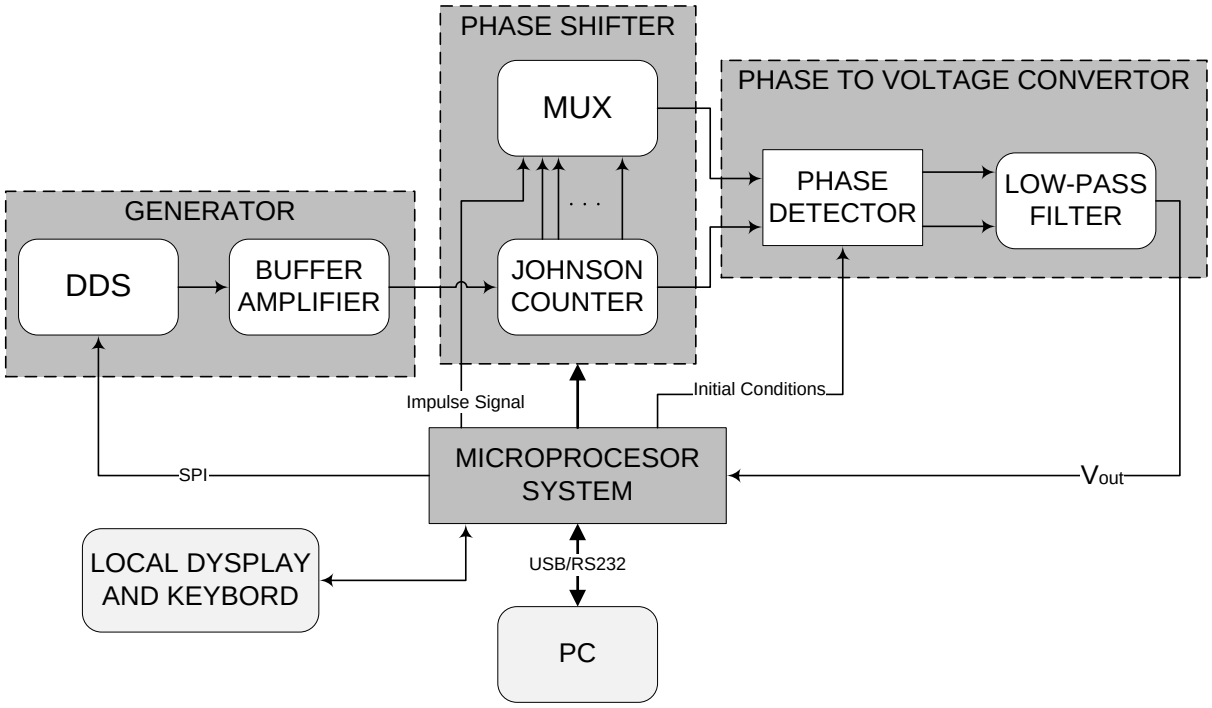

Fig. 1. Block diagram.

The generator pulse signals are transferred to a phase shifter. It consists of a Johnson counter and two multiplexers. The phase steps are determined by the order of the counter. The maximal phase shift from the last output of the counter is π, *rad*. If the Johnson counter contains *n* flip-flops the phase shift of the *k* output will be $k\frac{\pi}{n}$. Any phase shift can be selected by a multiplexer and can be transferred to the phase detector. The main disadvantage of this phase sifter type is the decrease of the input frequency $f_0 = \frac{f_i}{n}$, where f_0 is the frequency of the pulse sequence on the output, f_i is the input signal frequency from DDS generator. In order to achieve higher frequency it is necessary to decrease the order *n* of the Johnson counter. In contrast, the number of the phase shifter steps is higher when the order of the counter is higher. These two contradicting requirements can be satisfied when a second multiplexer is used in the Johnson's counter feedback. Thus *n* can be made optimal for each different case.

The main building block of every PLL is the phase to voltage converter. It consists of two blocks that define the speed, noise resistance and stability. To examine the phase detector behavior and the low-pass filter in the proposed scheme an external module is used. This way different configurations and schemes could be assessed [6], [7].

The device is controlled by a microprocessor system that sets the operating modes, measures the output signal, processes and visualizes the results. The parameters of each block in the scheme can be controlled separately which makes the complete system very flexible. The system is controlled by a PC but additional keyboard and display are implemented.

3. CONTROL ALGORITHM

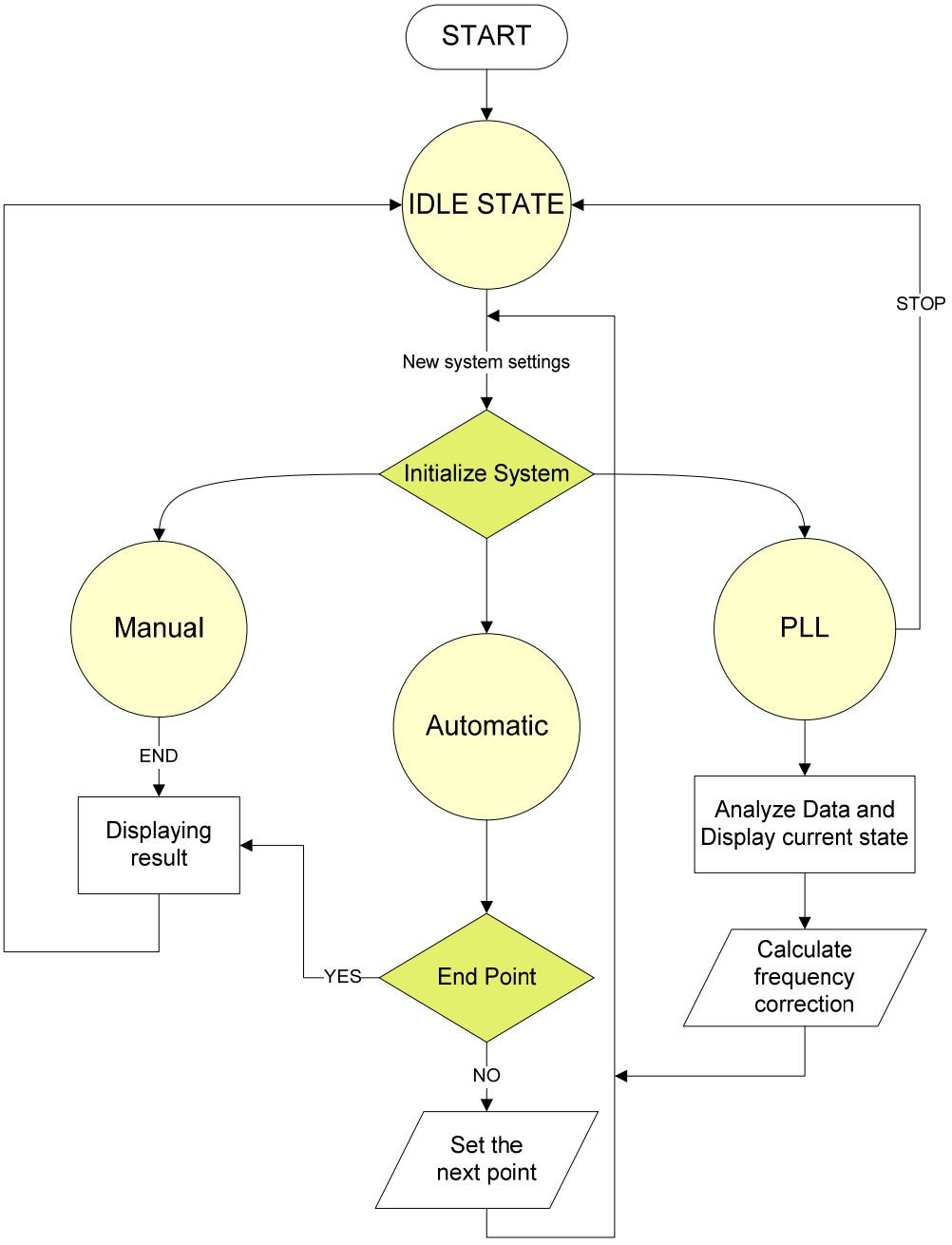

Fig. 2. Control algorithm.

The control algorithm is shown on Fig. 2. On Power-on the device is in IDLE state and is ready to be set in a selected operating mode. To examine the behavior of a device one of the most important steps is to set the initial operating conditions.

Improper setting of the initial conditions may lead to incorrect results or unpredictable behavior.

The control algorithm can work in three possible operating modes.

3.1. Manual operating mode

In this mode signal with fixed frequency, amplitude and shape is set from the generator. The generated signal (analog or digital) can be used and measured directly or can be fed to the phase shifter input. In this mode a fixed phase difference and initial operating conditions of the phase detector are set. On the display the voltage corresponding to the set phase difference is visualized.

The manual operating mode is set when the device is used as a generator of pulse signals with fixed parameters.

3.2. Automatic operating mode

In this mode the dynamic system behavior can be examined. All states that are to be examined are set through the PC and after starting the system are executed in sequence. This gives the possibility to measure different parameters. As an example it is taken the phase to voltage converter response measurement. First a fixed generator frequency and certain initial operating conditions of the phase detector are set then the phase is dynamically changed by the phase shifter. The changing of the phase is done in time intervals that are long enough for all transients to be finished. The microprocessor system measures the voltage on the output of the low-pass filter and sends the data to the PC for each phase step.

The transient's examination when the phase is changing is done in a similar way as in the example given above. In this case the frequency is fixed and the output voltage is measured for a single change of the phase difference.

These two characteristics are of great importance in a PLL design because the system's stability and reaction depend on them.

3.3. PLL mode

In this mode the microprocessor system generates signal with predefined frequency that is compared to the one output by the DDS generator. The two pulse sequences are compared in the phase to voltage converter and the difference is fed back to the microprocessor. The main advantage of this mode is the possibility to examine different digital control algorithms in DPLL and FLL development and the synchronization of digital sequences. The frequency correction computed by the microprocessor and the measured voltage on the low-pass filter's output are sent to the PC for each step. This allows the mathematical approach and the algorithm to be assessed.

4. CONCLUSIONS

There are many kinds of generators which can provide different types of signals. Unfortunately none of them provides automatic examination of the transient and phase to voltage response of phase detectors and phase locked loops. The described device is very useful in generating signals with shape, frequency and phase shift of

any kind. It can be tuned precisely and all parameters of the signals can be controlled. The main advantage of this scheme is the possibility to create two phase shifted pulse sequences and rapidly change the phase difference between them. Also the test generator can control the initial operation conditions of examined scheme. This makes the devices extremely flexible and useful for almost any kind of phase-, delay- or frequency-locked loops. The major problem in developing PLL systems is stability. The proposed device helps to examine the scheme in many different operation modes.

Using this device in the education process can be very helpful for students in order to improve their knowledge and understanding in the filed of phase locked loops, direct digital synthesis and pulse signals generation.

5. ACKNOWLEDGMENT

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