THE INFLUENCE OF FABRICATION STEPS ON SELECTED PROPERTIES OF POWER DMOS TRANSISTOR

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The high-voltage power DMOS transistors are widely used for various power electronic applications as motor controls and power switching supplies. Research and optimization of their characteristics is one of the challenges of power MOS transistor design. The Technology CAD (TCAD) tools support process and device simulation and help to predict the technology parameters for achieving required structure parameters. In presented paper the influence of fabrication steps and structure parameters on the selected properties of power DMOS transistor are analyzed by 2-D numerical modeling and simulation.

Keywords: Power DMOS transistor, TCAD, fabrication steps, breakdown voltage, on-resistance, numerical simulations

1. INTRODUCTION

The high-voltage power DMOS transistors are widely used for various power electronic applications, e.g., motor controls and power switching supplies that require low on-resistance R_{ON} and high breakdown voltage V_{BR} [1]-[3].

The simulation process of semiconductor structures prior to manufacturing is important step for understanding of the device behavior and for obtaining the optimal electrical characteristics [4], [5].

The breakdown in power MOS transistors is a phenomena which some effects can be simulated, analyzed and studied. It appears in two forms: punch-through and reach-through mechanisms. Punch-through breakdown occurs in the channel of power MOS transistor. It is observed when the depletion region on the source side of the body-drift p-n junction reaches the drain region at drain voltages below the rated avalanche voltage of the device. This provides a current path between source and drain and causes a soft breakdown characteristic. Careful selection and optimization of the doping profile used in the simulation process of the power MOS transistor is therefore very important. The surface concentration of the body diffusion and the channel length will determine whether punch-trough will occur or not. There are trade-offs to be made between on-resistance R_{ON} which requires shorter channel lengths and punch-through avoidance which requires longer channel lengths.

Also, higher channel implant dose is beneficial from the punch-through point of view since depletion width will be smaller, but R_{ON} will suffer through reduced carrier mobility. The design of the doping profile involves choosing channel and

source implant doses, diffusion times and temperatures that give the desired characteristics. Optimizing them in simulation process is one of the challenges of power MOS transistor design.

The reach-through phenomenon, on the other hand, occurs when the depletion region on the drift side of the body-drift p-n junction reaches the epitaxial layer-substrate interface before avalanching takes place in the epitaxial layer. This will cause a further increase in drain voltage which will cause the electric field to reach a critical value where avalanching begins. Once the depletion edge enters the high carrier concentration substrate, a further increase in drain voltage will cause the electric field to quickly reach the critical value where avalanching begins.

In this work the influence of fabrication process variation on selected properties of DMOS transistor is explored and analyzed. The variations in design process and layers parameters are considered to affect on the breakdown and on-resistance. The results of 2-D numerical simulations with Synopsis TCAD environment are presented.

2. Used Simulation Methodology

The methodology for performing the simulations of the submicron silicon power semiconductor DMOS structure comprises of TCAD tools, which precisely simulate advanced semiconductor processes and devices down to the nm level, and traditionally used for exploring and optimizing process technologies and device characteristics throughout the technology development cycle; using the systematic sequential process in some iterations, which includes structure design, simulation, measurement, visualization; different methods for physical verification, mask synthesis, lithography verification, implantation and impurity diffusion. The Genesis framework is used for the management of simulation flow, visualization of simulation results, analysis of simulation data and generation of statistical information, providing insight into process characteristics and device performance which may not be attainable through measurements. Synopsys' unique TCAD solution includes DIOS for process simulation including etching and deposition, ion implantation, and diffusion and oxidation with identical models in one dimension and two dimensions and DESSIS for device modeling [6], [7].

The design flow is presented in Figure 1. The modeling and simulation sequences of the 2-D structure and doping profile of one half cell of the N-channel vertical double diffused MOSFET is performed through the process simulator DIOS.

Then the DIOS output files (structure and corresponding doping profile) are used as an input for the advanced 2-D mixed mode device and circuit simulator DESSIS or as an input for MDRAW, where one can manually set the contacts area and can perform the mesh refinement [8], [9]. DMOS transistor is represented in the simulator DESSIS as a virtual device whose physical properties are discretized onto a nonuniform mesh of nodes. Continuous properties such as doping profiles are represented on a sparse mesh and are only defined at a finite number of discrete points in space. The doping at any point between nodes can be obtained by

interpolation. Therefore, the quality of the mesh in different structure regions is very important for the results after DESSIS simulation. The drift-diffusion, thermodynamic, and hydrodynamic models are implemented in DESSIS. The thermodynamic nonisothermal model is used to calculate additional effects, such as an increase of the avalanche breakdown voltage due to temperature growth. This model assumes that the electron and holes are in thermal equilibrium with the lattice temperature. A fully coupled (Newton) method for the selfconsistent solution of the Poisson and electron continuity equations is specified. The Extrapolate is specified in the Math section, and therefore the initial guess for each bias step is calculated by extrapolation from the previous two solutions. For successful simulation results to the steps (min, max, initial) have to be assigned appropriate values.

Tecplot-ISE is used to visualize the output from the simulation in 2D, and INSPECT is used to plot the electrical characteristics.

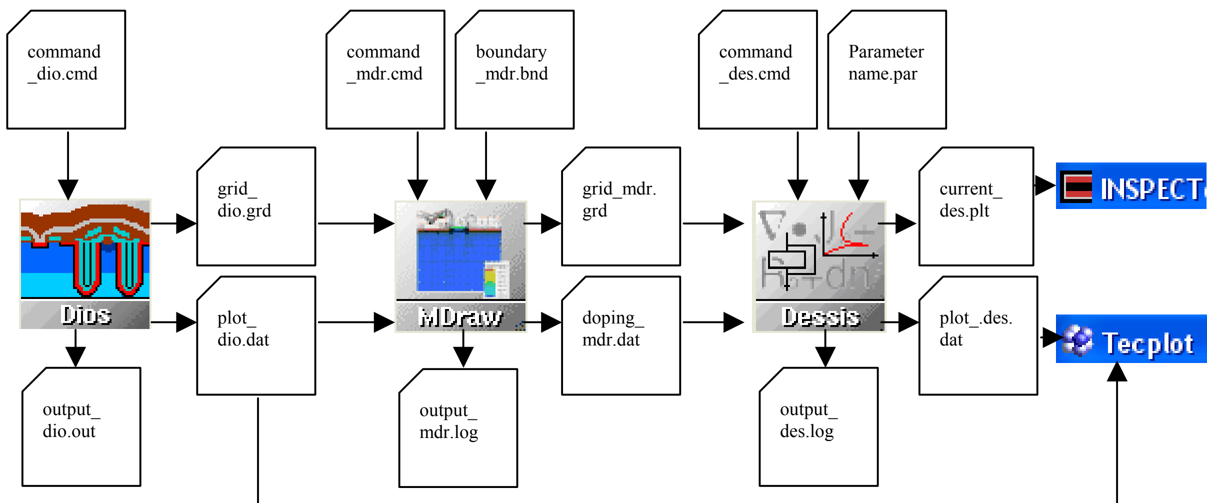


Fig. 1. Design flow

3. Experimental Results and Discussion

In this work some fabrication steps are performed with following aim: the examinations of breakdown occurrence process in the power DMOS transistor with focus on exploration of the parameters of epitaxial layer: thickness and resistance, and implantation dose of P-well region. They are important in the finding of the optimal design solution according to interrelation breakdown voltage/on-resistance. The research is provided in different steps as changing the resistance of the epitaxial layer, changing the implantation dose of P-well layer, adding new values for thickness of epitaxial layer at implantation dose=1,6E13 particles/cm^2 and at dose=6E13 particles/cm^2, adding new diffusion operation.

At the experiment with changing the resistance of the epitaxial layer, the DMOS structure is simulated at different values of the resistance of epitaxial layer: ρ_{epi} = 0,21; 0,23; 0,25; 0,27; 0,29; 0,31 Ωμm at implantation dose of P-well = 3,6E13 particles/cm^2 and thickness of epitaxial layer 2,65 μm. The obtained electrical characteristics show that breakdown voltage increases with increasing the ρ_{epi} as it is shown in Figure 2.

The distribution of total current density in the DMOS structure at different ρ_{epi} is shown in Figure 3. The increasing values of ρ_{epi} are from left to right. The breakdown is the avalanche reach-through type. The DMOS structure is free from the punch-through/drain-induced barrier lowering effect caused by short channel.

The main reasons for the lack of a short-channel effect in DMOS device are the very lightly doped drain and the p-well doping profile with the higher boron doping level wrapped around the n-source. The lightly doped drain and the higher doping profile of the p-well channel at the source edge make the depletion regions in the channel region very small.

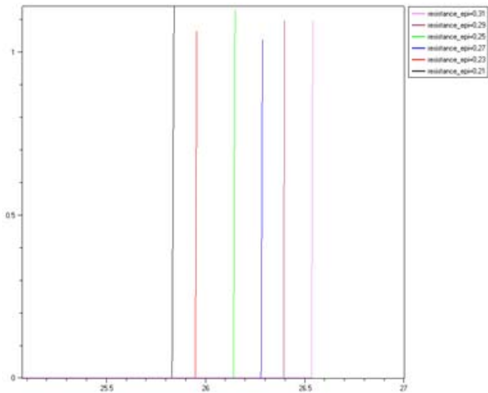


Fig.2 Breakdown Voltage at different ρ_{epi}

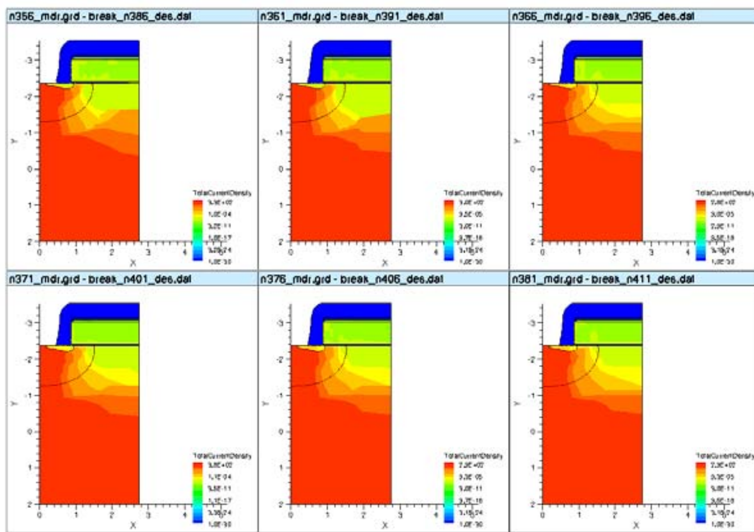


Fig. 3 Total current density in the DMOS structure at different ρ_{epi}

In the second experiment the influence of the implantation dose of P-well layer on on-resistance and breakdown voltage is explored.

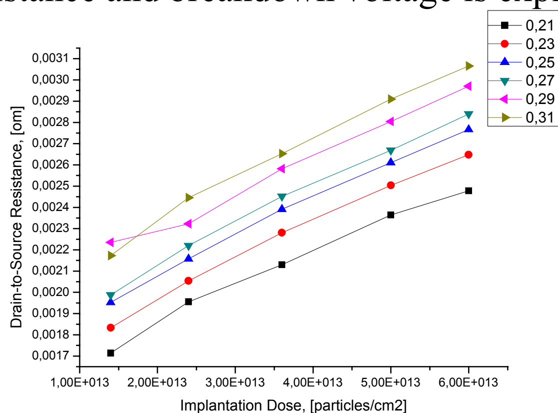


Fig.4 Drain-to-Source Resistance versus Implantation Dose

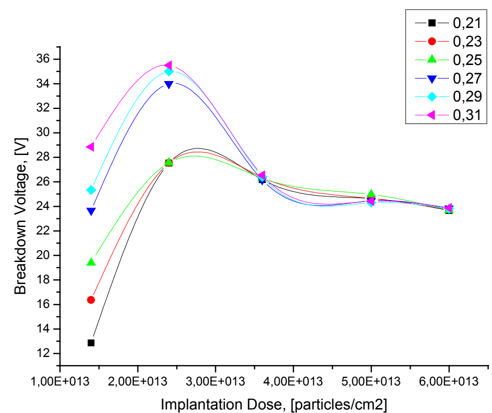


Fig.5 Breakdown Voltage versus Implantation Dose

At each of the above used epitaxial resistances the four other values of P-well implantation dose are added: 1,40E+13; 2,40E+13; 5,00E+13 and 6,00E+13.
The drain-to-source resistance is proportional of the implantation dose as shown in Figure 4. The dependence of breakdown voltage from implantation dose is shown in Figure 5 and the optimal achieved value for V_{BR} is around 35 V at ρ_{epi} = 0,29 and 0,31 Ωμm.

In the third step according to the results of the previews results:

- V_{BRmax} = 35 V at ρ_{epi} = 0,29 Ωμm
- The maximum value of breakdown voltage at P-well implantation dose = 2,4E13 particles/cm^2 and at ρ_{epi} = 0,29 Ωμm,

the four new values of the P-well implantation dose = 1,6E13; 1,8E13; 2,0E13; 2,2E13 particles/cm^2 are added, in order to be explored the influence of these implantation dose values on the breakdown voltage.

The maximum value of breakdown voltage around 30V is reached at P-well implantation dose = 1,6E13 particles/cm2, but the observed breakdown is in the channel of the DMOS structure, which is not typical for this kind of structure (Figure 6).

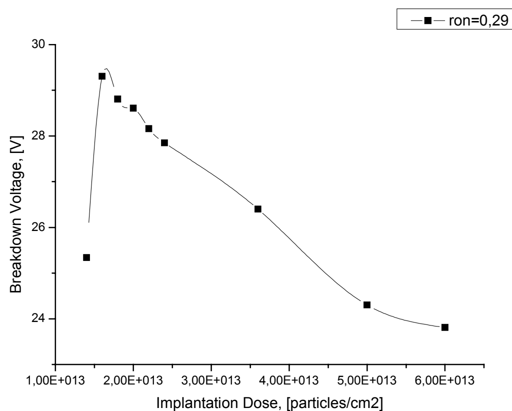


Fig. 6 Breakdown Voltage versus Implantation Dose

According to these results the next step is focused on exploration how thickness of epitaxial layer at P-well implantation dose=1,6E13 particles/cm2 influences on the breakdown voltage. The maximal value of the breakdown voltage=35 V is obtained at the value of epitaxial thickness =3,05 μm.

After the previews step with this experiment it is tried to prepare shorter channel through importing of one new diffusion operation at epitaxial layer thickness=3.05 μm. The DMOS structure is simulated in three different times: 10min, 15min and 20min. The new diffusion operation does not increase the breakdown voltage as it is shown in Figure 7.

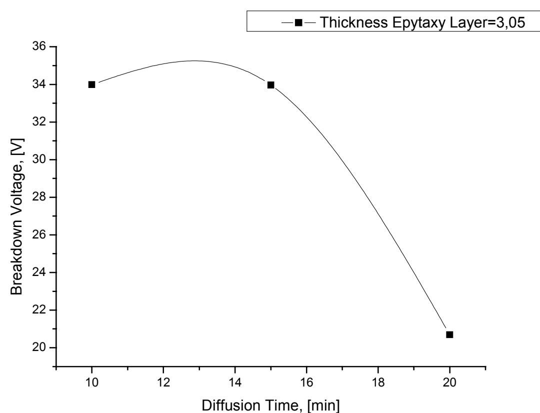
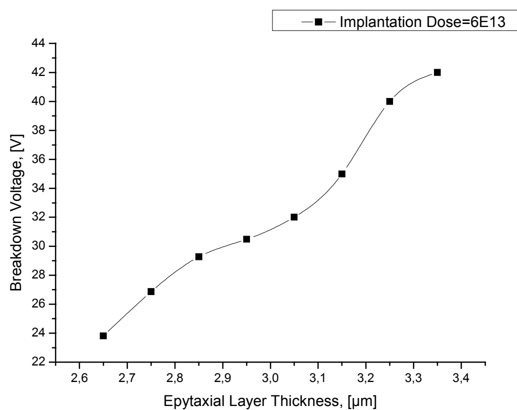


Fig. 7 Breakdown Voltage versus Diffusion Time



In the next step some new values for thickness of epitaxial layer at P-well implantation dose=6E13 particles/cm2 are added with goal to perform the exploration of the influence of increasing Epitaxial Layer Thickness = 3,15; 3,25; 3,35; 3,45; 3,55μm on Breakdown Voltage. The results show that the value of breakdown voltage increases with increasing the thickness of epitaxial layer.

Fig. 8 Breakdown Voltage versus Epitaxial Layer Thickness

4. CONCLUSION

The presented work analyze the influence of fabrication steps on breakdown occurrence in the vertical power DMOS transistor and on-resistance is examined according to some structure's parameters as resistance of epitaxial layer, thickness of epitaxial layer and P-well implantation dose. After numerical simulations with TCAD tools the results show that the optimal value of the breakdown voltage depends of good designed combination of epitaxial layer and P-well region properties. The higher breakdown voltage is obtained through increasing the resistance of epitaxial layer, increasing the epitaxial layer thickness and precisely chosen value of P-well implantation dose. The type of breakdown in DMOS structure at the highest achieved values of breakdown voltage and at low P-well implantation dose is punch-trough that corresponds to the changed location and mechanism of diode breakdown to bipolar transistor breakdown.

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