

## BEHAVIOR MODELING OF DC/DC BUCK CONVERTER

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*In this paper the implementation of analog extensions of Hardware Description Languages for behavior modeling and simulations of DC/DC converters is described. The design sequence from high level model to block level is examined. The system like description and top-down methodology are considered for behavior verification. The DC/DC converter was considered as entire system, so mathematical equations can be used to model the behavior of its functionality. This will represent the high level behavior model of the circuit. This model gives the ability to analyze functionality of the system on high level assuming different control techniques and characteristics. Particularly the buck converter was examined as it is widely used and with known structure. Hardware description language model reduces simulation time and initial design efforts.*

**Keywords:** hardware description language, VHDL-AMS, dc-dc converter, behavior modeling, system design

### 1. INTRODUCTION

The contemporary design flow pays more respect due to the fast time to market and first-time design success. The very important characteristic that makes achieving this possible is the ability to make fast design scratch on block level, model the design parameters and provide fast simulation to test its functionality and operability. Very successful way to do this is to use high level hardware description languages to model and simulate the design. Nowadays the analog and mixed signals designers have the chance to be able to use the advantages which not long ago only the digital designers have – hardware description languages. Analog and mixed signals HDLs such as VHDL-AMS and Verilog-Analog/ Verilog-AMS provide the ability to model pure analog systems and mixed signals systems on high level of abstraction, using basic electrical principles – electrical nodes and branches dependences. They can model systems on different abstraction levels – from elements to systems, using differential and algebraic equations. Being IEEE standards they provide ease of design flow and software tools interoperability.

In this work the way of modeling DC-DC converters with VHDL-AMS is represented. This is the mixed signals extension of VHDL. The tool used is the Ansoft's Simplorer SV simulator with built in VHDL-AMS simulator. The HDL here is used to create sub-sheets as user defined models and then to bind them in circuit using graphical interface. One can use HDL models along with standard cells from Simplorer database. Also rich VHDL-AMS database is provided.

Using analog and mixed signals HDLs gives the designers wide range of ways to describe the system properties. The system can be described by defining its transfer function using mathematical equations or by splitting it into sub modules and

describe each module separately. In this paper the DC-DC converter modeling is represented by using both principals – the control part is described behaviorally on high abstraction level and the electrical parts – resistor, capacitor and inductor are given separately. At the end the principles of creating VHDL-AMS description of capacitor, inductor and resistor at a high abstraction level is given and the results of using it in simulations.

## 2. DC-DC BUCK CONVERTER

With development of new technologies in the field of microelectronics is increasing the use of integrated circuits (IC) with large and very large scale of integration (LSI and VLSI), because the schematics became much more sophisticated. Operated voltages of the integrated circuits go down, parasitic capacitance are increased. Today design of fully monolithic, high efficiency, buck dc-dc converter is very important task. Integration of the whole system components will be decrease essentially the price of battery operated electronic devices. They are many problems connected to the integration of the standard buck converter. One of them is low Q factor of monolithic passive components and especially of the inductors. The high switching frequency  $f_s$ , which is needed for reducing of the values and sizes of the filter's components, leads to high switching losses in the main switches. Thus overall efficiency of the buck converter's system is decreased.

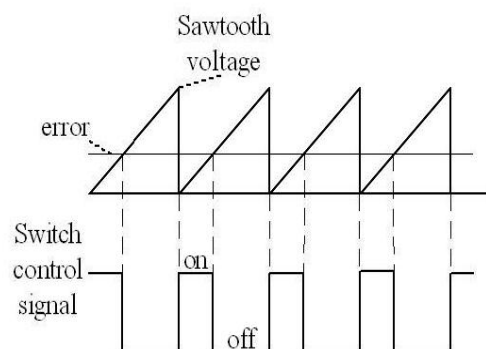


Fig. 1 PWM Control.

In Fig. 1 is shown PWM (Pulse-Width Modulation) method used for control of the output voltage. The switch control signal, which regulate the states “on” and “off” of the main switch  $S1$  is generated by comparing the voltage with repetitive waveform and error control voltage.

In order to be improved one of the most important parameter in the dc-dc converters – efficiency, different control's techniques is good to be investigated and analyzed. In this paper is simulated whole system of the buck converter. The diode in the basic circuit is replaced by the switch.

Simulations of the whole system of the buck converter and investigations of different control techniques over the behavior of the circuit take a long time. Using VHDL some of the analysis can be performed very fast, and this will save time.

## 3. BUILDING BEHAVIOR MODEL

The whole control part of the design is described in one VHDL-AMS entity. The inputs are: feedback from the output of the converter and saw-tooth generator. The outputs are two so each switch is controlled separately. The output signals are described as digital values with pure digital delays inserted as control system parameters. The delays may control switch “on” and switch “off” times. The switches are modeled like VHDL-AMS sub-sheets so “on” and “off” resistance is defined. Thus they can be considered non ideal switches. The equations for voltage and current are defined according to Ohm’s law.

The description code of the “regulator” entity is given below:

```

ENTITY    regulator IS
generic(   vref : real := 1.2;
            param : real := 0.5;
            ctr1_on_delay : time := 0.0 ns;
            ctr2_on_delay : time := 0.0 ns;
            ctr1_off_delay : time := 0.0 ns;
            ctr2_off_delay : time := 0.0 ns
            );
port (    terminal fb : electrical;
            quantity saw : real;
            signal ctr1 : out bit;
            signal ctr2 : out bit);
END ENTITY regulator;

```

Four global constants of type TIME are defined, as GENERIC elements to represent control signals delays – turn “on” and turn “off”. Also a generic called “param” is defined. It is used in mathematical equations to determine error value and the value to compare to the saw-tooth signal. The reference value also is defined as a generic element of type real. This allows using it freely in the mathematical equations to perform regulation. The feedback voltage is lead into the entity using TERMINAL of type ELECTRICAL (named “fb”).

The values of the reference voltage, feedback and the parameter are used to define the value which is compared to the saw tooth signal.

The saw-tooth signal is defined as a QUANTITY of type REAL. This is done in order to use the saw-tooth generator provided in the software tool libraries, which output is of type REAL.

The code to generate output signals is:

```

process(saw'above(temp))
begin
if (saw'above(temp) = true) then
    ctr1 <= '0' after ctr1_off_delay;
    ctr2 <= '1' after ctr2_on_delay;
else ctr1 <= '1' after ctr1_on_delay;
    ctr2 <= '0' after ctr2_off_delay;

```

**end if;**  
**end process;**

In order to control switches separately two control signals are used – one for each switch. They are defined as digital outputs of type BIT. The scheme is given on Fig. 2.

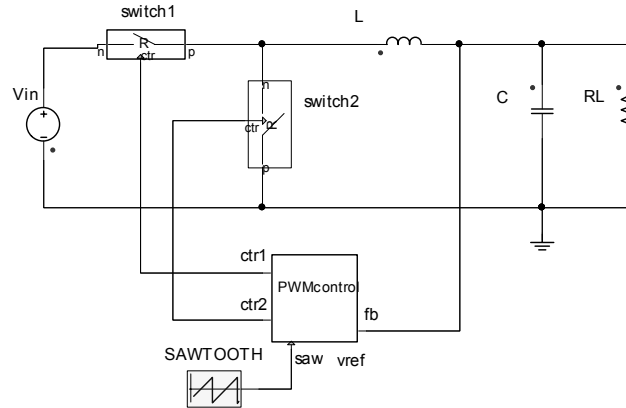


Fig. 2 Buck system.

Here `ctr1_off_delay`, `ctr2_on_delay`, `ctr1_on_delay` and `ctr2_off_delay` are the delays of the switches when they turn “on” and “off”. The “`ABOVE()`” attribute is used to determine when value of the saw-tooth signal is greater than value `temp`, which is evaluated from the feedback signal. This is embedded in sequential if-else statement, which is normal for digital VHDL. It is possible, because the returned value of the “`ABOVE`” attribute is Boolean and can be used as an equation for the “if” statement. Whole this is inserted into “Process” statement.

The higher level model can be build by merging elements in the behavior model sub-sheet. The version with behaviorally modeled R, L and C elements is given:

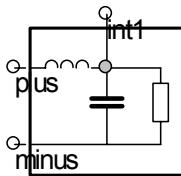


Fig. 3 Behavior model of passive elements.

This is described by the following VHDL-AMS code:

```

IF (domain = quiescent_domain) USE
  flx == L * IL0;
  il == IL0;
ELSE
  flx == L * il;
  vl == flx'.dot;
END USE;
IF (domain = quiescent_domain) USE
  temp_charge == C*VC0;
  vrc == VC0;

```

**ELSE**

```
temp_charge == C * vrc ;
ic == temp_charge'dot;
```

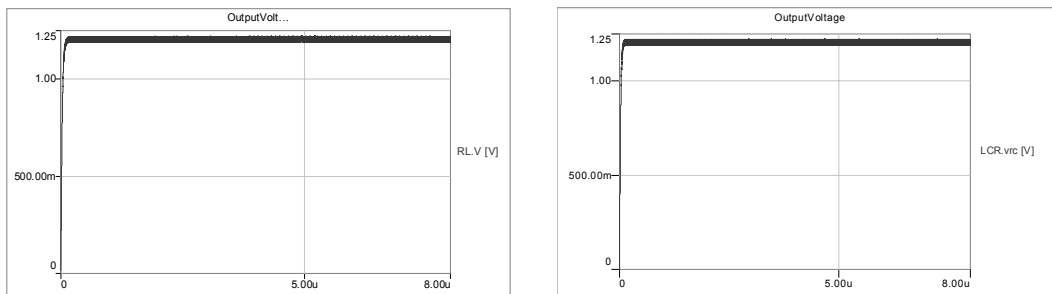
**END USE;**

```
ir == vrc/R;
```

**4. RESULTS**

The buck converter system is investigated and analyzed with software tool Simplorer. The input voltage is 3.3 V and the output voltage is set to be 1.2 V.

On Fig. 4 the output voltage for 500 Ohm load resistance is given.



a) with separated R, L and C elements.

b) when the passive components are modelled behaviorally.

Fig. 4 Output voltage.

The received simulations results for the output voltage with respect to the load resistance are given on Fig. 5.

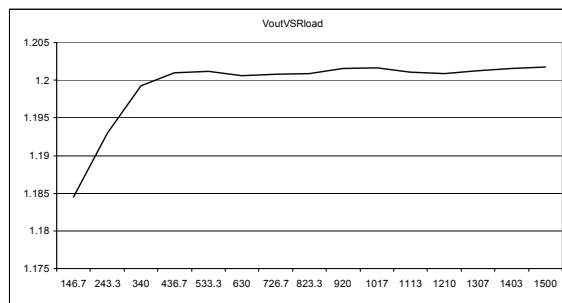


Fig. 5 Vout as a function of the load resistance.

The described model of the control system is fully behavior, based on the mathematical equations and voltage levels comparison.

In Table 1 some simulation results from the model with separated R, L and C elements are given.

Table 1 Simulation results;  $V_{in} = 3.3V$ ;  $f_s = 200MHz$ ;  $f_c = 5MHz$

L = 100 nH, C = 10 nF				
Vout (av), [V]	1.2	1.2	1.2	1.2
Iout (av), [mA]	24.0	12.0	6.0	2.38
RL, [ $\Omega$ ]	50	100	200	500
Pin, [mW]	35.29	17.85	11.88	8.84
Pout, [mW]	28.8	14.4	7.2	2.88
$\eta$ , %	81.6	80.6	60.0	32.5

## 5. CONCLUSIONS

The represented principals of using high level behavior languages for analog and mixed signals systems modeling gives satisfactory results. They allow using mixed mode models to optimize system structure on high level. Other main advantage is the fast way the simulations are performed and ease of making changes.

The technology independence of the model can be considered as its drawback when precise modeling is needed. The technology parameters can be included at element level. This will make models precise but simulation time may increase.

As it is not technological based model there are no error dependencies implied and no accuracy checks in comparison with evaluated monolithic structures are made. Further work in this field is intended to clear out the model precision dependences and functionality.

## 6. FURTHER WORK

The work in this area will continue further on evaluating modeling principals and clearing the design flow with using HDL-AMS for high level design descriptions.

## 7. ACKNOWLEDGMENTS

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