BEHAVIOR MODELING OF ELEMENTS OF THE STRUCTURE OF ANALOG ARRAY

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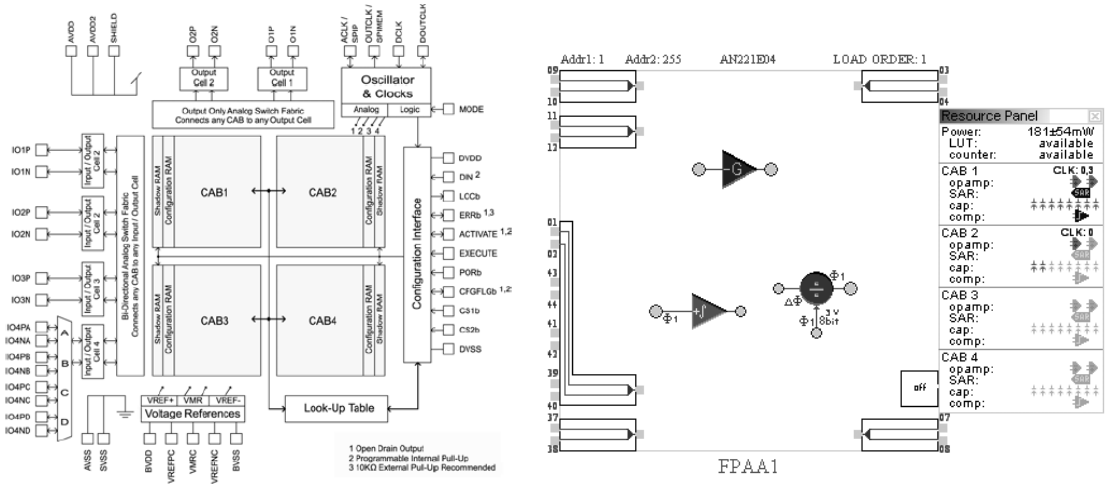
In this paper the way of creating universal AMS (Aanlog and Mixed Signals) HDL (Hardware Description Language) models for the elements of the structure of Field Programmable Analog Array (FPAA) chips is discussed. These are programmable chips that perform analog functions and are similar to digital FPGA (Field Programmable Gate Array) chips. They give analog designers flexibility to easily evaluate and prototype different designs. Analog description languages such as VHDL-AMS and Verilog-AMS gain popularity as instruments for mixed signals modeling and simulations. They make it easy to model systems on high behavior level of description, to perform mixed-domain simulations and to design using modern system on chip approach. Building universal models of the elements of FPAA structure will allow more complex simulations to be made with universal HDL-AMS simulators.

Keywords: FPAA, VHDL-AMS, Modeling, Simulations, Behavior description.

1. INTRODUCTION

Field programmable analog arrays are becoming more and more popular for the ability they give analog designers to evaluate different design structures and to configure the chip fast. As can be seen from [2] and [3] different design can be configured and implemented. The FPAA structure consists of so called "Configurable Analog Blocks" - (CABs) which are connected to each other and to Input/Output blocks by a fabric of programmable interconnect resources [4]. The key element is operational amplifier with switch capacitors technology used to implement different functions like inverters, integrators, differentiators and others. The structure of FPAA chip of Anadigm is presented on Fig. 1a) and device in Anadigm Designer Software Tool with available resources – on Fig. 1b).

These types of chips give the analog designers the freedom to reconfigure designs and to prototype, not long ago a privilege only for digital designers. Thus the parallel between FPAA and FPGA is direct. The parallel can be made also in design tools available. Behavior description languages, such as VHDL and Verilog-HDL that allow digital designers to create, describe, simulate and synthesize VLSI circuits, were developed and extended to support analog models. This provides the ability to describe behaviorally not only digital but analog and mixed signals designs. The use of such languages provides the tool independency of designs as both VHDL-AMS and Verilog-Analog/AMS are IEEE standards. This way analog and mixed signals designs can be evaluated at behavior level on different software platforms.



a) Chip architecture **b) Device in Anadigm Designer 2 Software Tool**

Fig. 1 Overview of FPAA device.

Building behavior models of FPAA elements will give the ability to make complete system simulations with different external elements and for different domains – modeling electrical engines, hydraulic machines, etc. Behavior models reduce the simulation time and increase design readability and reuse.

2. DESIGN PRINCIPALS

There are different ways to define system model using HDLs. A system, which consists of different sub-modules, can be modeled by providing behavior models for these blocks, then to connect them in structural model representation as shown on Fig. 2.

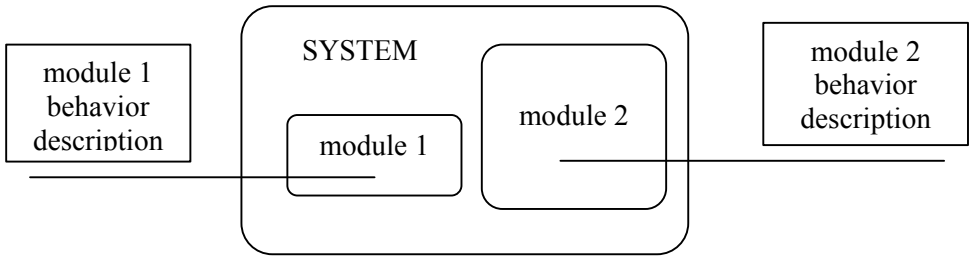


Fig. 2 Defining system by its modules behavior.

This way gives the ability to refine each model, verify it and reuse it when needed for other designs. This also gives the ability to create models for different purposes like pure behavior simulation, fault tests, etc. and easily replace them in system model.

Other way is to create behavior model for the entire system. This description must provide information for all parameters and dependencies system behavior is founded

on. Sometimes these models might be more complicated for the complex equations they require.

As mentioned above the principals of design with FPAA are to use CABs contained elements to build desired function. If behavior models are built for the elements then the method defined on Fig.1 can be used to create structural models based on these elements.

The main element in CAB is operational amplifier, which with properly configured switching capacitors represent different functions. Scheme to perform inverting gain element is given on fig. 3. This represents the main way to build elements available in FPAA array. Peculiarity here is the differential input and output.

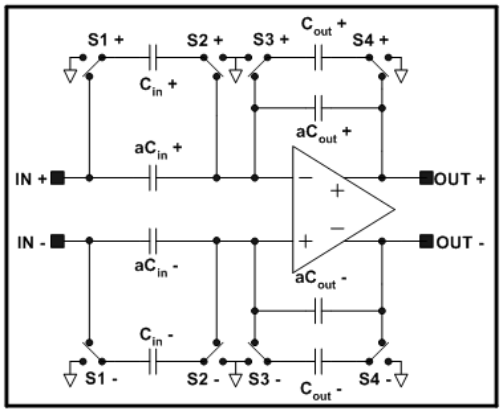


Fig. 3 Anadigm FPAA Inverting Gain Circuit.

The transfer function for this circuit is given with Equation 1.

Equation (1) $$V_{out}(s)/V_{in}(s) = -G.$$

Behavior model for the circuit can be build based on behavior models of the operational amplifier, capacitor and switch. Sample circuit is given on fig. 4.

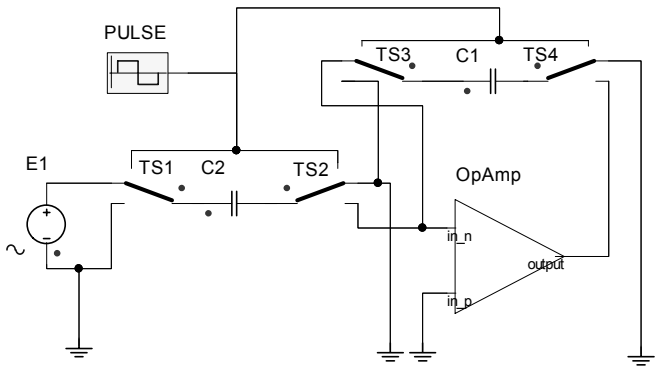


Fig. 4 Switched capacitor inverter.

To evaluate VHDL-AMS models Simplorer simulator software tool by Ansoft is used. This is universal simulator tool which supports VHDL-AMS models. Elements are defined in schematic sub-sheets and connected together graphically – Fig. 4.

Here the models used for the elements are behavior. They are given in Table 1.

Table 1 VHDL-AMS codes for operational amplifier, capacitor and switch.

Operational amplifier

```
ENTITY      OpAmp IS
      generic( vdd : voltage := 15.0;
               vss : voltage := -15.0;
               gain : real := real'high);
      port( terminal in_p, in_n, output : electrical);
END ENTITY OpAmp;
ARCHITECTURE arch_ OpAmp OF OpAmp IS
      quantity vin across in_p to in_n;
      quantity vout across iout through output;
BEGIN
      if(vin'above(vdd/gain)) use
            vout == vdd;
      elsif not vin'above(vss/gain) use
            vout == vss;
      else
            vout == vin* gain;
      end use;

      break on vin'above(vdd/gain),
vin'above(vss/gain);
END ARCHITECTURE arch_opAmp;
```

Capacitor

```
ENTITY Cap IS
   generic (C : capacitance := 1.0e-6);
   port (  terminal p,n  : electrical);
END ENTITY Cap;
ARCHITECTURE C_arch OF Cap IS
  Quantity v across i through p to n;
   BEGIN
        i == C*v'dot;
   END USE;
END ARCHITECTURE C_arch;
```

Switch

```
ENTITY Switch IS
   port (quantity ctrl : real := 0.0;
         terminal n1,n2  : electrical);
END ENTITY Switch;
ARCHITECTURE SW_arch OF Switch IS
   quantity v across i through n1 to n2;
BEGIN
   break on (ctrl 'ABOVE(0.0));
   if (ctrl 'ABOVE(0.0)) use
      v == 0.0;
   else
      i == 0.0;
   end use;
END ARCHITECTURE SW_arch;
```

The descriptions are fully behavior and the elements are ideal. More detailed codes can be used, of course, to precise the models if needed.

3. EXPERIMENTAL RESULTS

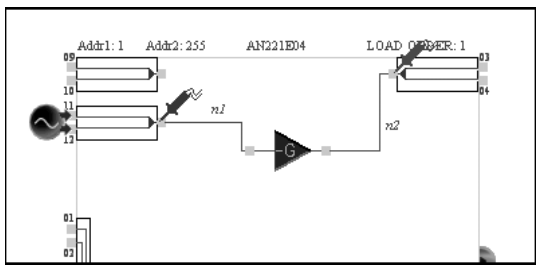


Fig. 5 Inverter Gain CAM simulation scheme.

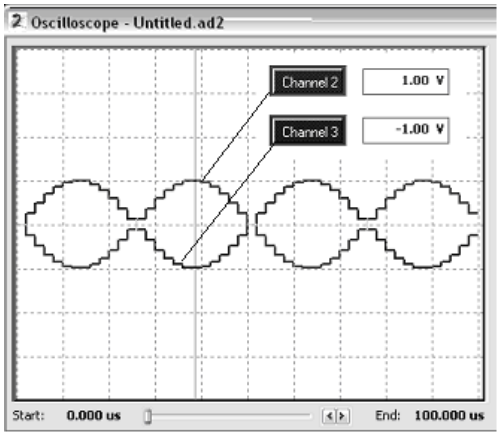


Fig. 6 Results from Inverter Gain simulations with AnadigmDesigner2 tool.

Simple configuration will be used to evaluate principals of model creation. Inverter is implemented in FPAA chip and simulated using Anadigm Designer 2

software tool. The scheme is given on Fig. 5. The element is connected to the input and output cells of the chip. Signal generator is connected to the input cell. Measurement markers are put on the input and output of the inverter.

On Fig. 6 simulation results for the Inverter Gain element, shown on Fig.3 are given. It is implemented in FPAA chip in simulations using Anadigm Designer 2 software tool by Anadigm. The CAMs setting are as: Clock 250 kHz; Gain 1. The input signal is 20 kHz sine signal with 1V amplitude.

On Fig. 7 simulation results for the circuit from Fig. 5 are given. As mentioned above they are received from Simplorer simulator.

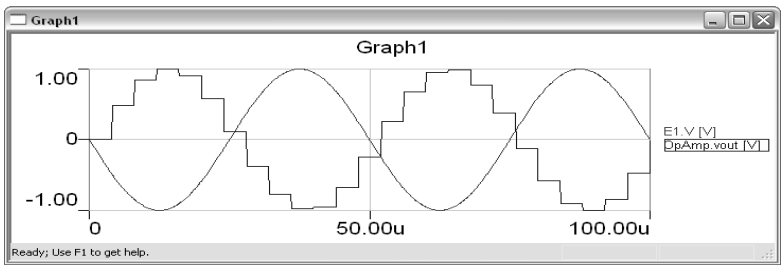


Fig. 7 Simulation results for behavior model at 250 kHz clock frequency.

The form of the output signal at both simulations depends on the switch clock frequency. Simulation results for 4000 kHz clock frequency are given on Fig. 8 and Fig. 9. As can be seen the outputs are smoothened for the higher clock frequency.

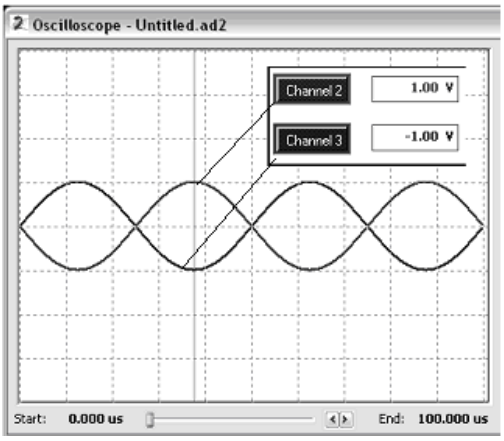


Fig. 8 Simulation results for Inverter CAM at 4000 kHz clock frequency.

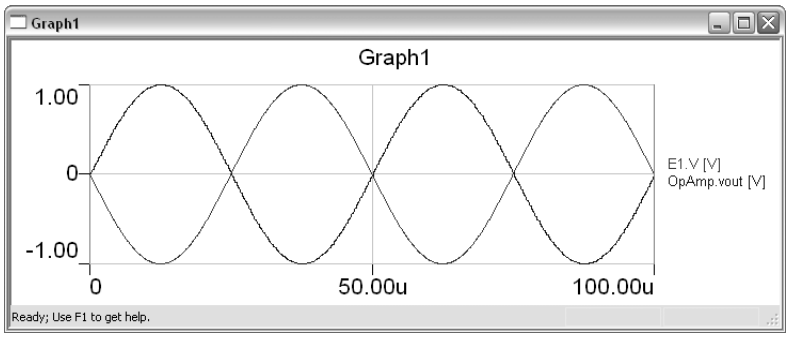


Fig. 9 Simulation results for behavior model at 4000 kHz clock frequency.

4. CONCLUSIONS

Presented way of creating behavior HDL models for elements of the structure of FPAA chip gives satisfactory results with respect to Anadigm Designer 2 simulator. The clock frequency dependencies for both simulations are regular and behavior model follows FPAA inverter relevance.

5. FURTHER WORK

The work on this project will continue with evaluating such type of models for other elements available in FPAA structure. Besides behavior models, based on components transfer functions will be evaluated.

6. ACKNOWLEDGMENTS

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7. REFERENCES

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