THE I/O OUTPUT BUFFER AUTOMATED DESIGN WITH CONSIDERATION OF SIMULTANEOUSLY SWITCHING NOISES

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The sizing rules method for analog CMOS I/O output buffer circuit design that consists of two pre-buffers (inverters) and output inverter is presented. The sizing rules method efficiently captures design knowledge on the technology-specific level of transistor pair groups. This reduces the preparatory modeling effort for I/O circuit design. No expert knowledge about the circuit is required as in most knowledge based optimization tools.

1. INTRODUCTION

I/O devices are an important part of integrated circuits: either in terms of elements and are in mixed-signal systems, pad driving, or clock generation. Despite their importance, design automation for analog circuits is still behind digital, even analog circuit automation tools. As a consequence, analog components are often bottleneck in the design flow.

Many attempts have been made to mimic the designer's experience and knowledge into automation tools for analog design, too [1]. Optimization tools are now categorized into two different streams: the knowledge-based and the optimization-based. In the knowledge-based stream, the designer extracts design equations and integrates them into the tool to be reused for the same topology. In the optimization-based approach, the optimizer searches the design space for the circuit that satisfies certain constraints and minimizes certain objectives. The optimization - based approach, in its turn, divided into: equation-based optimization and simulation-based optimization. In the equation-based optimization, circuit evaluation is done through pre-derived equations for performance specifications, initially extracted by the designer or by symbolic analysis. In the simulation-based optimization, the specifications are directly measured from the output waveforms of a simulator (SPICE). The simulation-based advantages over the equation-based approach are:

· Accurate simulation models are used instead of approximate equations

· No long preparatory effort to extract all the describing equations. Practically, the extraction may fully rely on simulator capabilities.

In this work the simulation based sizing method suggested. The re-sizing consequence is based on exact formulas and curves which allow making optimization process very fast without any specific knowledge.

2. OUTPUT BUFFER IMPLEMENTATION OF I/O CIRCUIT

The Output Buffer consists of two pre-buffers (inverters) and output inverter as shown in Figure 1.

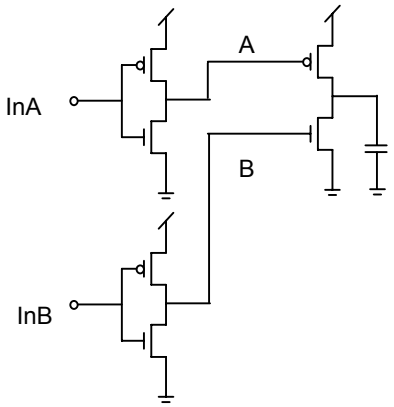

Figure 1. Schematic capture of I/O circuit output buffer

The first step of the optimization starts from DC analysis. The program check does the Output Buffer handle the desired drive strength. Drive Strength is measured with SPICE simulation as presented in Figure 2.

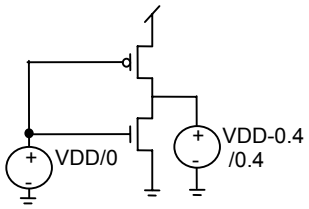

Figure 2. Schematic capture of I/O circuit output buffer

When DC parameters reached their desired values, the program started to check the transient parameters. The main parameters are: Propagation Delay- defined as a time interval when input and output voltages intersect VDD/2 value [2].Rise/Fall time - defined as a time interval when signal rises from 0.1 x VDD to 0.9 x VDD and fall time is a time interval when signal falls from 0.9 x VDD to 0.1 x VDD [2], SSN (Simultaneously Switching Outputs) - defined as an inductive noise caused by several signals in a bus are switching simultaneously [3].

The main input variable that can be controlled to improve the circuit performances is the Input Slope (Slope is a time interval when signal rises from 0V to VDD or falls VDD to 0V)

3. EXPERIMENTAL RESULTS

The max rise/fall slope time that can handle the described pre-buffer is Tslope(rise/fall)=0.4*Tper[3] where Tper=1/F_{max} (F_{max}- is the maximal operating frequency). For Output Rise/Fall time this parameter is even less than Toutput(rise/fall)=0.3*Tper, because the parameter variance for output part of the I/O devices can be more than anywhere else in the chip.

Many process specific tests give the detailed Rise/Fall time dependence from transistor's main sizing parameters.

The good approximation shows that angular coefficient is equal to 0.94. It means that if the parameters do not meet the specification, the transistors should be resized with the given formula.

$$0.95*(W2/L2)/ (W1/L1) =Tedge2/ Tedge1 \quad (1)$$

$$Tedge2=0.95*(W2/L2) *Tedge1/ (W1/L1) \quad (2)$$

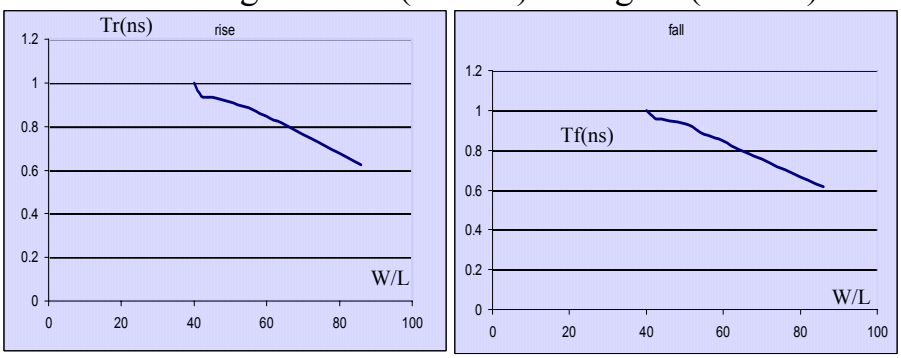

Figure 3. Rise/Fall time dependence from W/L

After resizing the angular coefficient can be recalculated if it does not match with the given value. The recalculation can be done after each time step. When the Rise/Fall time values meet the user-defined specification, the program starts to optimize the simultaneously switching noise value. The value can be calculated with the given formula.

$$V_{SSN} = L\frac{di}{dt} \quad (3)$$

where VSSN is the simultaneously switching noise, L - the equivalent inductance through which current must pass, and I is the output buffer current.

The inductance value is one of the main package parameters and very often cannot be reduced. The optimization is done to reduce the di/dt. It is experimentally proven that there is some point (pre-buffer sizes) for the given Rise/Fall times that the di/dt value is minimal.

When the SSN value is more than user-specified value, the program starts to reduce (increase) pre-buffer sizes until the Toutput (rise/fall)<0.3*Tper or further resizing does not bring to significant reducing of the di/dt value: for example W/Wnext=0.1*((di/dt)/(di/dt)next.

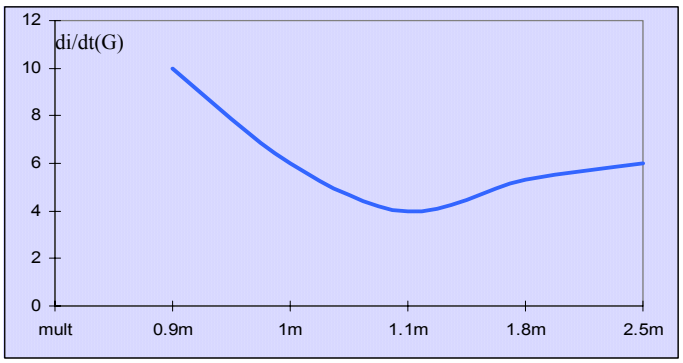

Figure 4. di/dt dependence from pre-buffer sizes

4. PROGRAM IMPLEMENTATION

The described design methodology is implemented in "Output Buffer Compiler" program (figure 5).

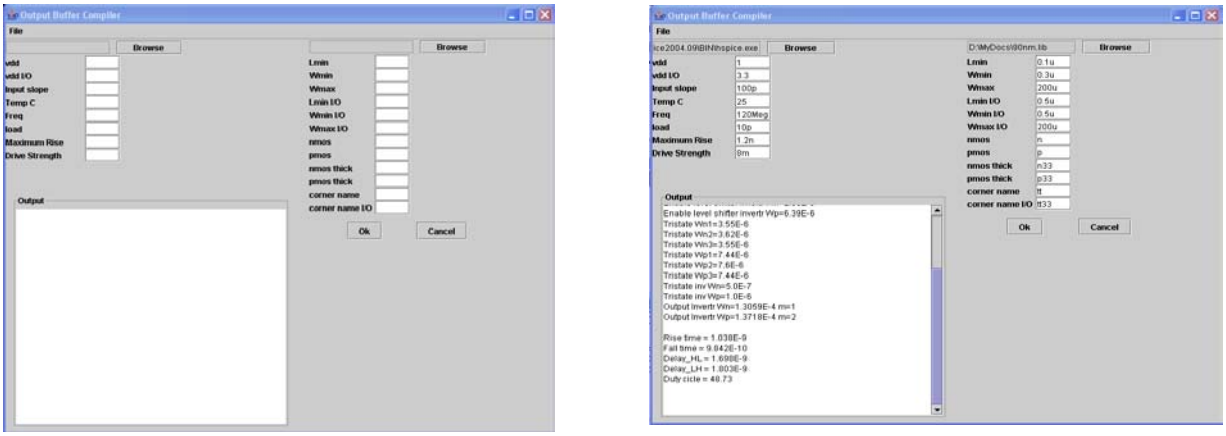

Figure 5.

Interface of the optimization tool The results of the optimization tool

User should enter process specific parameters and process library file to start the simulation. The main specific parameters of output buffer should be entered, too (For time being SSN calculated as the 0.25*VDD). The optimized and SPICE simulated parameters are plotted in the output part of the program interface

5. CONCLUSION

The new I/O circuit Output Buffer optimization tool has been presented. No any specific knowledge is needed to design one of the most difficult sub-circuits of I/O devices. The tool is 2-3 times faster than any simulation-based tool, because of dulcified optimization methodology, it gives an opportunity to get the first order sizes of an output buffers and get fast information about noises that caused by package inductance.

6. REFERENCES

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