NEW MODULAR CURRENT DEVICES FOR TRUE CURRENT MODE SIGNAL PROCESSING

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A CMOS07 technology chip was designed and manufactured containing building blocks allowing simple and fast modular design of the new devices CDTA and CCTA, specially developed for current mode analog signal processing as well as many other functional circuits. The blocks as the current conveyors, differential current amplifiers and transconductance stage were produced at the chip. Measurement results are introduced and discussed in this paper

Keywords: Analog signal processing, modern active blocks, measured results

1. INTRODUCTION

As the modern current mode devices we consider mainly such active devices like the COA (*Current Operational Amplifier*) [1], CDTA (*Current Differencing Transconductance amplifier*) [2] and CCTA (*Current Conveyor Transconductance amplifier*) [4,5]. This work is focused to design of CDTA and CCTA, because the COA can be always reached by a convenient connection of CDTA or CCTA with "infinity" gain. The above mentioned circuits are mostly designed as two-stage (input-output) devices. It allows us to design the input and output stages as independent **modules** designed in consideration of simple mutual connection. Such a way designed blocks can be then simply combined to create CDTA, CCTA and many other possible devices with regards to desired performance parameters like power, speed, accuracy etc.

1.1 CDTA short description

The CDTA has difference low-impedance current inputs p and n. The difference of input currents flows out of the z-terminal into an outside load. The voltage across the z-terminal is converted through a transconductance gm into a current that is generally led in a number of copies into the out-terminals. The transconductance can be either fixed or given by external component or controlled electronically from an auxiliary terminal as well.

1.2 CCTA short description

CCTA is designed for usage mostly in current mode circuits but it is also good choice in case of hybrid (voltage-current) circuits. The CCTA consists from two basic blocks. The first stage is represented by the current conveyor CCIII that is followed by double output transconductance "*gm"* stage. The input behavior is mostly given by properties of the CCIII conveyor. Conveyor output current flows out of the CCTA terminal "z" into an outside load. The voltage across the z-terminal is processed like

in CDTA and it is converted through a transconductance gm into a two output currents with opposite polarity.

As it was already introduced in [4], the CDTA can be simply realized by connection of the differential current amplifier with gain B=1 (current differentiator) and transconductance stage as well as the CCTA is possible to build from current conveyor CCIII and transconductance "*gm*" stage. Different topologies of the blocks were realized and they are discussed and compared below.

2. CMOS Realization of the Building Blocks

In the chapter the individual circuit blocks are shortly introduced including circuit topology, realized schematic, layout and measurement results. Minimum demands for possible processed signals are maximum current I_{max}=±100uA and voltage V_{max}=±0.5V. Parameter summary and cell comparison can be found in Conclusion

2.1 Current differentiator based on current mirror design

This topology limitation is mostly in the current amplitude when we use the cascode connection which is necessary for good current mirror output impedance and precise circuit behavior. Advantage of the circuit is high speed but higher input impedance. The possible principle schematic is in Fig.1a, realized Cadence schematic is shown in Fig.1b. Layout and input to output characteristics are in Fig.1c and Fig.1d respectively.

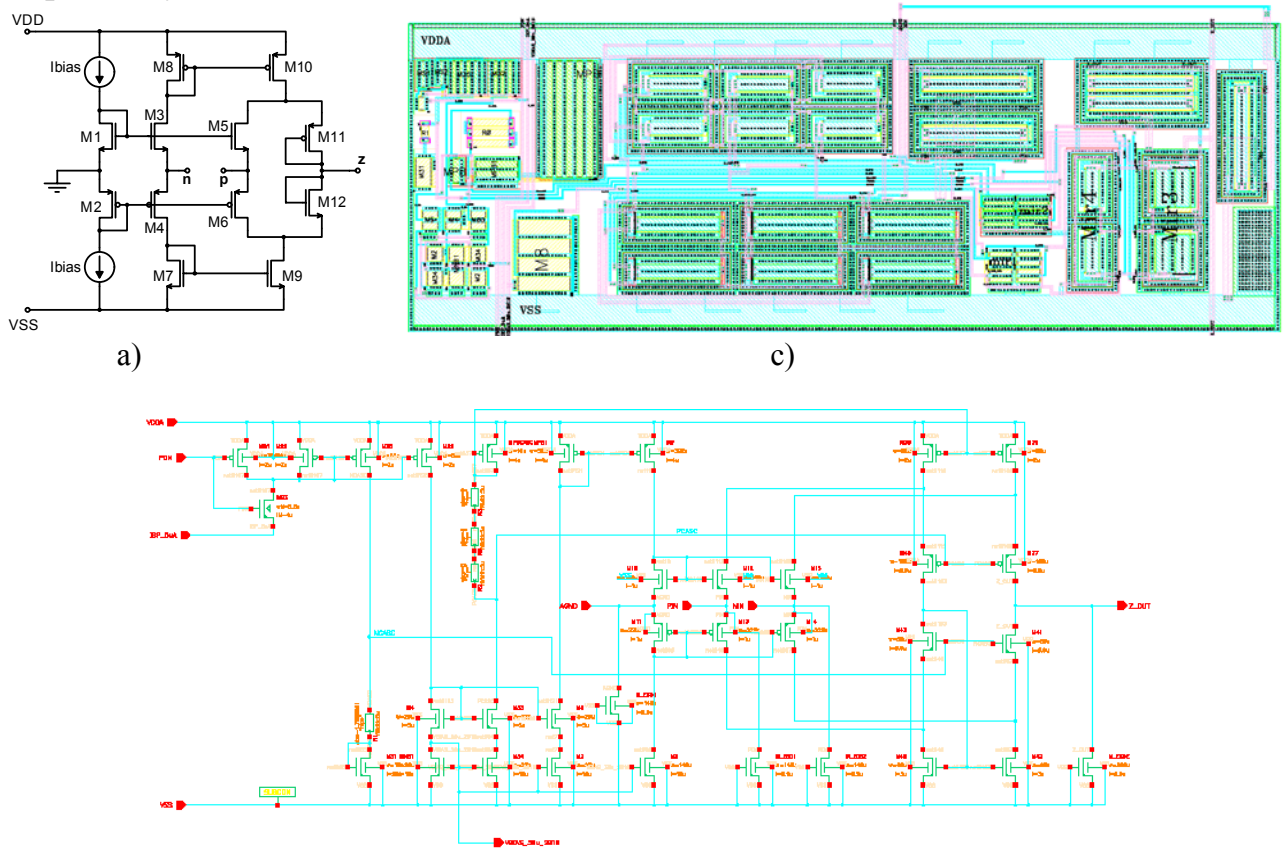


Fig. 1: Current differentiator based on current mirrors
a) principal schematic, b) realized schematic, c) layout

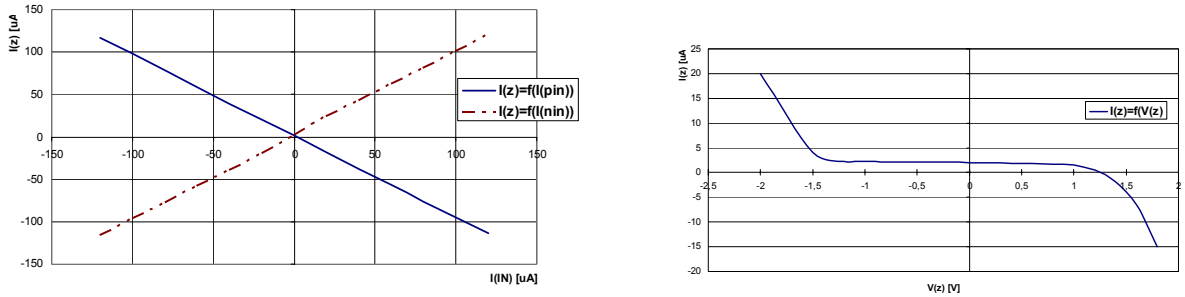
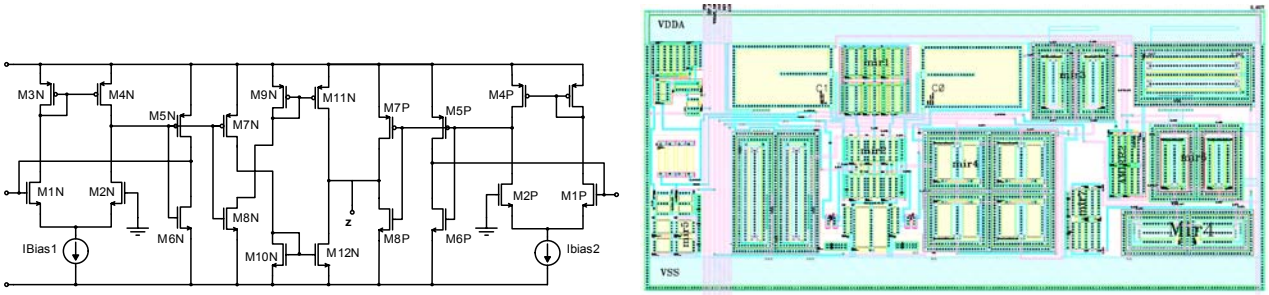


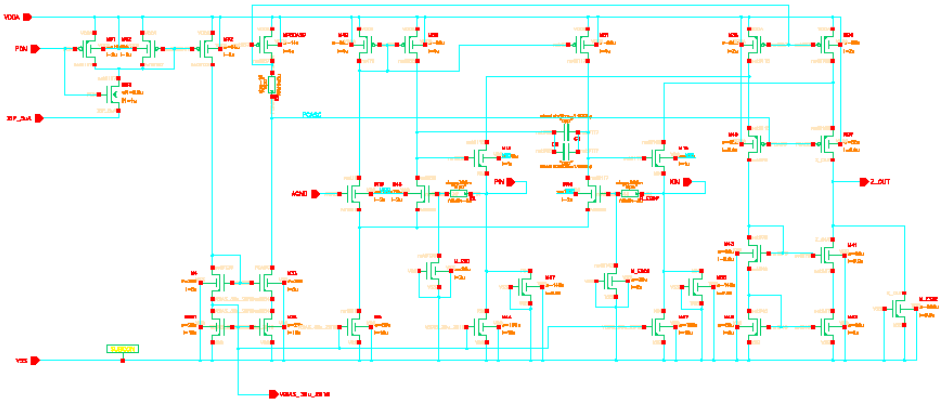
Fig. 1d: Current differentiator measured characteristics
a) output current depending on the input currents
b) output current depending on output voltage (output impedance)

2.2 Current differentiator based on opamp loop

Advantage of the topology is low input impedance but lower GBW.



a) c)



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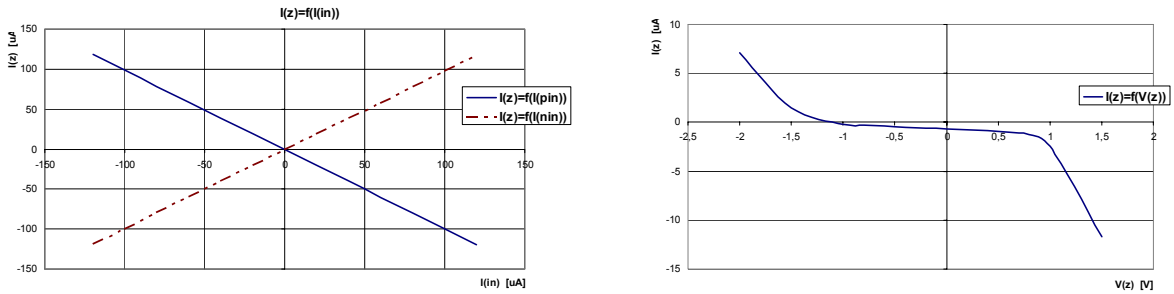


d)

Fig. 2: Current differentiator based on opamp structure a) principal schematic, b) realized schematic, c) layout, d) graphs *I(out)=f(I(pin),I(nin))* and *I(out)=f(V(out))* -> Zout

2.3 Current conveyor CCIII build on current mirror topology

The topology of the circuit input is similar like for current differentiator and from that reason the limitation in current amplitude comes in account, but more serious is the constraint in input voltage amplitude at node Y due the MOS threshold voltages, even for low voltage design. For 5V supply voltage the demanded input signal V(Y)=±0.5V was satisfied.

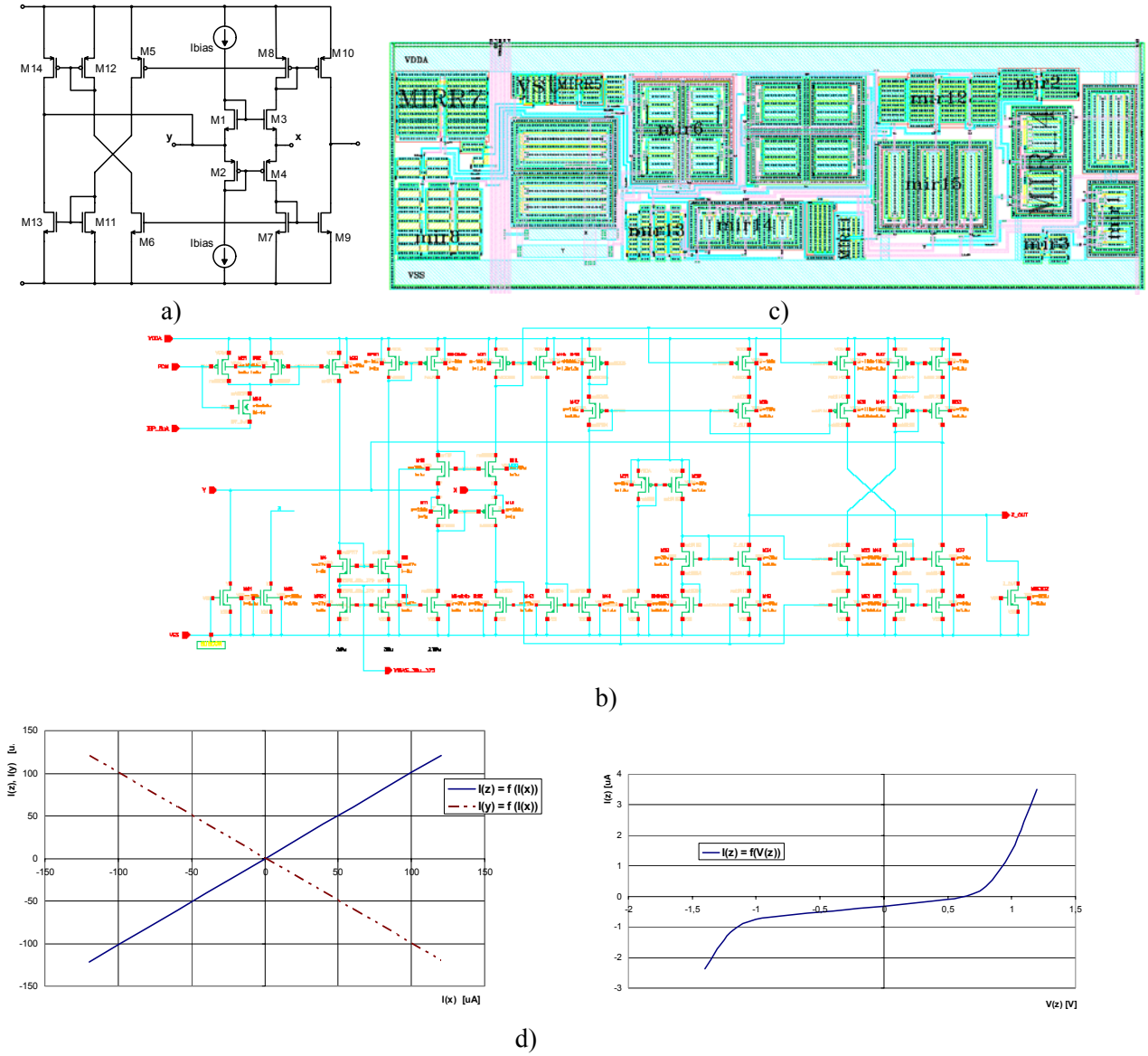
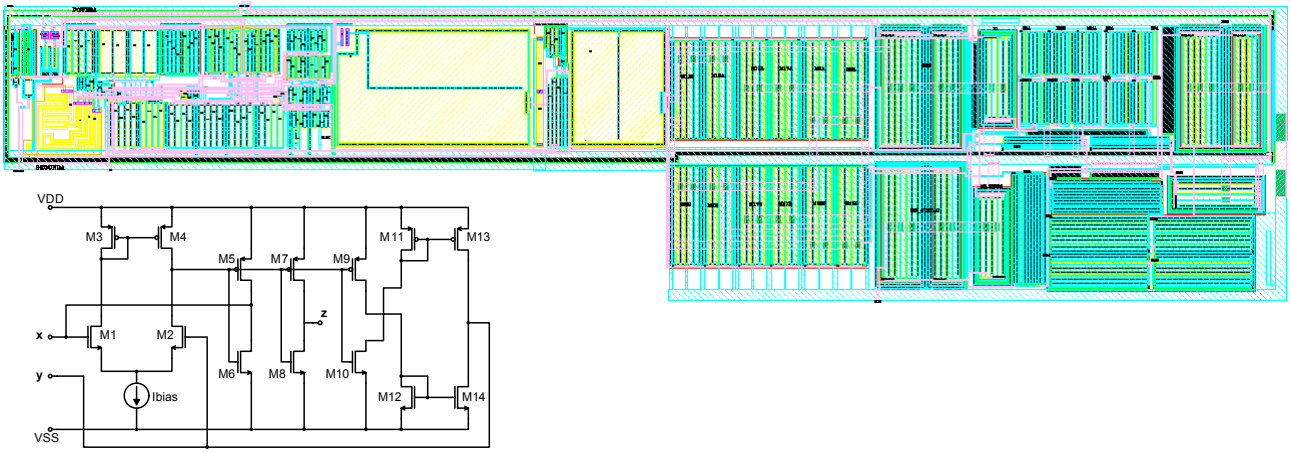


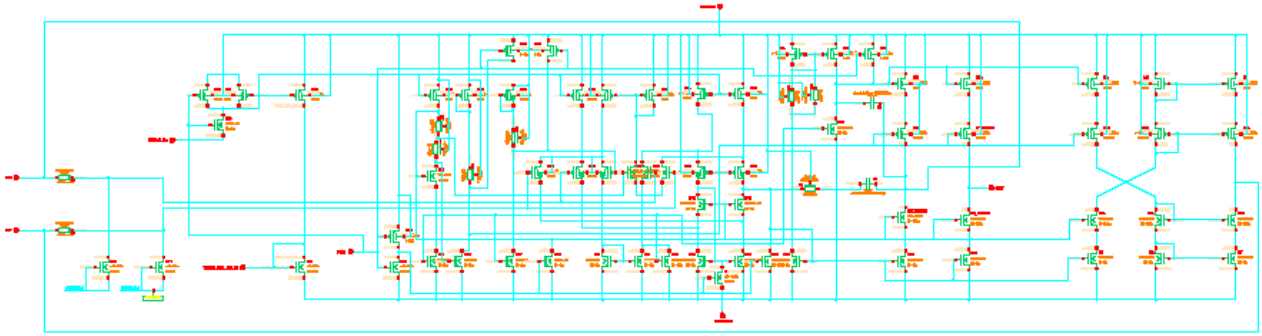
Fig. 3: Current conveyor CCIII based on current mirrors a) principal schematic, b) realized schematic, c) layout, d) graphs *I(z,y)=f(I(x))* and *I(z)=f(V(z))* -> Rout(z)

2.4 Current conveyor CCIII build on opamp

The CCIII conveyor was build on robust Rail-to-Rail opamp with class AB output stage. Thanks to the topology its input can work in the full supply voltage range and it is able to managed currents up to ±3.5mA while its current consumption without signal is about 1mA. It is paid by lower GBW.



a) c)



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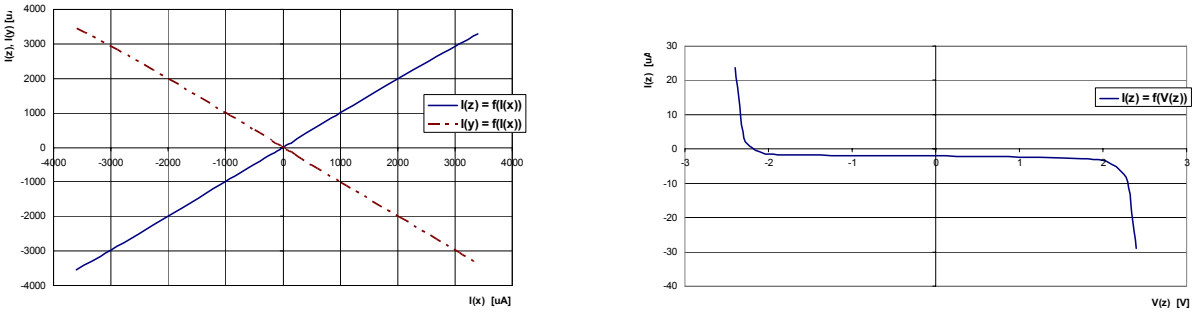


d)

Fig. 4: Current conveyor CCIII based on opamp a) principal schematic, b) realized schematic, c) layout, d) graphs *I(z,y)=f(I(x))* and *I(z)=f(V(z))* -> Rout(z)

2.5 Transconductance "gm" stage

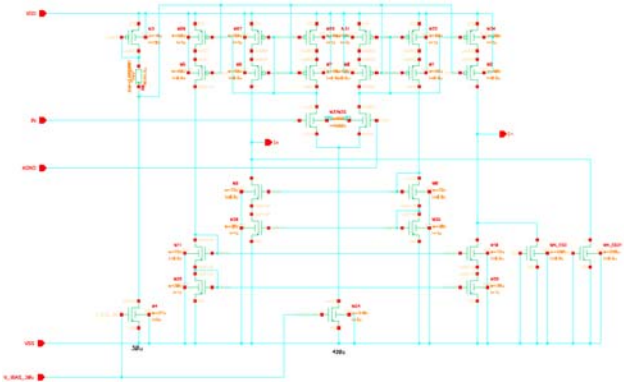


Fig.5a

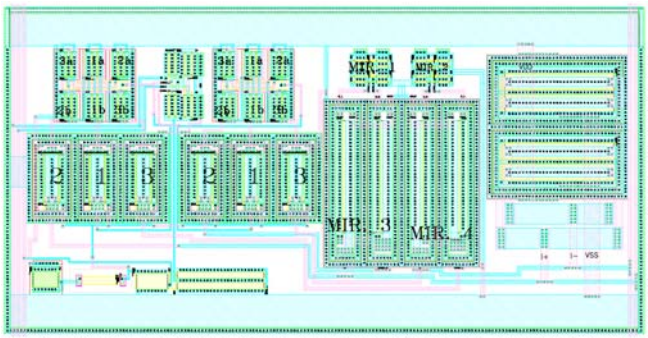


Fig.5b

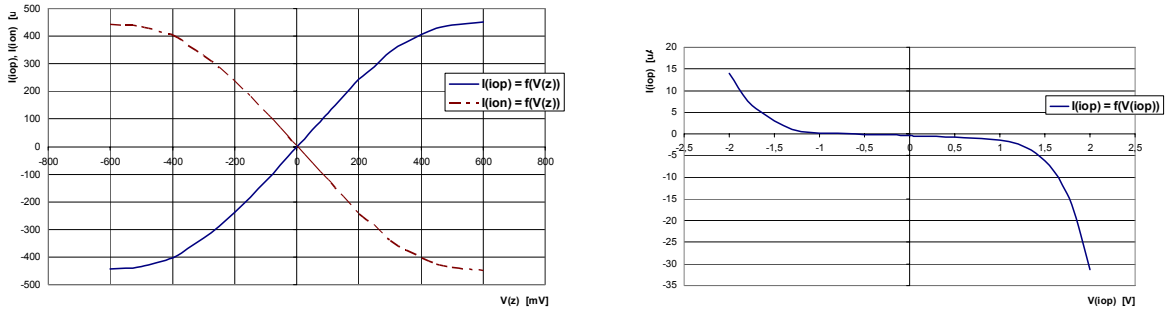


Fig.5c

Fig.5: Transconductance stage with fixed gm
a) schematic, b) layout, c) transfer graphs I(iop),(ion) = f(V(in)) -> *gm*
output graphs I(iop) = f(V(iop)) -> Zout

The realized transconductance stage with two opposite current outputs has fixed (uncontrollable) *gm* parameter. It is about 1,24mA/V in our design

3. CONCLUSION

Table 1: Measured results of the DC parameters; Supply Voltage V_{dd} = 5V

	V_{in} range [V]	V_{out} range [V]	I_{in} (max) [µA]	V_{offset} [mV]	I_{offset} [µA]
Diff I_mirr	N/A	-1,2 ÷ 0,8	-150 ÷ +150	5	1,4
Diff I_opa	N/A	-0,8 ÷ 0,7	-200 ÷ +200	7	0,6
CCIII_mirr	-0,7 ÷ 0,6	-1,1 ÷ 0,6	-150 ÷ +150	2,4	0,8
CCIII_opa	VSS ÷ VDD	-2 ÷ +2	-3600 ÷ +3600	0,36	1,6
Gm stage	-0,2 ÷ +0,2	-1 ÷ +1	N/A	N/A	P(out)=-2,1; N(out)=1,1

Table 2: Measured results of the AC parameters; Supply Voltage V_{dd} = 5V

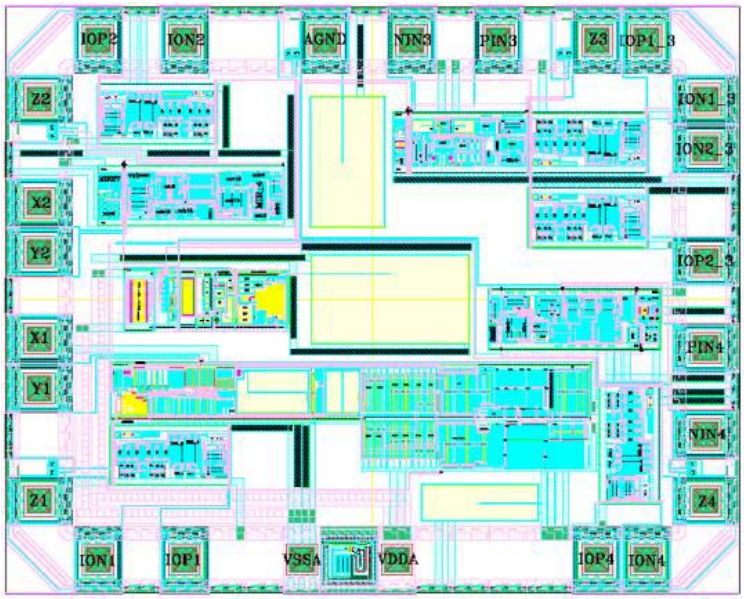
	Z_{in} (*I inputs*)	Z_{out}	Gain(I)	BW(-3dB)/GBW
Diff I_mirr	380 Ω	3,4 MΩ	B_0 = 1	BW = 180MHz
Diff I_opa	20 Ω	2,1 MΩ	B_0 = 1	BW = 100 MHz
CCIII_mirr	240 Ω	2.5 MΩ	B_0 = 1	BW = 100MHz
CCIII_opa	10 Ω	5.2 MΩ	B_0 = 1	BW = 50 MHz
Gm stage	∞	2.4 MΩ	*gm* = 1.24 mA/V	BW = 220 MHz
CDTA_mirr	380 Ω	2.4 MΩ	B_0 = 4200	GBW = 35 MHz
CCTA_mirr	240 Ω	2.4 MΩ	B_0 = 3100	GBW = 28 MHz

Note: a) BW(-3dB) is measured as the 3dB bandwidth when current outputs are connected to low impedance nets
b) GBW is introduced for compensated (stable) circuit with Phase Margin PM = 60 deg

In the realized chip there were four new devices built from the above mentioned blocks by a cascade connection of four different input blocks together with transconductance output stage creating two CDTA and two CCTA devices. Unfortunately only the transconductance stage with fixed *gm* was manufactured. But

the transconductance stage with *gm* given by external resistor can be easy build up from any CCIII block by a convenient connection.

The all designed building blocks are able to process current at least 150 μA and voltages with amplitude ± 0,5V. The overview of the DC parameters is shown in Table 1, a comparison of the cells by AC behavior is given in Table 2. The offset parameters are introduced just for measured device but from the simulation the matching voltage offsets can be about 8mV and current matching offset up to 8uA for 6σ of the "normal distribution".



Because of the accessibility of the circuits outside of the package, ESD protections have been added to all external pins whose add extra parasitic capacitance as well as bondwires etc. If the circuits are buried in the chip, their GBW will increase rapidly.

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