ANALYSIS AND DESIGN OF CMOS SMART TEMPERATURE SENSOR (SMT) WITH DUTY-CYCLE MODULATED OUTPUT

Kataneh Kohbod, Gerard C.M. Meijer

Electronic Instrumentation Laboratory, Delft University of Technology
Mekelweg 4, 2628 CD Delft, the Netherlands.
Phone +31 15 2785026; Fax: +31 15 278 5755; E-mail: a.heidary@tudelft.nl

In this paper the design of a CMOS smart temperature sensor (SMT) with duty-cycle modulated output is presented. The effects of the main non-idealities such as amplifier offset and mismatching of components have been addressed. It is shown that these effects can be eliminated or reduced by applying both dynamic-offset cancellation and dynamic-element matching. A complete SMT has been designed for implementation in 0.7μm standard CMOS technology. Simulation results have been presented.

Keywords: Sensors, Temperature sensors

1. INTRODUCTION

A smart temperature sensor (STS) has the attractive feature that it can straightly be connected to a microcontroller or computer (figure 1).

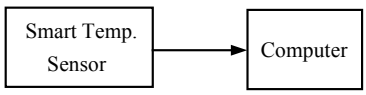


Figure 1: A temperature measurement system with a smart sensor.

The first STSs introduced in the market were devices with a duty-cycle modulated output [1]. Nowadays, in the market also many STSs can be found with digital output signals. As compared to an STS with a digital output, the ones with a duty-cycle output have some attractive features, such as simplicity and that no internal or external clock signals are required. Moreover, duty-cycle modulated signals have an average value proportional to the duty-cycle. This offers the advantage that with a simple low-pass filter also analog output signal can be obtained. So both digital signals and analog signals can be offered to applicants. To distinguish STSs with a duty-cycle from those with a digital output, we will refer to the first ones with the abbreviation SMT.

The first SMTs were designed in BICMOS technology [1]. Since CMOS technology is cheaper than BICMOS technology, it makes sense to design also CMOS versions. In [4], highly interesting designs of high-precision CMOS STSs have been presented. Those devices use an internal sigma-delta converter. In this paper, we will introduce a

similar device, but implemented with a duty-cycle modulated output and modified with features that make it compatible with the original BICMOS version of Smartec [1].
It will be shown that the typical non-idealities of CMOS technology, such as component mismatching can be overcome by applying techniques such as chopping, auto-zeroing and dynamic element matching. Simulation results for a chip that is designed for implementation in 0.7μm standard CMOS technology will be presented.

2. TEMPERATURE TO DUTY-CYCLE CONVERSION:

Figure 2 shows the main principal of the temperature sensor with duty-cycle output [1]. The duty-cycle, $M(T)$, equals:

$$M(T) = \frac{t_{\mathrm{H}}}{t_{\mathrm{H}} + t_{\mathrm{L}}} = \frac{I_2}{I_2 + I_1} \tag{1}$$

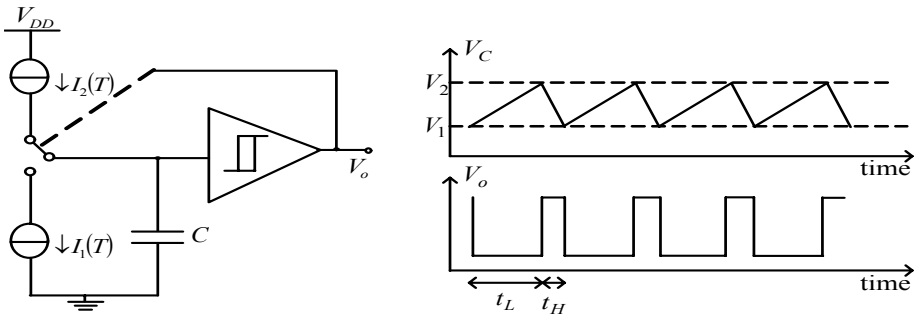


Figure 2: Temperature to duty-cycle converter and some related signals

The currents $I_1(T)$ and $I_2(T)$ satisfy the equations [2]:

$$I_1(T) = I_{\mathrm{BE}} - I_{\mathrm{PTAT}}, \tag{2}$$

$$I_2(T) = -K_1 I_{\mathrm{BE}} + K_2 I_{\mathrm{PTAT}}. \tag{3}$$

Where I_{BE} and I_{PTAT} are the currents derived from V_{BE} and $V_{\mathrm{PTAT}} = (kT/q) \ln n$. If we make $I_{\mathrm{ref}} = I_1(T) + I_2(T)$ temperature independent, then the duty-cycle will be linearly related to the temperature. Figure 3 shows the principle the circuit that we applied for the novel SMT implemented in CMOS technology. When we initially suppose that, $v_{\mathrm{io}} = 0$, then $I = V_{\mathrm{PTAT}} / R_{\mathrm{PTAT}} = I_{\mathrm{PTAT}}$. When S_1 is in position 1 and S_2 is in position 2 we will have:

$$I_{\mathrm{C1}} = I_{\mathrm{BE}} - I, \tag{4}$$

where $I_{\mathrm{BE}} = V_{\mathrm{BE}} / R_{\mathrm{BE}}$. In this case I_{C1} is the realization of $I_1(T)$ in equation 2. When S_1 is in position 2 and S_2 is in position 1, we will have:

$$I_{C2} = K_1 I_{BE} - K_2 I \,, \qquad (5)$$

where I_{C2} corresponds to $-I_2(T)$ in equation 3.To improve the power-supply rejection ratio (PSSR), all current sources will be implemented with cascoding transistors.

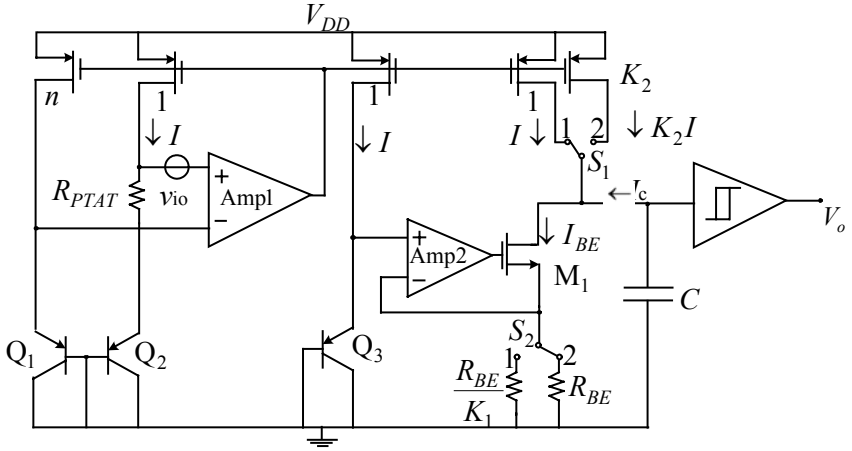


Figure 3: Temperature to duty-cycle converter in ideal case

3. MODERN CIRCUIT TECHNIQUES TO INCREASE THE ACCURACY OF CIRCUIT IN FIG. 3

3.1. Dynamic element matching (DEM)

To realize a precise PTAT voltage, the current-density ratio of n of the current mirror should be implemented with DEM [3]. It means that we use (n +1) equal current sources. And each time we connect n of them in parallel (figure 4). Then by rotating the position of transistors, after (n +1) cycles, the mismatches will be averaged out [5]. The switch-positions are controlled by the output signal of the sensor. To extract the temperature accurately, we should use ($n+1$) or an integer multiple of ($n+1$) cycles. We also applied DEM technique to implement the scaling factors K_1 and K_2.

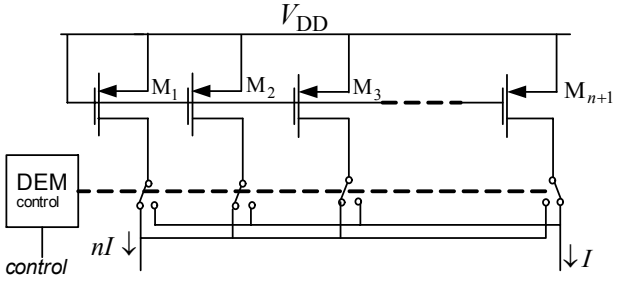


Figure 4: Dynamic element matching circuit for PTAT current density ratio.

3.2. Chopping.

Let's suppose the circuit (Fig. 3) is ideal, but that the op-amp AMP1 has an offset voltage v_{io}. Then:

$$I = (V_{PTAT} + v_{io}) / R_{PTAT} = I_{PTAT} + I_{off}, \quad (6)$$

where $I_{off} = v_{io} / R_{PTAT}$. To make the sensor compatible with Smartecs SMT we have choosen that $K_1 = 0.5$ and $K_2 = 3$. To evaluate the effect of the offset voltage, we substitute those values in Eqs (1)-(6), which yields for the duty-cycle $M(T)$ that:

$$M(T) = \frac{I_2 + 3I_{off}}{I_{ref} + 2I_{off}}. \quad (7)$$

This equation shows that with, for instance, $R_{PTAT} = 120$ kΩ at 27 ºC, $I_2 \approx 0.6$ µA and $I_{ref} \approx 1.4$ µA , that an offset voltage of 2 mV causes and error of more than 5ºC, which cannot be tolerated at all.

A usual way to remove the offset of an op-amp is using a chopper (figure 5).

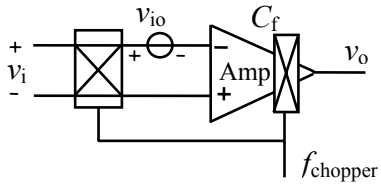


Figure 5: A chopped amplifier.

In that case, the input voltage v_i is modulated to a higher frequency and again demodulated to the base band. After demodulation, the offset voltage is modulated to a higher frequency, and therefore can be removed with a low-pass filter. In our circuit, the chopping frequency is in the range of a few kHz. The (digital) low-pass filter is implemented in the microcontroller. When we select the frequency of the chopper half of the output frequency, then the average duty-cycle of two concatenated period will amount to:

$$M(T) \approx \frac{I_2}{I_{ref}} \left(1 - \frac{6{I_{off}}^2}{I_{ref} I_2} + \frac{4{I_{off}}^2}{{I_{ref}}^2} \right). \quad (8)$$

Since the duty-cycle is not a linear function of the offset, after averaging we will have some residual error. As can be seen this residual error depends on temperature because I_2 is heavily temperature dependent. At a temperature of 27 ºC, an offset voltage of 2 mV results in a residual error of 0.13 ºC. To reduce this residual erro, besides chopping, we also need to apply auto-zeroing.

3.3. Auto-zeroing.

The applied auto-zero amplifier, AZA, uses a main amplifier for wideband signal amplification and a nulling amplifier for offset correction (figure 6) [6]. In our design the output signal of the SMT is used to control the auto-zeroing process.

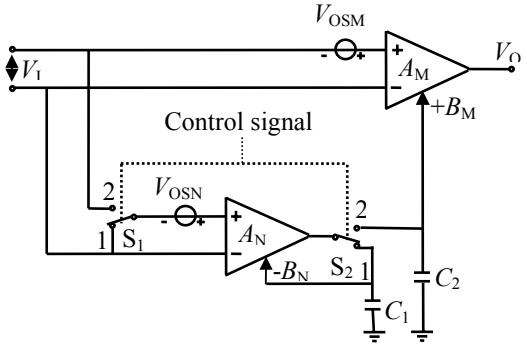


Figure 6: The block diagram of an auto-zero amplifier

Each of the amplifiers has an A and a B input channel, with open loop gains of A_M, $+B_M$ and A_N and $-B_N$, respectively. The input offset voltage of the A channels are denoted by V_{OSM} and V_{OSN}, respectively.

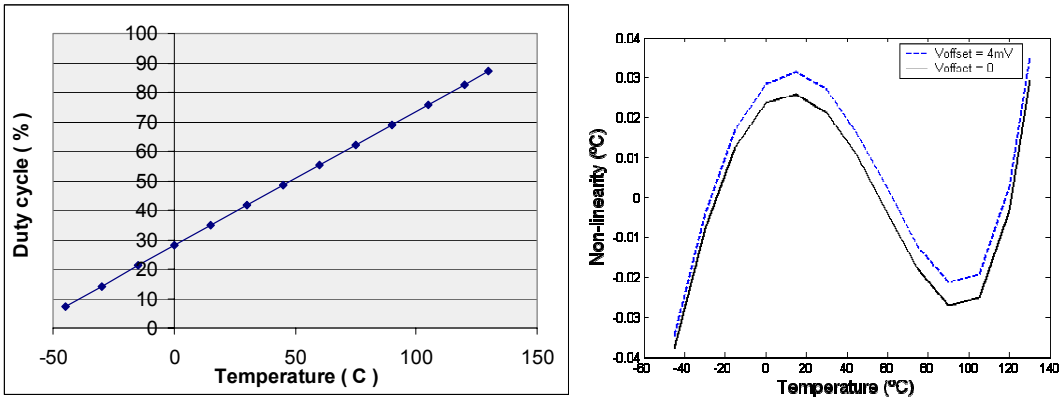
In the nulling phase, both switches are in position 1, and the nulling amplifier samples its own offset on capacitor C_1. In the amplification phase, when the switches are in position 2, the offset of both amplifiers is compensated. If we suppose that $A_M = A_N$, $B_M = B_N$, and $B_N >> 1$, the residual offset of the overall amplifier $V_{off\text{-}Eff}$ amounts to [6]:

$$V_{OS-Eff} = \left(\frac{V_{OSN} + V_{OSM}}{B_N} \right). \qquad (9)$$

4. SIMULATION RESULT

The complete circuit including dynamic element matching, chopping and auto-zeroing, has been designed for implementation in 0.7μm standard CMOS technology. Also curvature correction [2] is applied. Figure 7-a shows the duty-cycle versus the temperature. Figure 7-b shows the error caused by the nonlinearity and offset. It is concluded that after curvature correction, and for the temperature range of -45 ºC to 130 ºC, the non-linearity, is less than ±40 mK. Also it is shown, that the effect of even a big offset voltage v_{io} = 4 mV is efficiently removed by chopping and auto-zeroing.

Figure 8 shows the effect of supply voltage variations on temperature readout. This simulation result shows that for supply a voltage higher than 4.2V, the power supply rejection ratio, PSRR, is very high. However, for lower voltages the PSRR will deteriorate, which is probably due to the reduced output impedance of the current sources.



(a) (b)

Figure 7: (a) The duty-cycle versus temperature when the circuit is offset free. (b) The error due to non-linearity and offset.

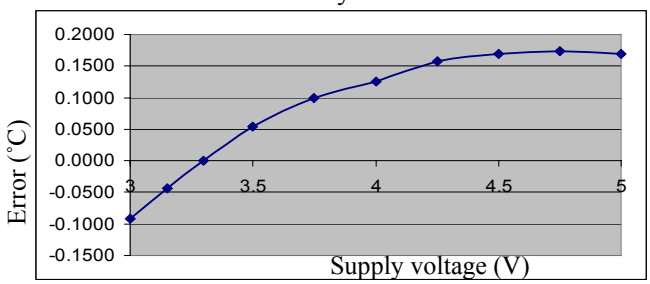


Figure 8: The error due to supply voltage variation at 0°C.

5. CONCLUSION

A design of an SMT with duty-cycle modulation output voltage in 0.7 μm CMOS technology has been presented. High performance is obtained by applying chopping, auto-zeroing and dynamic element matching. Simulation results show a nonlinearity as small as ±40 mK over the temperature range of -45 ºC to 130 ºC. It is shown that chopping and auto-zeroing can easily remove the effect of an offset as big as 4 mV. According to the simulations, the temperature error caused by power supply variations corresponds to about 250 mK over the voltage range from 3V to 5V.

6. REFERENCES

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