ANALYSIS AND DESIGN OF AN INTEGRATED INTERFACE FOR LEAKY CAPACITIVE SENSORS WITH EMPHASIS ON HUMIDITY SENSORS

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This paper presents the analysis and design of an integrated interface for leaky capacitive sensors. For such an application, we developed a novel type of interface circuit. With this circuit it is possible to measure the capacitance of a humidity sensor, at the presence of shunting resistors, with sufficient accuracy. For the signal processing, a relaxation oscillator is used with a modified front-end to optimize the interface circuit for immunity to leakage. Simulation results show, that a 500 kΩ shunt resistance (2μS) causes an error that corresponds to about 0.5% in relative humidity. The interface chip consumes about 1mA and, when implemented in 0.7μm standard CMOS technology, takes a chip area of 2mm^2.

Keywords: Capacitive, Humidity sensors, Interface

1. INTRODUCTION

Capacitive sensors are widely applied in cascade-sensor systems, such as liquid–level gauges, displacement sensors, pressure meters, accelerometers, humidity-measurement systems, etc, in which physical, mechanical or chemical quantities are converted into a capacitance value and further processed by an electronic circuit, called modifier. Depending on the application, the leakage could be a problem. For instance, for humidity sensor or sensors which work in a contaminated environment, resistive leakage is big problem. For such applications, its effect should be considered in the interface design.

An algorithmic way to improve the immunity of the measurements for leakage is reported in [1]. However, with this method the measurement time will increase considerably. It is clear that a better way to obtain leakage immunity would be keeping the DC voltage over sensor at zero level. An interface, based on this concept, with discrete elements, is reported in [2]. In this paper we present an integrated circuit that is based on the same concept [2]. However, since the challenges in integrated circuit are completely different from discrete ones, we end up with a different configuration for the front-end circuit.

The applied front-end circuit, for the interface for leaky capacitive sensor, is based on the use of the relaxation oscillator and a new capacitance-to-voltage converter. The output signals are period modulated and can directly be interfaced to a microcontroller. By applying temperature-independent biasing and when using the three-signal auto-

calibration technique, we can remove any error caused by temperature changes of the interface chip. In addition, errors caused by cross sensitivity of the sensing element, can be removed, for instance, by applying a temperature sensor at sensor location, and using a Look-Up-Table (LUT) to compensate for these temperature effects. Although we optimized the interface for humidity sensors, the main concept will work for all kind of capacitive sensors that are suffer from leakage. For experimental evaluation, the interface has been designed for a 0.7μm standard CMOS process. Design opportunities and constraints will be discussed together with simulation results.

2. CONVENTIONAL INTERFACE

Figure 1 shows a capacitive-sensor interface, implemented with a relaxation oscillator [3]. Some important signals are shown in Fig. 1-b. One measurement period T_{msm}, has eight different phases: at the start of phase one (Ph1), φ_1 goes high and a charge $q_1=V_{pp1}C_{o1}$ will be pumped into integrator capacitor C_{int}, where V_{pp1} equals the peak-to-peak value of the square wave-signal V_1 Next, this charge is removed by integration of I_{int}. In phase two (Ph2), φ_2 goes high and a charge $q_2= V_{pp2}C_{o2} + V_{pp1}C_x$ will be pumped in C_{int}. Also this charge is removed by integration of $I_{int.}$ A similar procedure happens in the four phases (Ph3 to Ph6). However, to obtain the advantages of advanced chopping [3], the directions of voltages and currents is reversed. In the seventh and eighth phase (Ph7 to Ph8), the signals are equal to those in the first two phases. When $V_{pp1} =V_{pp2}= V_{DD}$, then for one measurement period T_{msm}, is holds that:

$$T_{msm} = 4\frac{V_{DD}(C_x + C_{o1} + C_{o2})}{\hat{I}_{int}}, \qquad (1)$$

where, $\hat{I}_{int}$ represent the magnitude of I_{int}.

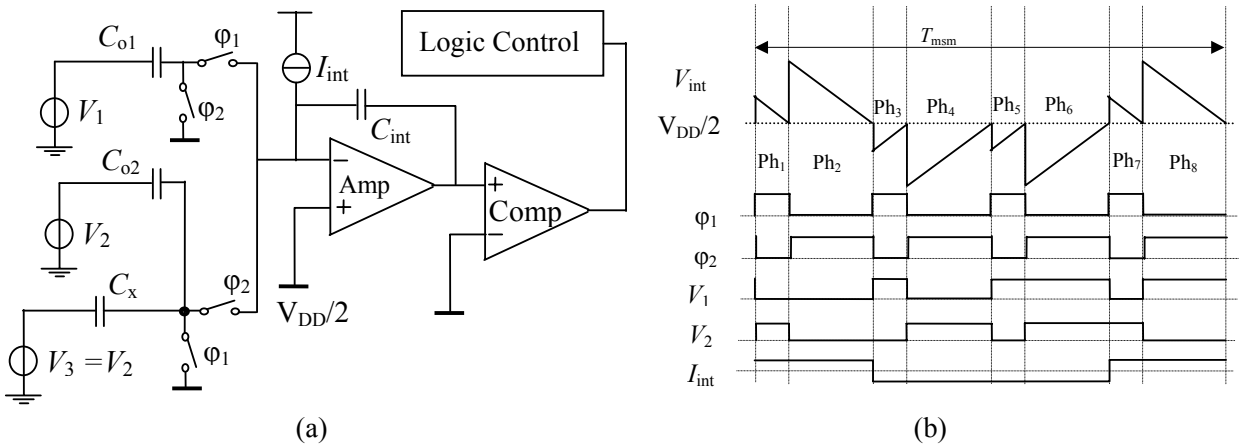

Fig. 1. Basic principle of the interface for capacitive-sensor; (a) circuit diagram, (b) some relevant signals.

So far, the interface has been optimized for the measurement of high-quality capacitive sensors in the range of tens of pF. Now we will show, that, by changing the sensor driving voltage V_3 for its common-mode level [2], we can use this circuit for leaky capacitive sensors too.

Our design goal is to make this front-end a part of a universal transducer interface [3]. Therefore, the front end should be compatible with front-ends for other sensors. For this reason, we designed the circuit of figure 1 as a Voltage to Period Converter ($V_3 = V_x$ and $C_x = C_s$).

3. CAPACITANCE-TO-VOLTAGE CONVERTER

Figure 2 shows the capacitor-to-voltage converter (CVC) with some related signals. The capacitors C_{off} and C_{ref} are external capacitors, the resistor R_x represents the leakage resistance of a leaky capacitive sensor C_x. The other components are implemented inside the chip. The pins of the chip are named A, B, C and D.

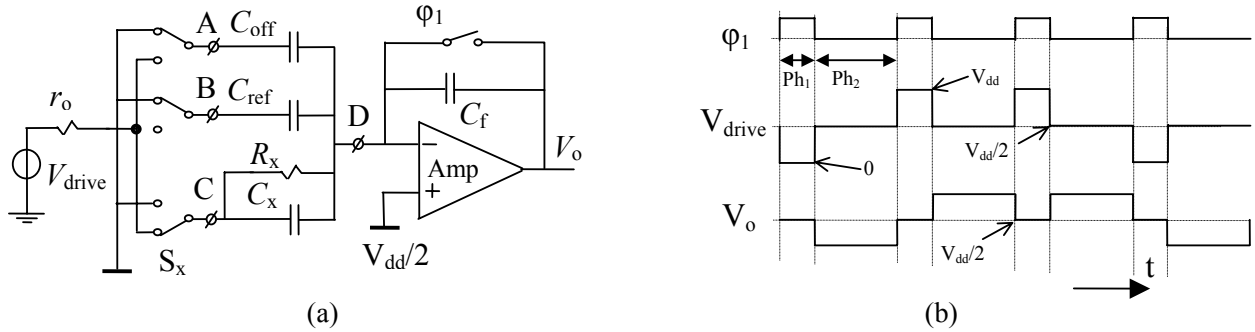

Fig. 2: A Capacitor-to-voltage converter (CVC) for leaky capacitive sensor (a) and related signals (b).

In phase 1, when φ_1 is high, the selected capacitor will be charged to V_{dd}. In phase 2 the charge of $C_{in}V_{dd}/2$ will be pumped to C_f and cause the voltage jump of $C_{in}V_{dd}/2C_f$ at the output voltage V_o. Where, C_{in} is one of the three input capacitances. Even in case that the amplifier (Fig. 2) has a rail-to-rail output, to prevent saturation of the amplifier, it should hold that $C_f \geq C_{in}$. However, C_{in} can be in the range of hundreds of pF, which would require a large area-consuming on-chip capacitor C_f, or and external component. As a better alternative, we prefer to sacrifice some resolution and to decrease the amplitude of the driving voltage with a factor of, for instance 10. In the case of humidity sensors, this voltage reduction will also increase the sensors lifetime.

4. NON-IDEALITIES IN CVC

There are several non-idealities in the CVC circuit to be considered in this paragraph:

4.1. ON Resistance of switches and output resistance of the driving source

When ignoring R_x, the only limitation for the switch ON resistance will be due to the required charge-transfer speed. To achieve the certain level of accuracy, the charge-transfer time-constant, should be small enough. However, the presence of R_x will also introduce a steady-state error. As mentioned in the previous section, in phase 1, the selected capacitor is supposed to be charged to V_{drive}. If the switches are ideal, the capacitor will be charged to a level determined by the driving signal, independent of R_x and the selected capacitor. However, due to an ON resistance $R_{on,x}$ of switch S_x, C_x cannot be fully charged, which causes inaccuracy. The relative error due to this effect amounts to:

$$\varepsilon_{R_{on}} = R_{on} / R_x \qquad (2)$$

It is clear that it will be easy to keep R_{on} small enough as compared to the leakage resistor to achieve enough accuracy. In addition to this static error of the switches, as we will discussed in section 4-3, R_{on} also causes a dynamic error. The output resistance of the driving source r_o, will affect the accuracy in the same way as R_{on} of switches.

4.2. Offset

It may seem that due to offset of CVC amplifier, and presence of shunt resistance, R_x, some part of pumped charge will be lost. However, the chopper can solve this problem. In phase 2, the current of V_{off}/R_x will flow through C_f, and cause a voltage increase of the output voltage (Fig. 3). Since the output voltage at the end of phase 2, will be sampled and causes an error. However, the effect of this error is compensated by the same error caused in phase 4. As a result, the value of $V_1 + V_2$, which is independent of the current V_{off}/R_x, will be converted to the period. Additionally, because this current is independent of the selected capacitor, any residual error will be removed by three-signal auto-calibration.

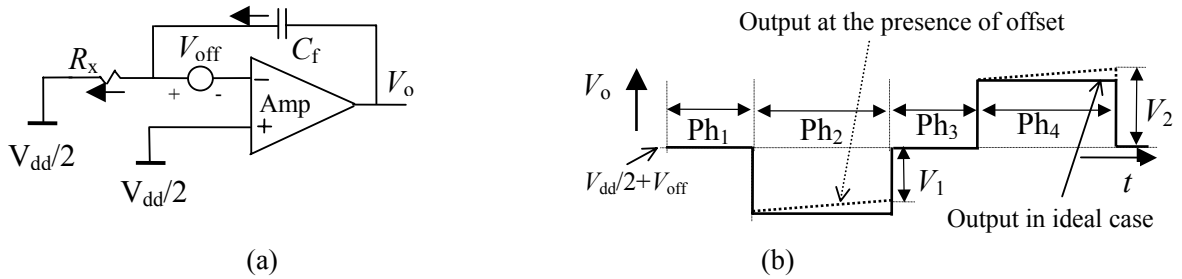

Fig. 3: The effect of the offset voltage on the accuracy of the CVC (a) Equivalent circuit for calculation of the effect; (b) the output voltage versus time.

4.3. Transients

Up to now, we supposed that the charge of input capacitors is transferred to C_f immediately and that during the charge-transfer phase, the voltage over R_x equals zero. In that case, no charge will be lost via R_x. However the charge-transfer time is finite and is determined by the high-frequency pole of the system. We can divide the charge loss due to transients into two parts. The first part is due to the transient voltage at the negative input of amplifier and the second part is due to the transients in the driving voltage. The first part is almost independent of the selected capacitor, and can be canceled out by three-signal auto-calibration. However the second part exists only when we select C_x and is a source of error. Analyzing this error is not simple however, to minimize this error; we should maximize the bandwidth of the amplifier and minimize both the switch resistance $R_{on,x}$ of switch S_x and the internal impedance of the driving-voltage source.

5. IMPLEMENTATION AND SIMULATION RESULT

Figure 4-a, shows the complete interface with implemented three-signal auto-calibration. The interface output signal is shown in figure 4-b. Because of the use of the three-signal auto-calibration technique, one measurement cycle consists of three phases: one to measure the offset capacitor C_{off}, one for the reference capacitor C_{ref}, and third one for the sensor capacitor C_x. The interface has been designed for implementation in 0.7 μm standard CMOS technology.

The different periods of the output signal, can be read with a micro-controller. For identification purposes, the time interval T_{off} is splitted into two short periods [3]. Data can be read via a serial port (RS232) and can be analyzed, for instance, with a Labview program.

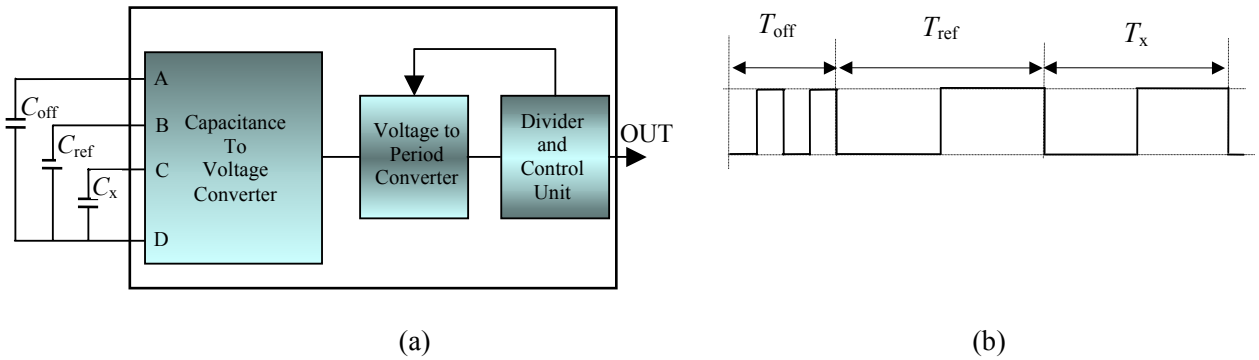

Fig. 4: The complete interface including three-signal auto-calibration (a) and the interface output signal.

We simulated the complete interface for $C_{o1} = C_{o2} = 1$ pF, $C_s = 15$ pF, $C_{int} = 10$ pF, $I_{int} = 0.7$ μA, $C_f = 100$ pF, $V_{pp1} = V_{pp2} = 5$ V and a peak-to-peak value V_{ppx} for the driving signal for C_x , $V_{ppx} = 0.25$V.

We suppose that our input signal is a humidity sensor with the sensitivity of 0.4 pF per percent of relative humidity (%RH) and its value can be in the range of 200 pF to 300 pF. Therefore we selected C_{off} =200 pF and C_{ref} =300 pF. Figure 5-a shows the corresponding error in the measured relative humidity for C_x=250 pF due to leakage resistance. As it can be seen the total error, static and dynamic, is proportional to reciprocal of the shunt resistance. Figure 5-b shows the error in relative humidity for a fixed value R_x=500 kΩ, as a function of the input capacitance C_x. As expected, increasing the value of the input capacitance will increase the dynamic error, which is due to the transient voltage across R_x.

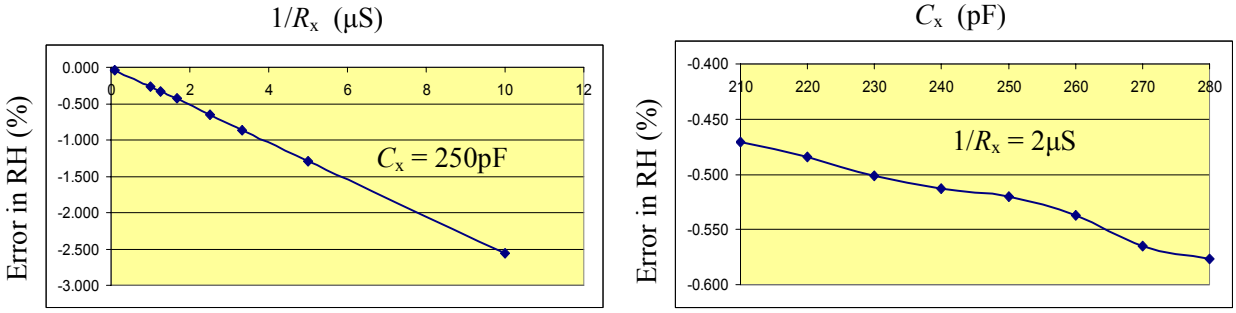

Fig. 5: Error in relative humidity (a) versus $1/R_x$ for C_x = 250 pF; (b) versus C_x for R_x = 500 kΩ.

6. CONCLUSIONS

A novel interface for leaky capacitive sensor has been designed. In order to minimize the effect of leakage, the front-end will keep the voltage across the sensor during charge transfer close to zero. To optimize the design, the non-idealities of the front-end are investigated. The interface has been implemented in 0.7μm standard CMOS technology. Simulation results show that we can measure humidity with a capacitive sensor at the presence of leakage resistor as small as 500 kΩ with less than 0.6% error in RH.

7. REFERENCES

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