IMPROVEMENT POSSIBILITIES OF THE DEVICE FOR MEASURING OF SMALL CAPACITIES

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The methods developed for decreasing the influence of parasitic capacitances of measuring capacitance converter with one grounded electrode and with very small capacitance and very small change of the capacitance enable increasing the sensitivity of the converters substantially.

Keywords: Capacitance converters, parasitic capacitances

1. INTRODUCTION

Measurement of capacitances in the range of (0.1 ÷10) pF is accompanied by the main difficulty, which caused by the effect of parasitic capacitances. In practice the three-terminal sensor has a grounded screen of its electrodes to protect it from external sources [1]. Parasitic capacitances between the capacitor terminals and the screen C_{s1} and C_{s2} as well as the parasitic capacitances C_p and C_p` of the measuring circuitry, into which the sensor is connected, are connected into electrodes of a measurement capacitance C_x. In many applications the parasitic capacitances are much bigger than the unknown capacity C_x.

To measure a very small capacitances accurately, stray-immune capacitance converter with high sensitivity and stability must be used.

Circuit solutions for capacitance measurement, which can provide compensation of the parasitic capacitances and the electrodes of the unknown capacitance C_x are ungrounded are known [2, 3, 4, 5, 6]. The methods for compensation used in them do not enable their application in circuit solutions for measurement of the capacity of converter with one grounded electrode.

A device for measuring of very small capacitances is developed, which is used in a converter with one grounded electrode [7]. The device consists of two converters – "capacitance – time interval" and "time interval – DC voltage". Applying the solution for compensating of the output voltage caused by the assembly parasitic capacitance between the terminals for integrating of the capacitance to be measured enables achievement of sufficient sensitivity (from a few *pF* to parts of *pF*), which is limited by the increased correlation between the parasitic capacitances and the measurement capacitance C_x.

The aim of this elaboration is to synthesize measuring converter with one grounded electrode and with decreased sensitivity for parasitic capacitances.

2. EXPOSITION

Two solutions *for* compensation of the parasitic capacitances to a great extent aiming the *increasing of the output relative sensitivity of capacitance converter* are suggested:

– connecting of the Voltage Negative Impedance Converter (VNIC) into the converter "capacitance – time interval";

- connecting of the second converter "capacitance – time interval" through a suitable logic.

2.1. Compensation of the parasitic capacitances by means of Voltage Negative Impedance Converter (VNIC)

2.1.1. Experimental treatment

VNIC, realized by DA2 (*fig.1*) with scheme analogous to that in [8] is connected to the developed device for measuring of small capacitances [7], which includes converter "capacitance – time interval", realized by DA1 and converter "time interval – DC voltage", realized by DA3. In *control point 1* starting impulses from software generator enter and in *control point 2* impulses with duration, which is proportional to the value of the unknown capacitance C_x are obtained. In *control point 3* DC voltage is obtained, which value is proportionally to the duty cycle of the impulses in *control point 2* and hence – to the value of the measured capasitance $\boldsymbol{C_x}$.

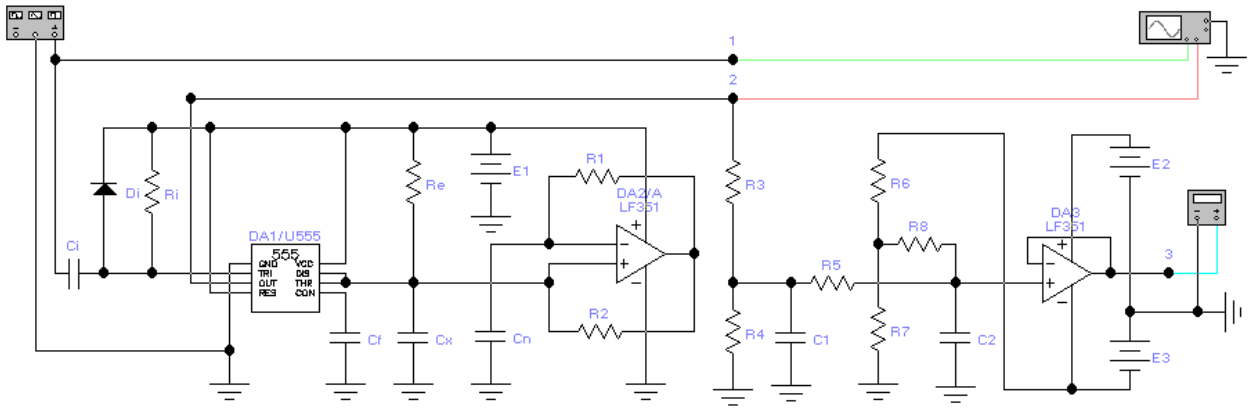


Fig.1. Converter "capacitance – DC voltage"
with beforehand transformation in period, by adding of the VNIC

The input capacity of VNIC is defined [8]:

$$C_i = -\frac{R_2}{R_1}.C_n . \tag{1}$$

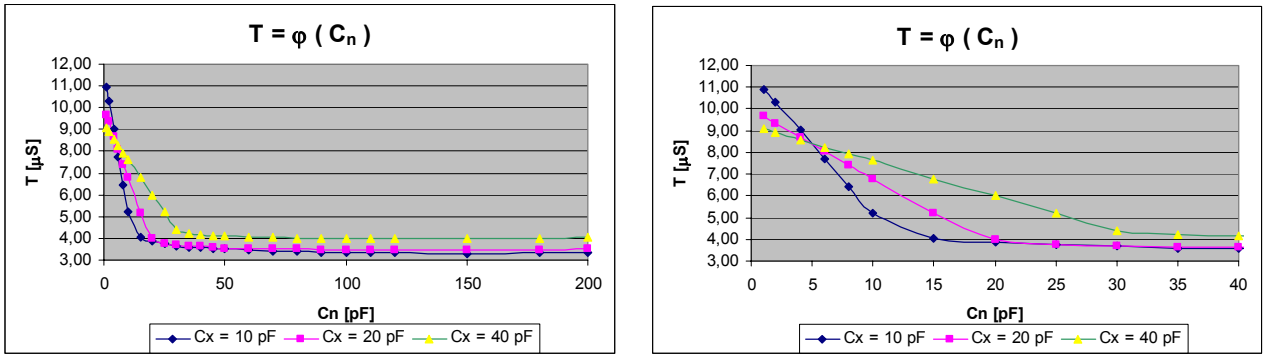
Connecting the input of VNIC in parallel to the unknown capacitance C_x in the circuit of the converter "capacitance – time interval" enables decreasing the influence of parasitic capacity – the duration of the output impulse T [9] is:

$$T = 1{,}1.R_e.C_{eq} = 1{,}1.R_e.(C_x + C_i) = 1{,}1.R_e.\left(C_x - \frac{R_2}{R_1}.C_n\right) \tag{2}$$

Where:
$\boldsymbol{R_e}$ – value of the reference resistor;
$\boldsymbol{C_x}$ - value of the measured capacitor;
R_1, R_2 – values of the resistors in VNIC's circuit;
$\boldsymbol{C_n}$ – value of the capacitor in VNIC's circuit;
$\boldsymbol{C_{eq}} = C_i + C_x$ – equivalent capacity, determining the durations of output impulses.

2.1.2. Results from the experiments

The experiments are done by simulation with the program product *Electronics Workbench 5.12*. In the paper only the results from the investigation of the influence of the capacitance variation C_n by VNIC, which is conected to the converter, on the duration T of the output impulses are presented. In *fig.2a* the dependences with values of the resistors $R_1 = R_2 = 15$ kΩ, values of the measured capacitance $C_x = 10$pF, 20pF, 40pF, and of the reference resistor $R_e = 909.2$ kΩ; 454.6 kΩ and 227.3 kΩ for the threevalues of C_x respectively are shown. In *fig.2b* the initial sections of these dependancies are shown.



a) b)

Fig.2. Dependences $T = \varphi\ (Cn)$, for $C_x = 10$ pF, 20 pF, 40 pF

Conclusions:

1. Adding of the VNIC to the converter "capacitance – time interval" decreases the equivalent capacity C_{eq} to a considerable degree (from 2 to 3 times) and the bigger change is at the lower values of $\boldsymbol{C_x}$.

2. The dependance for the duration of the output impulses T on the capacitance $\boldsymbol{C_n}$ corresponds to that of equation (1) – it decreases comparatively according to a linear law when the capacitance of VNIC increase till a certain value of $\boldsymbol{C_n}$ (about 80% of the value of the capasitance $\boldsymbol{C_x}$). At further increasing of the value of $\boldsymbol{C_n}$ the time interval T changes to a comparatively small extent.

2.2. Compensation of the parasitic capacitances by connecting of *second converter "capacitance – time interval"* by means of suitable logic

2.2.1. Experimental treatment

The investigated circuit solution (*fig.3*) consists of basic converter "capacitance – time interval", which is realized by timer *UA1* [7] and additional converter "capacitance – time interval", which is realized by timer *UA2* as well as additional logic circuit, which is realized by *UD1*. The work principle is given by time-diagrams, which are shown in *fig.4a* and *fig.4b*.

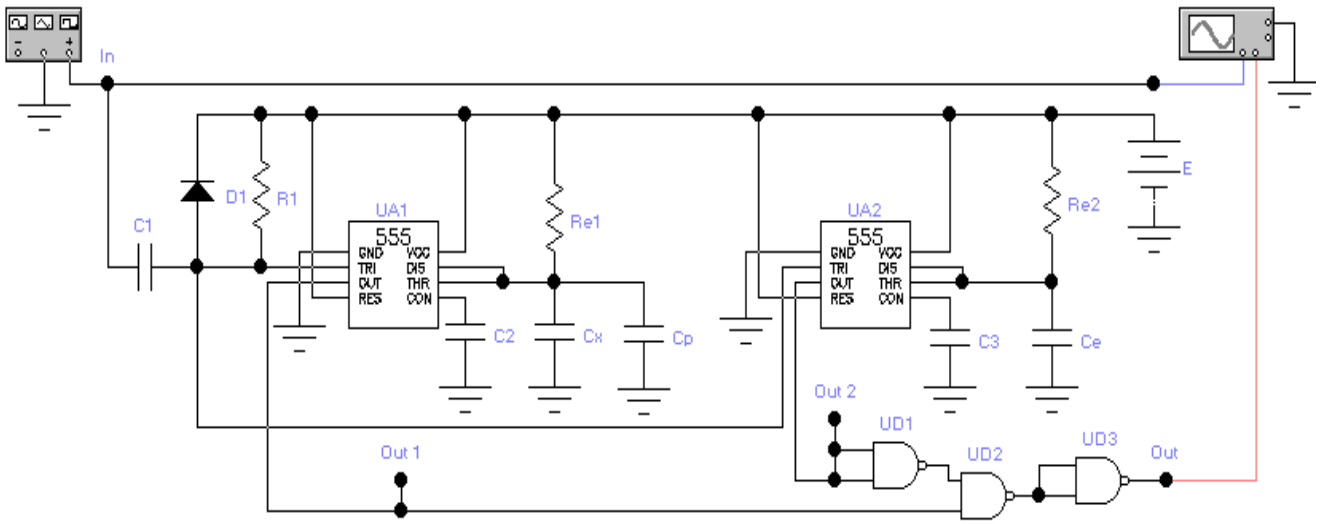
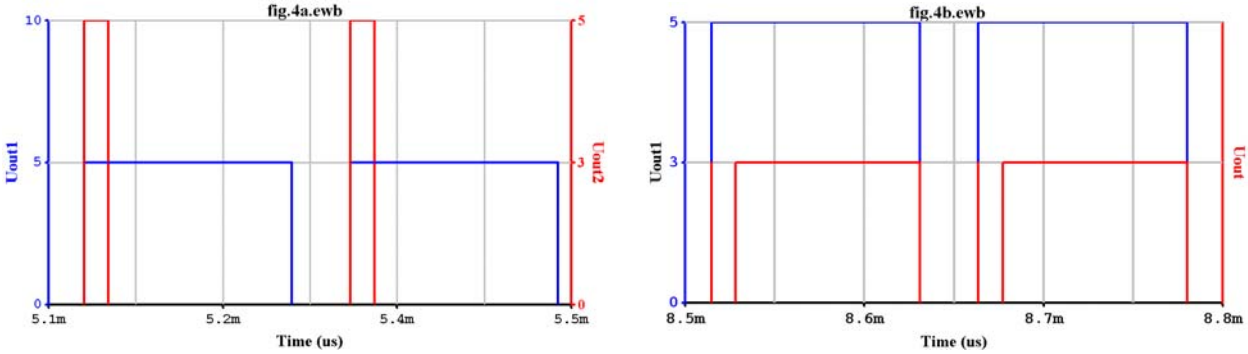


Fig.3. Compensation of the parasitic capacity C_p by second timer, it is connected into the basic timer with a logic circuit



a) U_{out1} , U_{out2} *b)* U_{out1} , U_{out}

Fig.4. Signals in the control points

The parasitic capacity between terminals for connection of the measured capacity C_x is presented by the capacitor C_p. A capacitor C_e with capacity, which is the same as the capacity of the capacitor C_p is connected to the additional timer. The output impulses of both timers have duration respectively:

$$T_{Out1} = 1{,}1.R_{e1}.(C_x + C_p) \quad (3)$$

$$T_{Out2} = 1{,}1.R_{e2}.C_e = 1{,}1.R_{e2}.C_p \quad (4)$$

At the output of the logic circuit obtained impulses with duration, this is defined by the difference in the durations of the impulses of both timers:

$$T_{Out} = T_{Out1} - T_{Out2} \quad (5)$$

When $R_{e1} = R_{e2} = R_e$:

$$T_{Out} = 1{,}1.R_e.C_x \equiv C_x \quad (6)$$

2.2.2. Results from the experiments

The results from the experiments with the converter's non-linearity $\delta_{Tout} = \varphi(C_x)$ for 2 ranges on a change of the measurement capacity C_x (200pF and 20pF) when assembly capacitances C_p=C_e=15 pF (near to the real assembly capaci-

tances) carried out with the help of the program product *Electronics Workbench 5.12* are graphically shown in *fig.5*.

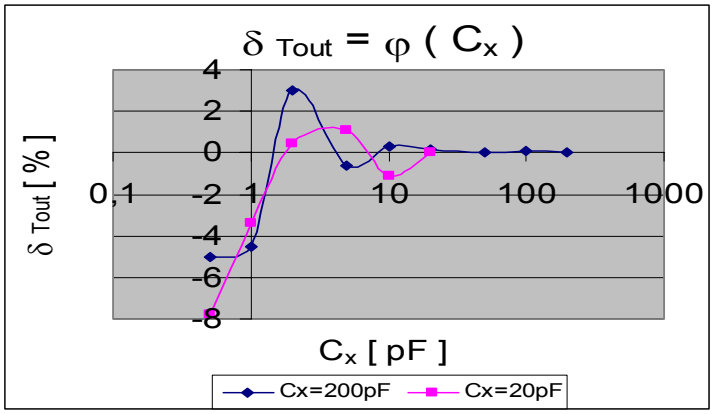


Fig.5. Dependences $\delta_{Tout} = \varphi (C_x)$

Conclusion: The investigated circuit solution provides good linearity of transformation of the measured capacity C_x to time-interval – the relative error is $\delta_{Tout} \leq 1$ % for values of C_x, which are of the order of the parasitic capacity C_p, and error below 4 % for values of $C_x = 0{,}1.C_p$.

3. CONCLUSION

The developed methods and circuit decisions for capacitance measurements relevant to them enable synthesizing measuring converter with one grounded electrode; *it enables increasing the sensitivity of the transducers to a considerable extent*.

The first method, which uses the equivalent negative capacity of VNIC enables decreasing of the assembly parasitic capacitances several times due to the decreasing of the correlation between the value of the measured capacity and this one of the parasitic capacitances.

The second method, which permits to measurement of capacitances that are considerable less than assembly capacitances is developed for entire compensation of the parasitic capacitances. In this way the sensitivity of the capacity converter is increased considerably (over 1 order). In combination with the additional compensation of the DC voltage, which is submitted in [7], it enables accurately measurement of capacitances, which are 2 orders less than the parasitic capacitances.

The developed capacity converter can be used as measuring converter with sensitivity below tenth from pF and with very low instability.

4. REFERENCES

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