# RESONANT DRIVER CIRCUIT FOR MOSFET'S AND IGBT CONTROL IN CLASS-DE INVERTER

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*The paper presents the application of a driver circuit for MOSFET's and IGBT control in quasi-resonance ZVS class-DE inverter for induction melting. It justifies the use of this type of circuits in induction heating. The requirements to the inverter control have been defined and a suitable circuit-"resonance driving" has been proposed. The behavior of the resonance driver has been studied at different operating frequencies and loads, and the experimental results have been presented.*

**Keywords:** Gate drive, high frequency, resonant gate drive.

## 1. INTRODUCTION

The ZVS class-DE inverter for induction melting can be seen in fig.1. For reasonable performance in a Class-DE inverter, the switching devices should be capable of a switching in less than approximately 5% of the period (for conduction angles is the region of 80º-150º). If the MOSFETs are to switch in less than 5% of the period at 0,4 MHz, then their total time to switch on or off should be less than 100ns. Hence the MOSFET gate must be charged / discharged in less than 100ns.

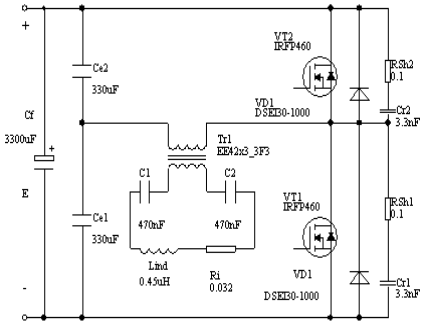



Fig.1

The effective gate capacitance or input capacitance, Ciss, of MOSFET can be comprised of the gate-source capacitance and the gate-drain capacitance (or Miller capacitance) [1]. The total gate charge, Qg, required to charge the gate of an IRFP450 MOSFET from 0 V to 12 V is 120 nC. This total charge includes the (Miller) charge required to discharge the gate-drain capacitance when the MOSFET switches from the off-state, with a $V_{DS}$ of 300 V, to the on state. If this entire charge is to be delivered in 10ns then the gate-driver must supply an average current of Ig = 120nC/10ns = 12 A.

The loops around which the current will flow when charging and discharging the gate capacitance can be seen in Figure 2. The current required to charge/discharge the gate capacitance must increase in a few nanoseconds from zero to maximum of 12 Amps or more. If the rate of current rise is to be in the order of 4A/ns, then an inductance of 1nH in the charging/discharging loop will cause a 4V voltage drop across it, reducing the drive voltage available and slowing the rate of rise of the current [2,3,4]. It can be seen, therefore, that it is imperative to keep the inductance of the gate charging and discharging loop to a minimum. The source-lead inductance is

part of the gate charging and discharging loop and in addition it has an induced voltage across it due the changing drain current which further reduces the gate-drive voltage available. Thus the source-lead inductance adversely effects the switching times and so it is desirable to keep it to an absolute minimum [3]. The gate-driver must source and sink in excess of 12A and should have as low output impedance as possible to prevent spurious turn on with high $dV_{DS}$ /dt. The gate-driver must be able to dissipate in excess of 7 W. The charging and discharging loop must have the least inductance possible and its supply rails should be very well decoupled.

## 2. PROBLEM STATEMENT

### 2.1. The driver schematic.

There are two practical choices for driving the gate capacitance with a square wave at a MHz range. The first uses a gate-driver coupled to the gate through a transformer. The transformer is used to provide galvanic isolation and the level shifting required for the high–side switch. The disadvantage is that transformers inherently have leakage inductance's and coupling capacitance's associated with their construction. The leakage inductance of the windings makes it very difficult to obtain the rapid rise of current required and will cause excessive ringing. The coupling capacitance's limit the dv/dt and noise immunity of the transformer. In a resonant circuit topology, the energy stored in the gate capacitance is resonated to an inductance and back again and hence much less power is dissipated than in a hard-switched system. The disadvantages of a resonant circuit topology are that it is a single frequency system and only a limited adjustment of the dead-time is possible. For the above reasons, a transformer-coupled gate drive was considered not to be the best solution for this application. The second way of driving the gate capacitance is to drive the gate directly with a gate-driver. This method will have the lowest loop inductance's, provided the physical layout is designed correctly, and thus will have the fastest charge and discharge times.

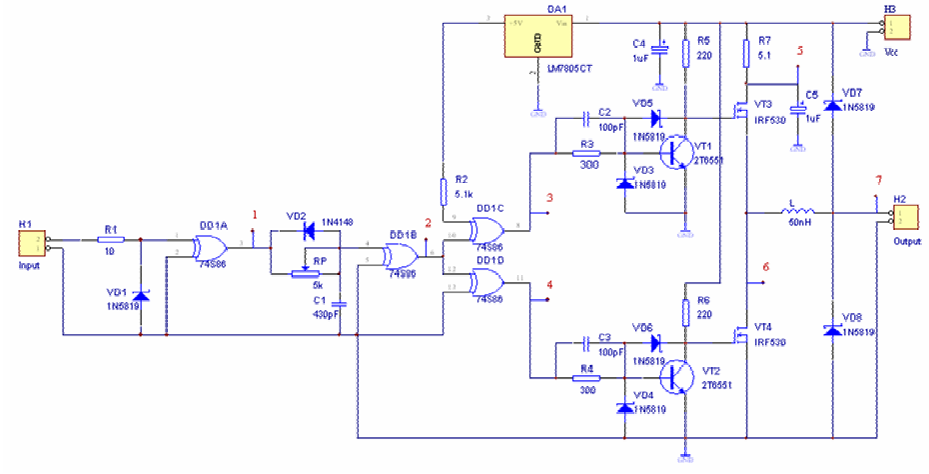



Fig.2

The topology of the studied gate driver power supply is provided on Fig. 2. Incorporating the gate-driver directly onto the same die as the power MOSFET enables the lowest loop inductances to be achieved and hence the fastest rise and fall

times. The next best solution is to mount the gate-driver directly from the gate to the source and design the charging and discharging loop with the minimum leakage inductance. This was the approach that was followed for this inverter. Input parameters for mathematical calculation are: switching frequency fs; Gate capacitance $C_G$; Times tr and tf; Rtotal= Rdri=0.18Ω.

The driver circuit is supply by 2 voltage: +15V for amplifiers bipolar transistors and output MOSFETs buffer and +5V for TTL IC 74S86.

In circuit's input is RD snubber for ESD protection with resistor value 10 Ω and fast-switching diode HER106.

Between the first and the second semi-summator is diode D2-1N4148 and elements RP and C1. The time constant for this chain is 2,15 μs.

The resistors values of R3 and R4 is determine from:

$$R3 = R4 \geq \frac{U_{0H}}{I_{0MAX}} \quad (1)$$

The fast diodes D3÷D6 protect transistors Q1 and Q2 from base overvoltage spikes. The capacitors is C4 and C5 capacitive filters. The transistors Q1 and Q2 is bipolar 2T6551 with parameters:

$U_{CER\max} = 50V$ , $I_{C\max} = 0{,}5A$ , $P_{C\max} = 0{,}8W$ , $h_{21E\min} = 26$ , $f_T = 300MHz$ .

The resistors R5 and R6 is determinate from:

$$P_{CE} = 0{,}625P_{C\max}\,;\, I = \frac{P_{CE}}{U_{CC}.k_{PWM}}\,;\, R5 = R6 = \frac{U_{CC}}{I} \quad (2)$$

The transistors Q3 and Q4 is MOSFET - IRF730 with parameters: $U_{DS} = 400V$ , $I_D = 5{,}5A$ , $U_{GS} = \pm 20V$ , $P_D = 75W$ , $r_{DS(ON)} = 1\Omega$ .

The resistor value for R7 is determined from: $R7 = (U_{CC}/I_D) - r_{DS(ON)}$ (3)

**2.2.Theoretical calculations.**

For switching control of the power MOSFET or IGBT at switching frequency f:

- output power for gate control;

$P = Q_{GS}.U_{DD}.f$

- peack current $I_{PEAK}$ is $I_{PEAK} = U_{DD} \times \sqrt{\frac{C_{GS}}{L_R}}$ (4)

- Time for rising $t_r = \frac{\pi}{2} \times \sqrt{L_R \cdot C_{GS}}$ (5)

- Time for recovery is $t_{rec} = \sqrt{L_R \cdot C_{GS}}$ (6)

- the characteristic impedance is $Z_0 = \sqrt{\frac{L}{C_{GS}}}$ (7)

- the power losses in $R_G$ is $P_{LOSS\_RG} = \frac{R_G}{(R_G + Z_O)} \cdot Q_{GS} \cdot U_{DD} \cdot F_S$ (8)

- the power losses in diodes is $P_{LOSS\_VF} = \frac{U_{F1}}{U_{DD} + U_{F1}} \cdot \left( \frac{Z_0}{Z_0 + R_G} \cdot Q_{GS} \cdot U_{DD} \cdot f \right)$ (9)

- for output efficiency is $\eta_{ST} = \frac{Z_0}{Z_0 + R_G}$ (10)

- for recovery efficiency is $\eta_{rec} = \frac{U_{DD}}{U_{DD} + U_{F1}}$ (11)

- for total efficiency $\eta = \eta_{ST} . \eta_{rec}$ (12)

Output results from calculation are generalized in table 1.

Table1

| L, nH | Ip, A | Vp+,V | Vp- | P, W | Q, W |
|---|---|---|---|---|---|
| 2.15 | 13,57 | 17.26 | 12.26 | 0.96 | 4.5 |

Output characteristic is presented in tabl.2 and fig.3.

Table2

| $C_{GS}$, nF | 2,2 | 4,2 | 7,5 | 21 |
|---|---|---|---|---|
| P, W | 0,86 | 0,86 | 1,79 | 9,9 |

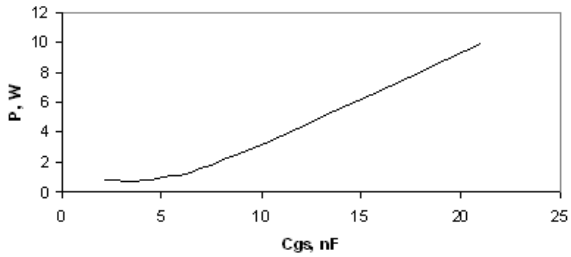



Fig.3

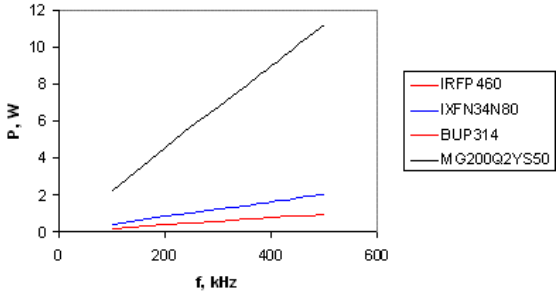



Fig.4

The theoretical frequency characteristic is presented in tabl.3 and fig.4.

Table3

| f, kHz | 100 | 200 | 300 | 400 | 441 | 500 |
|---|---|---|---|---|---|---|
| $P_{IRFP450}$, W | 0,195 | 0,39 | 0,585 | 0,78 | 0,86 | 0,975 |
| $P_{IXFN34N80}$, W | 0,405 | 0,81 | 1,215 | 1,62 | 1,79 | 2,025 |
| $P_{BUP314}$, W | 0,195 | 0,39 | 0,585 | 0,78 | 0,86 | 0,975 |
| $P_{MG200Q2YS50}$, W | 2,25 | 4,5 | 6,75 | 9 | 9,9 | 11,25 |

## 3. EXPERIMENTAL RESULTS

### 3.1. P-Spice simulation of the resonant driver operating with MOSFET.

The simulate circuits is shown in fig.5. In table 4 are shown parameters values for circuits and in fig.6 simulated waveforms.

Table4

| f, kHz | $K_f$ | P,µw | $I_{min}$,A | $I_{max}$,A | $U_{Gsmax}$, V | $t_{on}$,ns | $t_{off}$, ns | $P_{drv}$,W |
|---|---|---|---|---|---|---|---|---|
| 100 | 0,5 | 5 | 2.56 | 9.5 | 12 | 485 | 237 | 7,11 |
| 200 | 0,5 | 2,5 | 2.43 | 9.61 | 12 | 486 | 251 | 7,18 |
| 300 | 0,5 | 1,67 | 2.57 | 9.38 | 12 | 466 | 254 | 7,18 |
| 400 | 0,5 | 1,25 | 2.44 | 9.55 | 12 | 476 | 248 | 7,22 |

In fig.7 is shown current and voltage waveforms for driver's output with load transistor IXFN34N80 and in table 5 are shown parameters values for circuits.

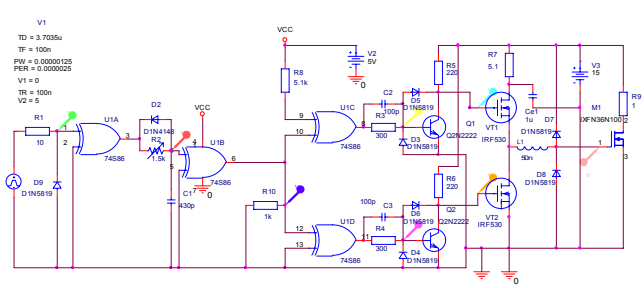


Fig.5

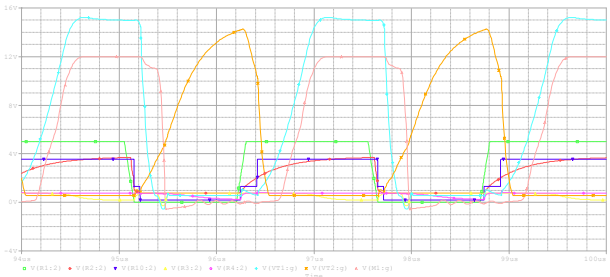


Fig.6

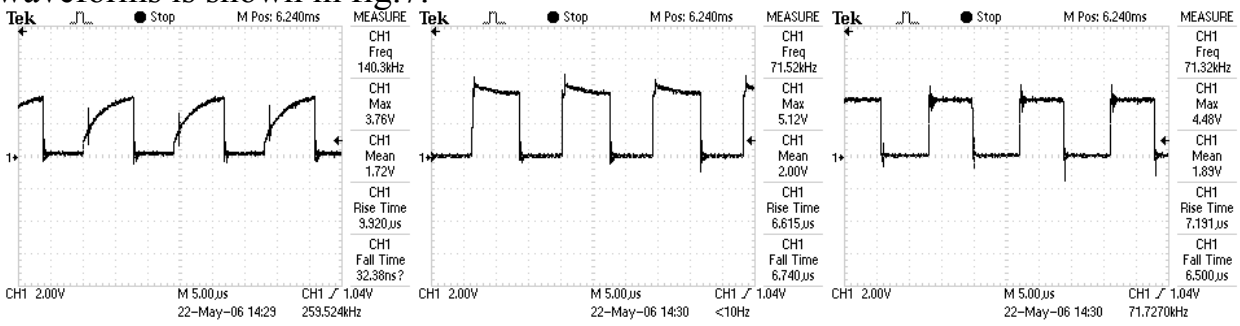
Table5

| f, kHz | $K_f$ | P, μW | $I_{min}$, mA | $I_{max}$, A | $U_{Gsmax}$, V | $t_{on}$, ns | $t_{off}$, ns | $P_{drv}$, W |
|---|---|---|---|---|---|---|---|---|
| 100 | 0,5 | 5 | 398 | 1,35 | 12 | 673 | 253 | 1,48 |
| 200 | 0,5 | 2,5 | 392 | 1,37 | 12 | 563 | 246 | 1,53 |
| 300 | 0,5 | 1,67 | 390 | 1,37 | 12 | 645 | 257 | 0,42 |

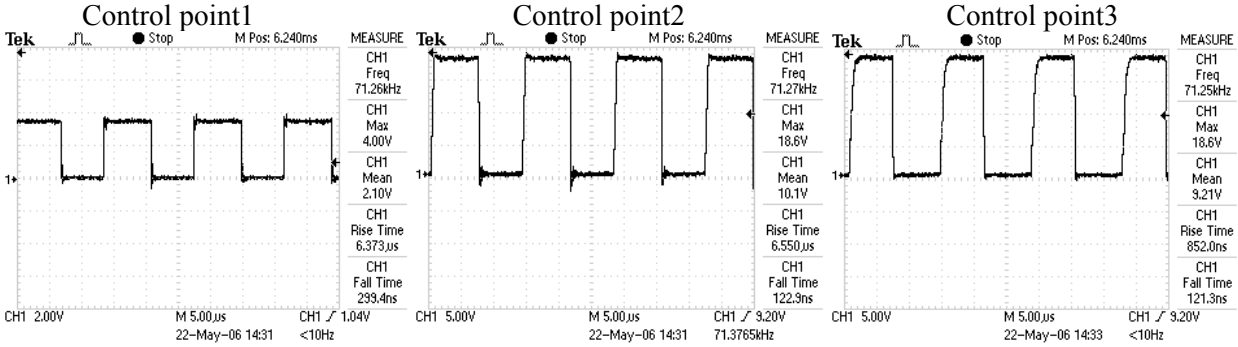
The driver's operation is simulated and with IGBT load transistor BUP314.

### 3.1. Experimental results of the resonant driver.

The practical driver's circuit is investigated in separated control points 1-6, shown in fig.2, at $f = const$ and determinate load transistor. The experimental waveforms is shown in fig.7.




Control point1 Control point2 Control point3




Control point4 Control point5 Control point6

Fig.7

The output gate waveforms with a load transistor IRFP450 for operation frequency f=100kHz and f=400kHz, is shown in fig7 and fig.8. At operation frequency 100 kHz, the rise time for driver's output voltage $U_{GS}$ is 420 ns and the fall time is 158 ns. For fig.8 at 400 kHz, the rise time is 348 ns and the fall time is 148 ns.

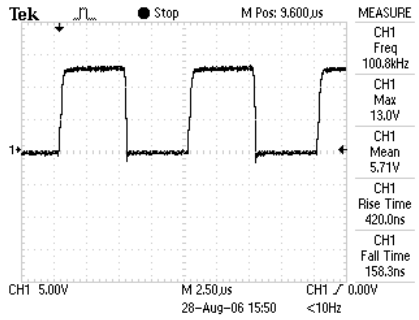



Fig.8

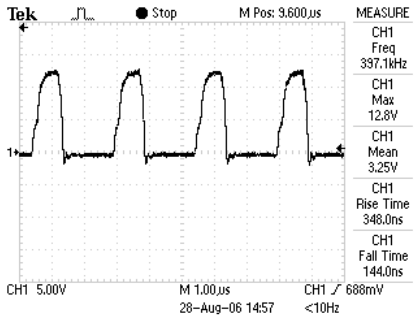



Fig.9

From these experimental results, it may observe that switching times are independent for frequency rise.

The experimental output load and frequency driver's characteristic are present in fig.10 and 11.

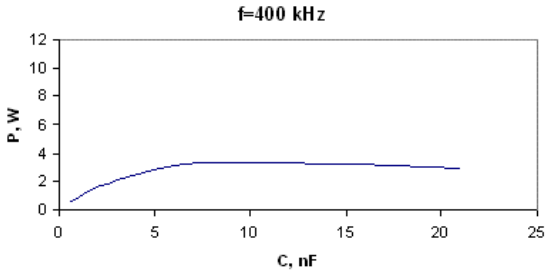



Fig.10

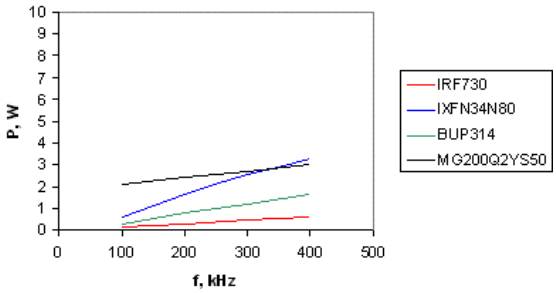



Fig.11

The obtained characteristic is relevant with theoretical characteristic shown in fig.3 and 4. The differences are better output power for MOSFET's IRFP450 and IXFN34N80 at high frequency and low input capacity, but for IGBT's BUP314 and MG200Q2YS50 control is better at low frequency.

## 4. CONCLUSIONS

The resonant driver described in this paper proves to be effective and advantageous gate control circuit for insulated gate transistors. The switching losses are decreased. The resonant driver is not sensitive to the values of gate capacitance changes and switching frequency.

## 5. REFERENCES

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