# DYNAMIC NON-OVERLAP COMMUTATION CONTROL IN SWITCHING REGULATORS

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*This paper discusses one easy accessible method for improved control in some topologies of switching regulators, inverters and other. It is based on adaptive feedback adjusted dead-time commutation strategy. Some preferences and disadvantages of synchronous switching is shown. A comparison of different topologies, based on efficiency and switching losses, is given. Test circuit and experimental results of dynamic non-overlap control with adaptive feedback are presented at the end of paper.*

**Keywords:** synchronous switching, commutation control, adaptive feedback

## 1.INTRODUTION

In present of industrial electronics many application has devices for power supplies, inductor motor drives, energy conversion and other. In most cases they use a switchmode power converters in different circuit topologies- buck, boost, half-bridge an so on. Common part of them is use of power MOSFET or IGBT transistors in switching mode of operation. That prove high efficiency, low power losses, small or no cooling elements.

Some basic topologies of switching regulators, their principles of operation and control, are presented in this report. Comparison of their efficiency is shown. Major of reasons for power losses and poor characteristics of conversion, ways of their calculations and improvement are given in the text. Authors propose solution for better performance of switching regulators in terms to avoid some of their main disadvantages-active power losses in switching elements, low quality waveforms caused by large transient time of commutation. Active control with adaptive feedback for adjusting turn-off and turn-on point of power switches is presented below, with test circuit and experimental results.

## 2. SYNCHRONOUS SWITCHING REGULATORS-OVERVIEW AND APPLICATION

Fig. 1 shows modification of DC-DC buck regulator, which is very adopted in practical applications. In this case the diode D1 originally is replaced by second power MOSFET Q2.This is a way to improve characteristics of converter circuit.

In regular DC-DC buck regulator D1 is open by voltage and current direction in Q1 turn-off period. Diode forward drop voltage causes active power losses, which are:

(1)

where $V_D$ is diode forward voltage drop, $I_o$ -diode forward current D-duty cycle.

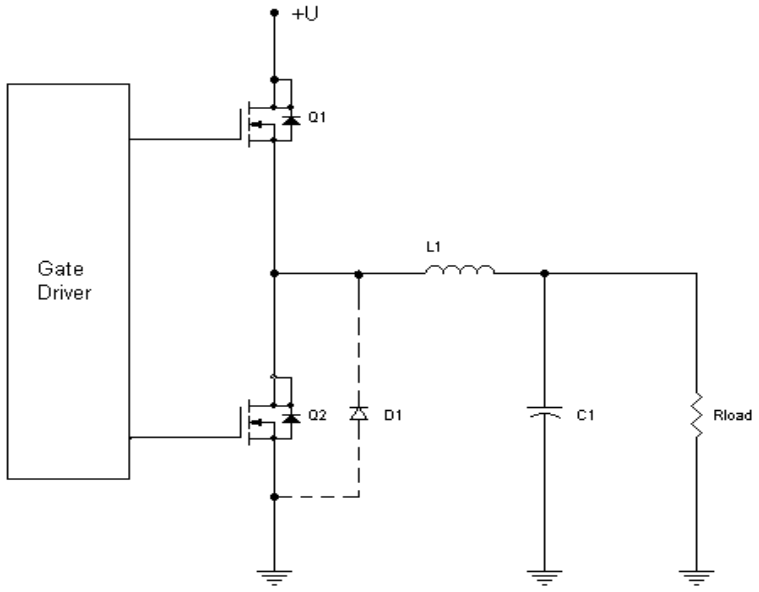


Fig.1

If D1 is replaced by Q2 power losses can be reduced. Calculation is made by next equation (Eq.2):

$$P_{Q2} = I_o^2 \cdot R_{DSON} \cdot (1 - D) \quad (2)$$

This equation shows that power losses depends on active resistance of elements and duty cycle. Active power dissipation is unacceptable in low duty factor and large load current applications. Advantages of using second MOSFET Q2 is easy to explain by next example: in PC power supply with input voltage 5V,output voltage 3,3 V load current 10A and duty cycle 66% current flow through diode D1 for 34% of all time. For normal diode with forward voltage drop 0,7V power losses are 2,38W.For proper chosen MOSFET transistor with $R_{DS(ON)}$=0,015ohms they will be only 0,51W [6]. Except the improvements of using second MOSFET there are problems and disadvantages. Not only a bigger price, but a more complex commutation circuits needed, are some of them. In practical implementation turn-off and turn-on periods of both transistors are related to minimum time needed for avoiding short circuit (dead-time) [1].

### 3.SYNCHRONOUS REGULATORS – PRINCIPLES AND DRIVE CIRCUITS

Very important rule in synchronous regulators is proper coordination of switching sequence for both transistors Q1 and Q2.Minimum time, needed for full turn-off and reactive power dissipation and prepare for next cycle of operation, is called "dead-time". In dead-time period both transistors are closed.

DC-DC synchronous buck regulator uses 2 MOSFETs called Q1(High-side) and Q2 (Low-side) and drivers, called the same way.

Switching losses is defined as:

- losses in Q1(High-side)
- losses in Q2(Low-side)

- conduction losses(Dead-time)

Losses in Q1 are:

$$P_{MOSFET} = P_{SW} + P_{COND}$$

$$P_{COND} = I_{OUT}^2 \bullet R_{DS(ON)} \bullet \frac{V_{OUT}}{V_{IN}} \qquad (3)$$

$$P_{SW} = \left(\frac{V_{IN} \bullet I_{OUT}}{2}\right)(F_{SW})$$

where $P_{COND}$ are conduction losses, $P_{SW}$-switching losses $I_{OUT}$ –output current, $V_{IN}$ and $V_{OUT}$-input and output voltage. $R_{DS(ON)}$-active resistance Q1,$F_{SW}$-switcing frequency.

Losses in Q2 are:

$$P_{COND} = (1-D)\,X\,I_{OUT}^2\,X\,R_{DS(ON)}$$

$$P_{SW} = \left(\frac{V_F + I_{OUT} \bullet 1.1 \bullet R_{DS(ON)}}{2}\right) I_{OUT} \bullet F_{sw} \qquad (4)$$

Conduction losses, caused by reverse diode conduction and recovery are:

$$P_{DIODE} = t_{DEADTIME} \bullet F_{SW} \bullet V_F \bullet I_{OUT} \qquad (5)$$

where $V_F$ is diode forward drop voltage[3].

Analyzing above equations, a conclusion is follows: with proper setting of dead time can be decreased total power losses in switching converter without any stability problems and element overloads.

Dead-time has minimal value for each application. Decreasing dead-time period may cause short circuit-both transistors are open at the same time. This current, also called "shoot through current", increase rapidly and may damage the MOSFETs. To avoid this situation many drivers work with fixed dead-time. Large dead-time is also negative situation, affects output voltage, cause harmonic distortion and it's not recommended for inductive loads, Proposed driver circuit have adaptive feedback, which monitors the state of power MOSFETs. In this way the driver holds a dynamic compensation of dead-time to avoid short circuit and the same time to keep it small enough ,do not affects output waveforms. This driver with adaptive principle of commutation have applications in DC-DC converters, inverters ant other devices with fixed commutation, which have two or more switching elements in synchronous sequence of operation. There is no need of extra reactive elements, like in other application with semi-soft and soft commutation.

## 4.Driver Circuit with Adaptive Feedback-Operation and Experimental Results

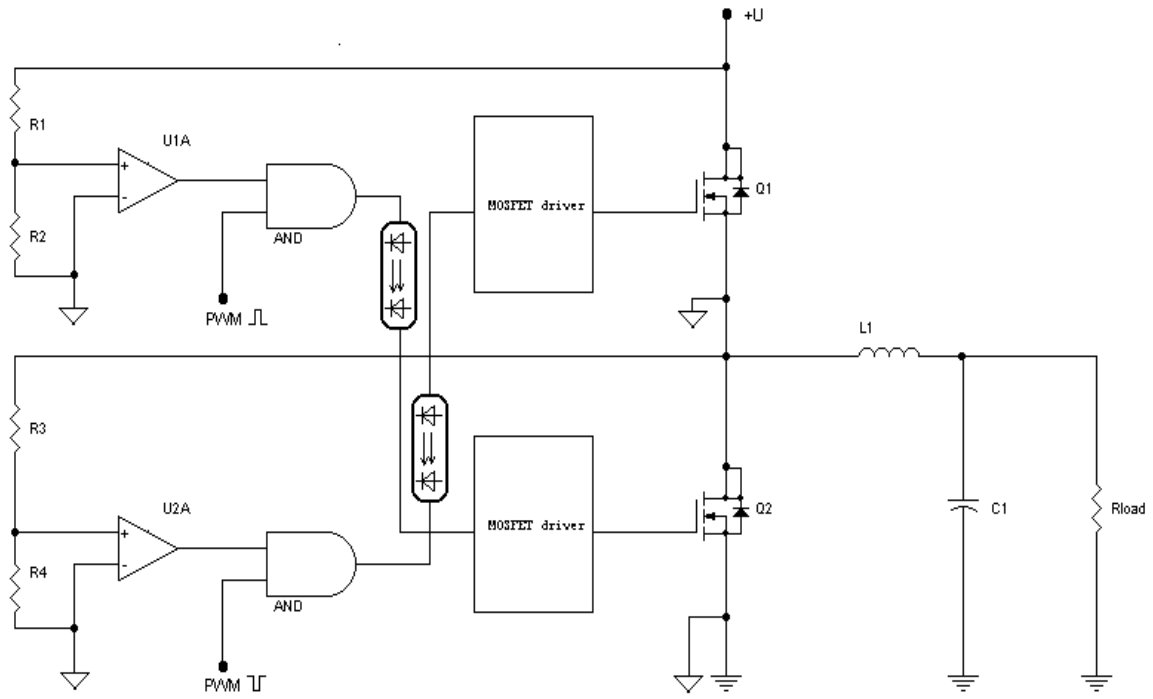


Fig.2

In shown circuit adaptive feedback monitors voltage $V_{DS}$ of each transistor. When it is fully turned-off, voltage drop across the drain-source rise high. Comparator U1A output rises at "high" logic level also, and this logic "1" goes to one of the inputs ot "AND" Other input has PWM-signal from oscillator. With valid input combination of "1" for both of inputs, output cross to high level and switch on the gate driver of other transistor. In this case we have cross-driving circuit: feedback of MOSFETs drive each other.

That allows to regulate in every moment dead-time between both switches with proper value, avoiding short circuit and same time do not affects waveforms with unwanted harmonics. In practical realization must be kept in mind delay in feedback, caused by delays of used elements. Feedback delay increase dead-time and indirect decline efficiency of all circuit. Using of optocouples is ordered by requirement of proper dielectric isolation between low-voltage driver circuit and high-voltage power stage. At once some of special features of optocoupler 6N137 are used.

The experimental results of driver circuit with adaptive feedback are tested with DC-DC synchronous buck regulator, implemented by presented circuit and with next characteristics:

- input voltage-U=30V
- duty cycle-D=0,5
- switching frequency-Fsw=20KHz
- MOSFETs-IRF630 200V 9A

Values of $R_{LOAD}$ and L1 are changed through the time of experiment, to demonstrate changes of dead-time, depending of output current and reactive elements, which store reactive power. Dead-time setting depends on the time needed for dissipation of reactive power and fully stop up the MOSFETs.

Main experimental results are shown ot Fig.3,4 and 5:


Fig.3

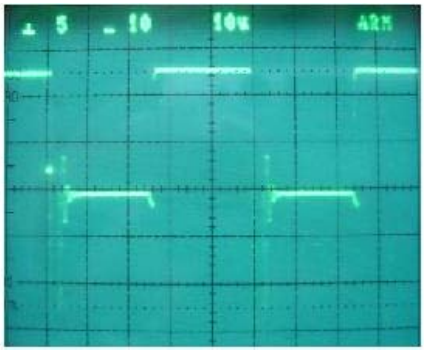

Fig4.

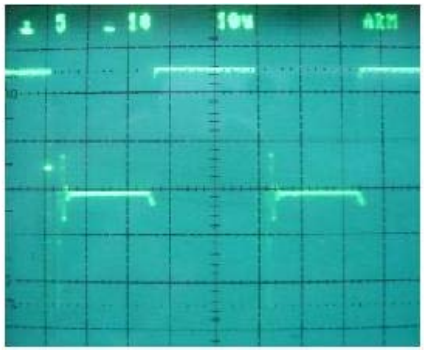

Fig.5

Fig.3 shows input PWM voltage and output driver voltage(to the gate of MOSFET).There is delay in rise of gating signals, which demonstrate time adjusting of adaptive feedback. Fig.4 and fig.5 shows the voltage $V_{DS}$ of one transistor at $R_{LOAD}$= 30 ohms and $R_{LOAD}$=30 ohms, $L_{LOAD}$ =1,9mH

## 5.CONCLUSION

Driver circuit with adaptive feedback have application in devices with synchronously drived switches, because need of dead-time in operation cycle. Proposed circuit improves performance of switching regulators by proper adjusting dead-time.This allow to reduce switching losses, dissipation of reactive power which increase total efficiency and lower total losses. This driver circuit remove need of any fixed delay settings for most drivers and every pointed disadvantages of their use.

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