HIGH-RESOLUTION FRONT-END FOR ECG SIGNAL PROCESSING

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This paper presents research system with 12 channel high-resolution (24 bits) front-end for ECG signal processing. The implemented high-resolution data conversion makes the system suitable for recording of late potentials which are microvolt-level high-frequency waveforms in the terminal portion of the QRS complex in patients prone to sustained ventricular tachycardia. The front-end consists of 12 channel ECG amplifier built on body potential driving concept. The amplifier outputs are connected to 12 delta-sigma ADCs. The whole ADCs work synchronously at 8 kHz sampling frequency and their output data are transferred to PC via USB. The presented system could be useful in other signal processing applications where multi-channel, high-resolution, data conversion is needed.

Keywords: high-resolution ADC, multi-channel ECG amplifier, multi-channel data transmission

1. INTRODUCTION

The high-resolution signal-averaged ECG has become a widely accepted technique for noninvasive risk assessment in patients prone to ventricular tachycardia and sudden death. This technique helps in detecting of so called 'late potentials': microvolt-level high-frequency waveforms in the terminal portion of the high-pass filtered QRS complex, correlating strongly with sustained ventricular tachycardia [1].

High-pass digital filters with corner frequencies of 25 to 40 Hz are most commonly used to remove low-frequency components within the QRS complex and ST-segment. After averaging and filtering the late potentials could be estimated by frequency (FFT) and time domain signal analysis techniques. According to the recommendations of Breithardt's Committee, a late potential exists if [2]:

- the filtered QRS complex is longer than 114 ms
- the root mean square amplitude of the terminal 40ms portion of the QRS vector magnitude is less than 20 uV
- the time during which the terminal vector magnitude remains below 40uV is longer than 38 ms.

Although 12 bits ADC resolution is enough for standard ECG signal processing, for recording of late potentials the resolution should be as high as possible.

This paper presents a high-resolution (24 bits), 12 channel, ECG data acquisition system for recording and signal processing of late potentials.

2. PRACTICAL REALIZATION

The block diagram of the presented high-resolution ECG data acquisition system is shown in fig.1. It consists of 12 channel ECG amplifier, 12 ADCs ADS1251, system microcontroller C8051F133, signal isolation integrated circuits (ICs) ADuM2400 and USB interface IC FT245.

The ECG amplifier is built on body potential driving concept [3, 4]. This is economical in respect to used operational amplifier structure and is especially suitable for multi-channel biosignal amplification. The amplifier has frequency band at 3dB from 0.05 to 120Hz which is usual for ECG amplification. The gain is set to relatively low value 150 (43.5dB). This gain allows up to ±30mV input signal range at ±5V supply voltage and corresponds to 1μV/LSB if the resolution is limited to 16 bits.

The 12 ADC chips operate in parallel. We selected and used the ADS1251 [5], which has the following main characteristics:

- ADC bit resolution – 24 bits;
- Sampling frequency for each channel – 20 kHz;
- Low power consumption – 5 mW;
- Applications with external reference voltage;
- Possibility for synchronous operation of multiple ADCs;
- Relatively low cost.

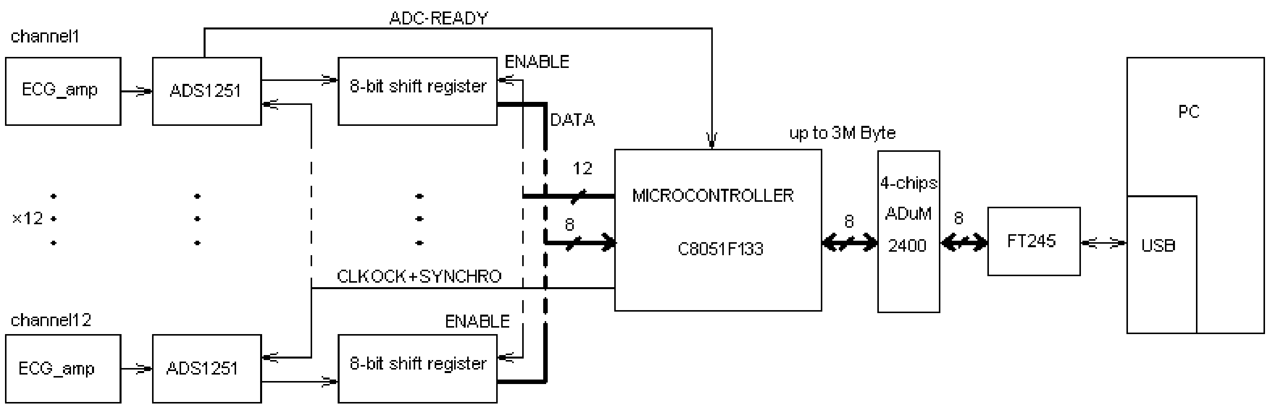

Fig. 1. Block diagram of the high-resolution ECG data acquisition system

Because the ADCs output data are in serial format they are converted in parallel form by means of twelve 8 bit shift registers.

The system works as follows:

At power on, the C8051F133 microcontroller performs synchronization on all 12 ADC ICs and starts the data conversion routine [6].

Within each data conversion cycle, with duration of 125us, the performed real-time operations are as follows:

- When one of the ADC chips is ready with the conversion (all ADC chips are synchronized) it generates a signal 'ADC READY' to the microcontroller
- The microcontroller enables all ADCs to store the first byte of the conversion result into the shift registers
- The microcontroller reads consecutively all shift registers and stores the data for each channel

- The procedures in previous two steps are repeated for the second (9-16 bits) and the third bytes (17-24 bits)
- The microcontroller transfers the stored data to the personal computer (PC)
- All procedures are completed within 125 us, i. e. one conversion cycle, and after that the microcontroller waits for a new 'ADC READY' signal.

The data transfer between the C8051F133 microcontroller and PC is performed through USB channel using an interface IC FT245.

The ICs ADuM2400 assure a reliable high voltage isolation between the front-end system and the PC, as well as an data transfer speed up to 10 Mbit/s. In the developed system (12 channels, 8 kHz, 24-bit ADC) the speed of data transfer is 3 Mbit/s.

For further data processing on PC we developed appropriate Windows based software. The software makes the mentioned USB communication and visualizes the received 12 channel ECG data.

3. EXPERIMENTAL RESULTS

Fig. 2 represents a noise signal, which is acquired through the most-noisy channel in the system. The sampling frequency is 8 kHz and the channel amplifier input is grounded. Thus the shown signal represents the intrinsic noise of the studied channel. The horizontal lines shown in fig. 2 correspond to the bit number within the ADC range and are included in order to facilitate the estimation of the noise amplitude. The peak-to-peak noise level is estimated to around 9-bits. It should be noted that there is no problem in detection of pacemaker pulses since their amplitude is usually higher than 23-bits (they always saturate the ECG amplifier). The rms value of the noise from fig. 2 is shown in fig. 3 and is calculated to 6.6 bits.

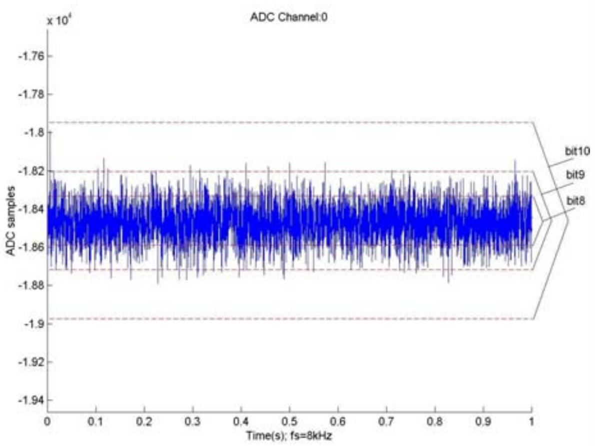

Fig. 2. Intrinsic noise of one ADC channel

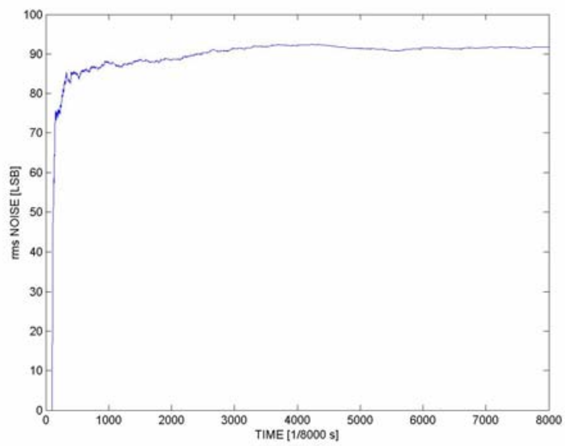

Fig. 3. The rms value of the noise as measured in fig.2

A real ECG signal sampled by one channel of the system with pacemaker pulses is shown in fig. 4. One pacemaker pulse from fig. 4, with duration of 0.5 ms, is zoomed in fig. 5.

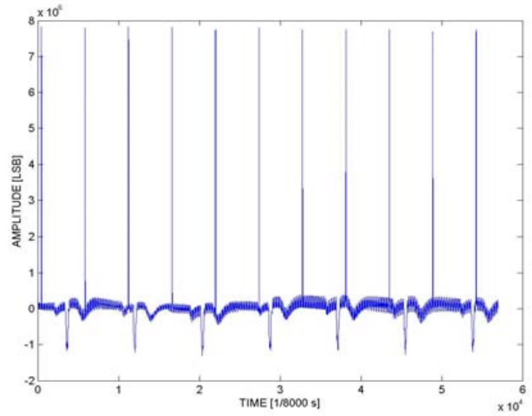

Fig. 4. Real ECG signal acquired by one channel of the system with pacemaker pulses

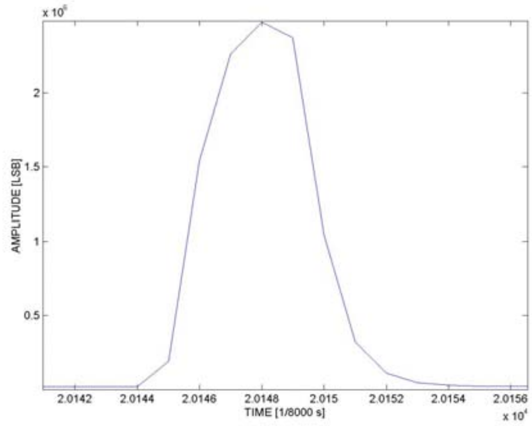

Fig. 5. Zoomed pacemaker pulse (from figure 4) with duration of 0.5 ms.

Fig. 6 represents again the noise signal from fig. 2, but after 8 point moving average filter with first zero at 1 kHz. Its rms value is shown in fig. 7. We should note that the implemented moving average filter does not influence on the ECG frequency band (assuming that the significant frequencies in ECG signal are up to 100 Hz) and is useful for noise reduction when ECG signal pre-processing is applied without pacemaker detection.

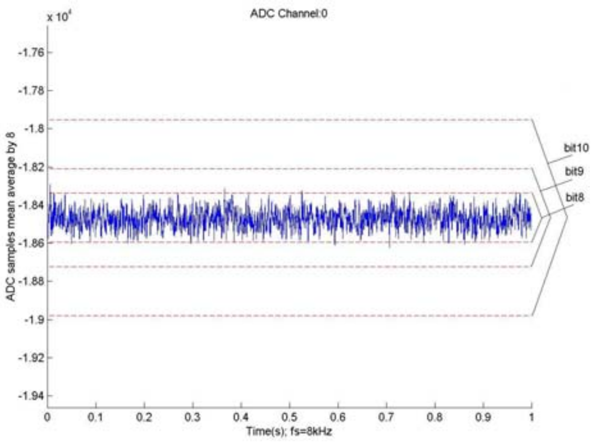

Fig. 6. Intrinsic noise of one ADC channel when signal-averaging by 8 samples is applied

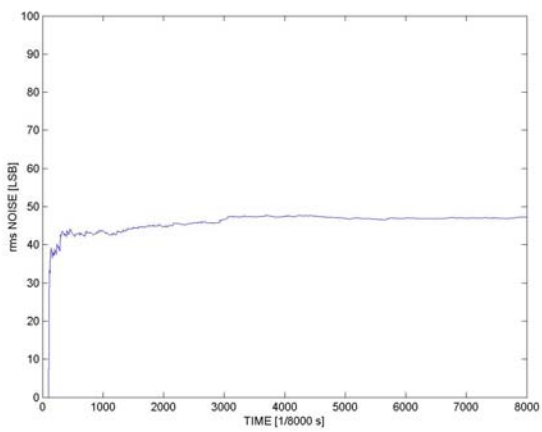

Fig. 7. The rms value of the noise as measured in fig.6

Note that the delta-sigma ADCs are integrating types ADC. If the sampling frequency is reduced the noise is integrated and also is reduced. If the sampling rate is reduced to 40Hz the effective resolution could be 23 bits [7].

While the term 'noise free bits' (NFB) are connected to peak-to-peak level of input noise, the effective resolution or effective number of bits (ENB) are connected to rms value of the noise. Because the common accepted conversion factor between peak-to-peak and rms noise is 6.6 the noise free bits are equal to effective bits rms - 2.7 bits [8].

In general the resolution is increased when the signal averaging is performed and averaging by 4 increases the resolution by 2 (one bit).

The measured effective number of bits (ENB) of the examined channel acording to fig. 3 are:

ENB = Full Scale Range – rms noise = 24 - 6.6 = 17.4 bits or expressed in dB as signal to noise ratio (SNR):

$$\mathrm{SNR} = 20\log\left(\frac{256^3}{92}\right) \approx 105dB$$

The usage of the proposed 8 point moving - average filter (fig. 7), the ENB could be increased by 1.5 bits and SNR by 9dB.

The measured current consumption of all circuit is 270 mA, supplied by the USB port (5V) of the PC.

The system operation is shown in Fig. 8. Transferred 12-channel ECG signals are real-time visualized on the PC screen by the developed software. The channels can be switched on and off and the desired channels can be selected, zoomed and off-time examined.

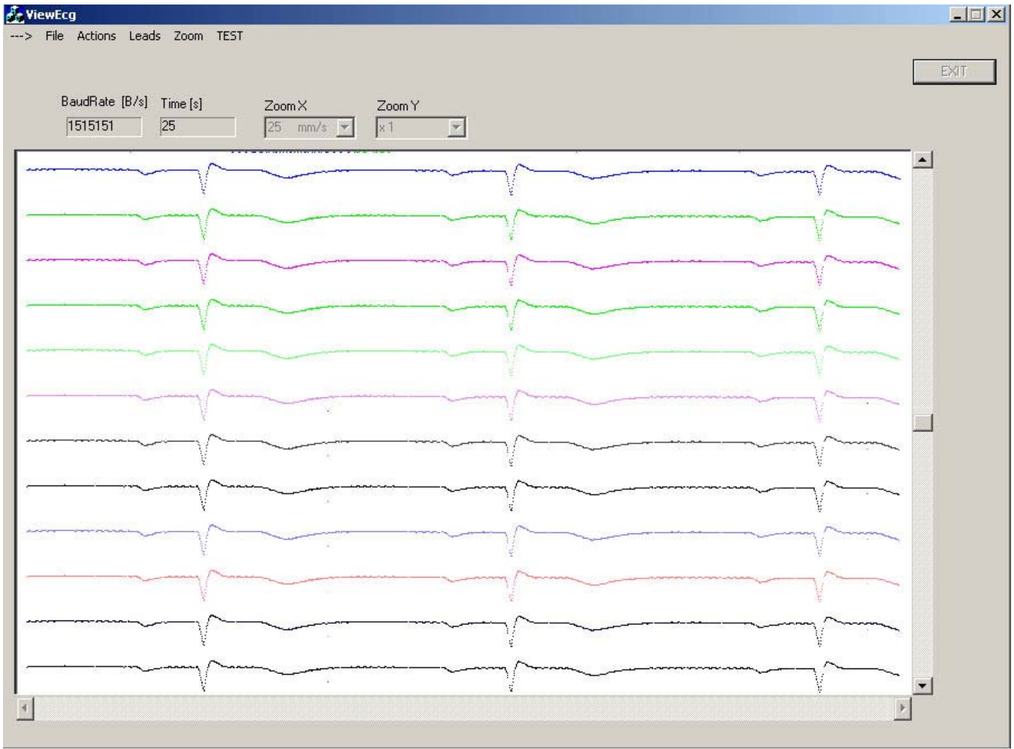

Fig. 8. PC Application for real-time visualization of 12-channel ECG data received from the ECG front-end

4. CONCLUSION

A high-resolution front-end for ECG signal processing was presented. The main characteristic of the described system should be pointed out:

- 12 channel ECG amplifier
- Simultaneous 12 channel delta-sigma AD conversion with 24 bit resolution and 8kHz sampling frequency
- Effective number of bits (ENB): 17.4 bits
- Patient isolation by ICs ADuM2400
- Data transmission to PC through USB

The presented system could be useful in other signal processing applications where multi-channel, high-resolution, data conversion is needed.

5. REFERENCES

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