MODELING AND IMPLEMENTATION OF THIRD ORDER SIGMA-DELTA MODULATOR

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Sigma-Delta (∑Δ) modulation has become more and more popular alternative for robust and inexpensive analog-to-digital (A/D) conversion for the past years. As a result of this, the converters based on 1-bit ∑Δ modulators are widely used in different applications. In this paper we present an experimental electronic realization of a third order Sigma-delta modulator. The general third order modulator is converted into decomposition of low order modulators, which interact through the quantizer function. The electronic circuit allows adjustment of the modulator's parameters and thus, obtains desired limit cycles. It can be used for making measurements and for comparison between the simulated and measured results. Its electrical scheme is simulated with the use of PSpice and it is shown that there is a good coincidence between the simulated and the measured results.

Keywords: Sigma-delta modulators, PSpice.

1. INTRODUCTION

The Sigma-Delta (∑Δ) modulation technique was first introduced in 1962 in Japan [1]. However, despite this its advantages have only been realized in the past recent years as high accuracy, 20-bit and beyond, conversion has become available. Analog-to-digital (A/D) conversion involves transforming time and amplitude continuous signal into time and amplitude discrete signal. Sampling makes the analogue signal time discrete and quantizing makes the signal amplitude discrete [2], [3]. Sampling process introduces errors that can be eliminated but errors due to quantizing, otherwise known as quantization noise, can only be reduced.

A disturbance called aliasing can occur if the sampling rate is less than two times the maximum signal frequency. Sampling is carried out at the Nyquist frequency when the sampling frequency is two times the signal bandwidth. Over-sampling, which is the number of times the sampling frequency is greater than the signal Nyquist frequency, reduces quantization noise in the recovered base band [4]. Noise shaping suppresses the quantization noise at low frequencies which usually covers the band of interest and it amplifies the quantization noise at high frequencies. This process reduces further the quantization noise present in the base band and therefore gives an increased Signal-to-Noise-Ratio (SNR). The resolution of a converter is the accuracy in bits of the conversion and is related to the SNR at the output of the converter. Higher order modulators are preferred because of their superior noise performance and relative freedom from harmonic quantization effects but more effort

is required to avoid instability. The basic structure of a Sigma-Delta modulator is shown in Fig.1, and it consists of loop filter with transfer function G(z) followed by a one bit quantizer in a feedback loop. The system operates in discrete time.

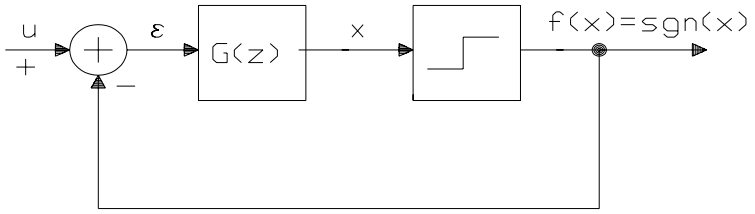

Fig. 1. Basic structure of a first order ∑Δ modulator.

The main difference to a conventional A/D converter is that Sigma-Delta converters trade off sampling rate with amplitude resolution. This means that they sample at very high rates but only need one bit of amplitude resolution. The advantage is that they trade reduced analogue circuit requirements for increased digital circuit complexity. They only require a single bit A/D and D/A converter with a relatively inaccurate analogue integrator. These are simple analogue circuits, unlike those in conventional A/D converters, and are therefore easily implemented in VLSI circuitry. Because the Sigma-Delta modulator uses very high sampling rates, a simple RC-filter is adequate to prevent aliasing. The input filter can pass frequencies many times higher than the frequencies of interest before filter cut-off is required. The need for abrupt cut-offs in recovery filters is also eliminated.

There is an ever growing list of applications of the Sigma-Delta modulators. Among the most common are high performance audio, image processing, communications and specialized instrumentation.

The aim of this paper is to present an electronic implementation of a third order Sigma-Delta modulator utilizing the parallel decomposition technique [5], that allows adjustment of modulator's parameters and to compare the measurement results with the results obtained via simulation by PSpice. The hardware realization scheme eventually is going to be introduced in the lab exams of the Theoretical Electrical Engineering discipline at the Technical University of Sofia. The paper is organized as follows. In the next section we give a theoretical background of the Sigma-Delta modulation. Then in Section 3 we present the PSpice model of the modulator and its corresponding electrical scheme. Simulations and measurement results are compared and they show a good coincidence. The final conclusions are given in Section 4.

2. THEORETICAL CONCEPTS OF SIGMA-DELTA MODULATION

2.1. Model for a sigma-delta modulator

In Fig. 2 a model for a single bit first order Sigma-Delta modulator is shown. The quantization error $e_q[n]$ is fed back and summed with the input. By subtracting the error signal from the input signal it is obtained an average error in the output signal of zero. This is where the function of a Sigma-Delta modulator excels that of conventional A/D converters. The feedback causes noise shaping. Q is a 1-bit quantizer which produces a 1-bit data word for each sample. Note that there is no

D/A converter in the feedback loop that sums with the analogue input signal. This is due to the two quantization levels, with values V+ and V-. It would introduce no error, so its analogue output signal contains the same information as its digital input signal. T is a time delay that must be present in the loop back to the input. The summing junctions are denoted by **Σ**. [*n*] indicates a step in time, i.e., *n*=1,2,3,4, etc. In other words, time has discrete values.

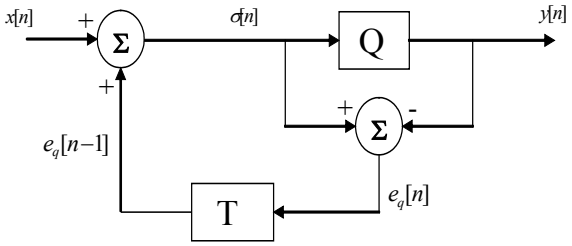

Fig. 2.Model for a 1-bit, first order Sigma-Delta modulator**.**

The way in which a sigma-delta modulator converts an input signal into a digital output signal is explained by using a DC input signal but the theory also applies to an AC signal. The feedback loop in the model forms a servo function that tends to drive $\sigma[n]$ toward zero. The system tries to minimize the error between its input and output, which gives rise to such a variation in *y* [n], that its average value will approximate the input signal over time.

From the upper the following equations can be derived:

$$\sigma[n] = x[n] + e_q[n-1] \tag{1}$$

$$e_q[n] = \sigma[n] - y[n]. \tag{2}$$

It should be noted that the range of $x[n]$ must be less than or equal to the output range of the quantizer, because if $x[n]$ exceeds this range, the system gets overloaded because it cannot correct itself anymore.

2.2. Model for a higher order sigma-delta modulator

Let us consider a N-th order modulator with a loop filter with a transfer function *G(z)*. Suppose the transfer function has *N* real distinct roots of the denominator. The corresponding block diagram of the modulator is given in Figure 3 [5].

The state equations of the following Sigma Delta modulator are:

$$\begin{aligned} x_k(n+1) &= \lambda_k x_k(n) + \left[u(n) - f\left(\sum_{i=1}^{N} b_i x_i(n) \right) \right] = \\ &= \lambda_k x_k(n) + \left[u(n) - f\left(\mathbf{b}^T \mathbf{x}(n) \right) \right] = \\ &= \lambda_k x_k(n) + \left[u(n) - y(n) \right], k = 1,2,...,N \end{aligned}, \tag{3}$$

where $\lambda_1, \lambda_2, ..., \lambda_N$ are poles (or modes) of the loop filter,
$\mathbf{b}=(b_1, b_2, \ldots, b_N)^T$ is the vector of fractional components coefficients and $\mathbf{x}=(x_1, x_2, \ldots, x_N)^T$ is the state vector.

The quantizer function is a sign function:

$$y(n)=f\left(\sum_{i=1}^{N}b_i x_i(n)\right)=f\left(\mathbf{b}^T\mathbf{x}(n)\right)=\begin{cases}1, & \mathbf{b}^T\mathbf{x}(n)\geq 0\\ -1, & \mathbf{b}^T\mathbf{x}(n)<0\end{cases} \quad (4)$$

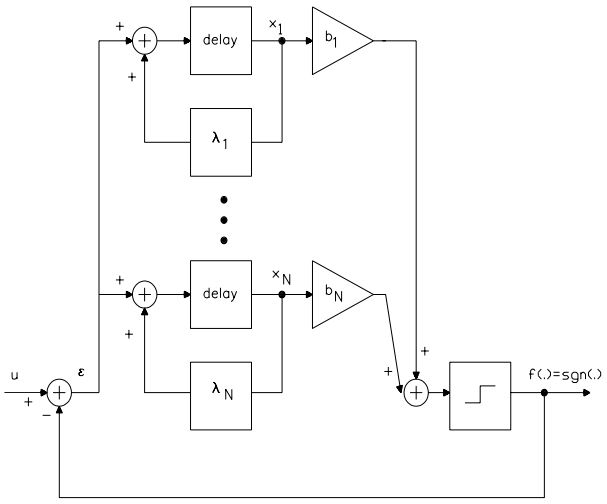

Fig 3. Block diagram of the modulator using detailed parallel form of the loop filter**.**

Using this technique a model of third or higher order modulator can be easily obtained. With the usage of this parallel form of the loop filter it is possible to create an adjustable modulator structure that allows the possibility to easily change the values of every pole and fractional coefficients either on software simulations or hardware implementations. With the ability to change these coefficients desired periodic solutions can be easily obtained [5], [6].

3. Model of the Schematic Implementation of a Third Order Sigma-Delta Modulator and PSpice Simulations

This higher order model of the electronic realization is an extension of a first order modulator electronic implementation [7]. In this case since the modulator is third order we have a three loop filter segments in the scheme. For the purpose of loop filter realization the TL061/Ti operational amplifier series were used in the scheme. The same amplifiers are utilized in conjunction with adjustable resistance in order to provide functionality for realization possibility to adjust modulators' coefficients λ_k and b_k through them. In such a case for every loop filter segment four operational amplifiers are needed – one for integrator realization, two for both coefficients and one to invert back the signal to a normal one. In such case to optimize the board we used TL064/Ti TSOP package, which contains four TL061/Ti elements gathered in one generalized corpus, so in this case for every loop filter segment only one electronic element on the PCB is needed.

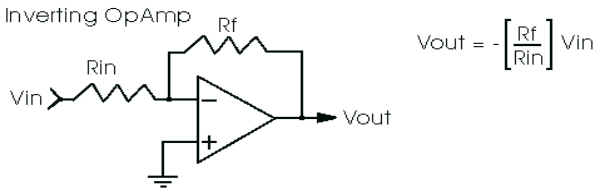

Fig 4. Adjustment of the coefficient's gain values

The adjustment of λ_k and b_k is possible when adjusting the appropriate designated resistor's value in schematics in a way as shown in Fig.4. In this case R_f is set to

1Kohm and only the value of R_{in}, which in our case is adjustable, has to be changed in order to set the desired coefficient value. Fig. 5 presents the full PSpice model of our third order modulator implementation created with the usage of parallel decomposition technique. The circuitry accepts AC or DC analog input sources from the active range 0 to 1V and gives digital output signal at its output. This is very convenient for us, because operating input voltages are always rescaled for the range from 0 to 1 and when in this case the range is varying from 0 to 1V there is virtually no need to rescale the input signals. The purpose of TL061/Ti in the scheme is described already. LM311 element is a low power low offset voltage comparator. The 74HC74 element is a D-type positive edge triggered flip flop with clear and preset. The other elements that are used in the schematics are regular DC voltage sources, resistors and capacitors. Digital synchronization clock signal is used for the 74HC74 part and all the results that have been obtained are gained when applying 100 KHz clock signal.

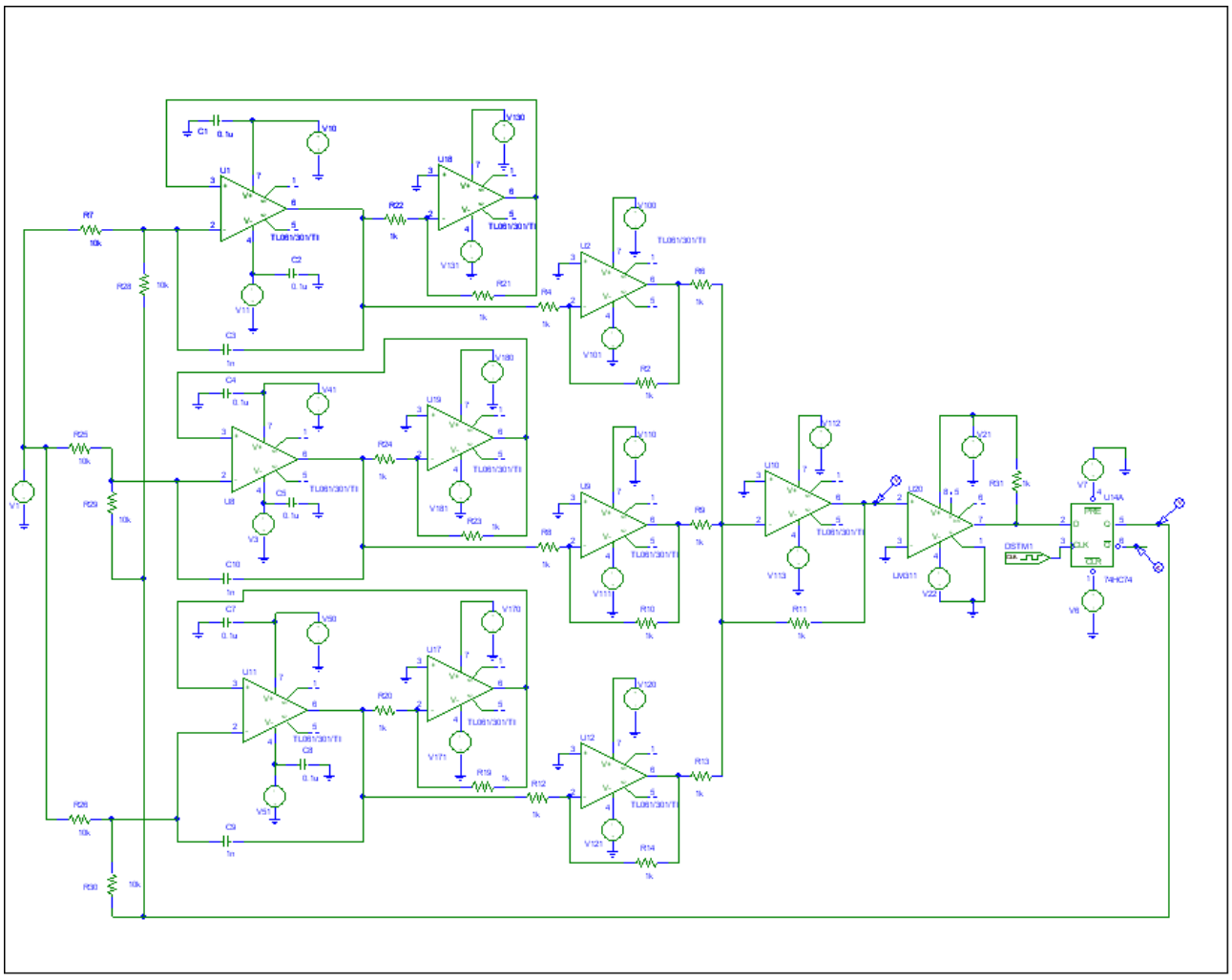

Fig. 5. The proposed third order Sigma-Delta modulator electronic circuitry realisation model in PSpice

For verification purposes we created a third order modulator model based on parallel decomposition technique in the Matlab Simulink environment. On Fig.6 is presented our modulator's model in Matlab Simulink software environment. We observed similar modulator behavior of the Simulik model, when we compared it

with the PSpice schematics model and the hardware implementation. When applying different modulator coefficients on the simulated models and schemes the modulator's stability range zone is varying and usually the modulator is stable when applying input signals from the 0.05-0.95 range. If we have some λ_k coefficient with a value greater than 1, then in most of the cases the modulator becomes unstable. In order to avoid modulator's instability on the PSpice model and on the electronic realization, through the utilized adjustable resistances we can adjust the values of λ_k and b_k only for the range from 1 to almost zero, when scaled respectively. For simplicity all the results that are given on the following figures in that section are for the case when all the coefficients value for both λ_k and b_k equals to 0.75 – in this case all of the adjustable resistances R_{in} are set to 1.43 Kohm. Also in order to make testing conditions similar for the models and for the hardware implementation we applied DC input source signal with value 0.7 from the scaled range.

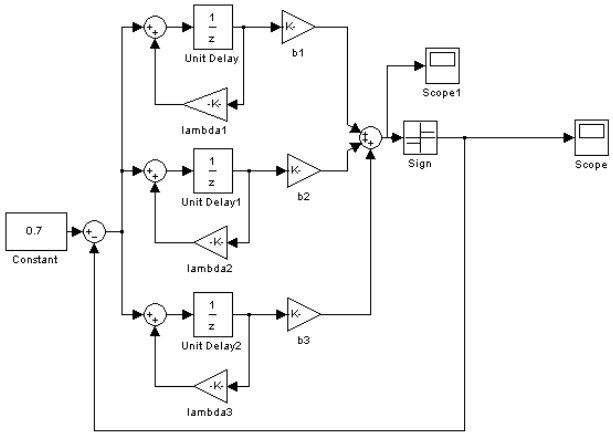

Fig. 6. The proposed third order Sigma-Delta modulator model in Matlab Simulink

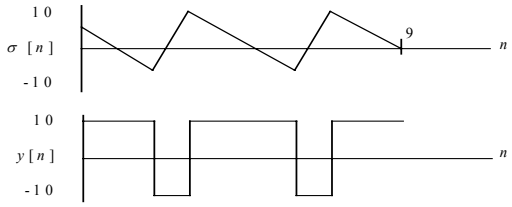

Fig. 7. Desired theoretical modulator output signals

As a desired theoretical result on both models the output of the modulator's loop filter and its global output should look like the graph shown in Fig 7.

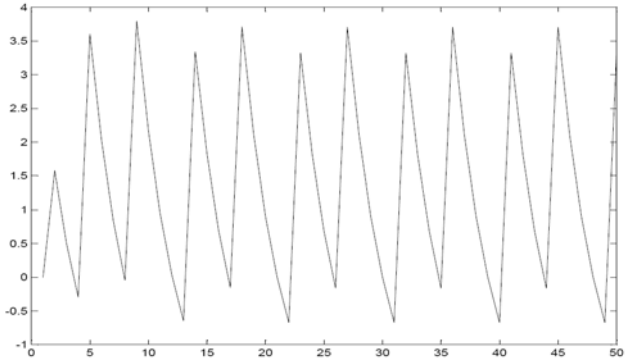

Fig. 8. Plot of the loop filter's output signal of Matlab Simulink model

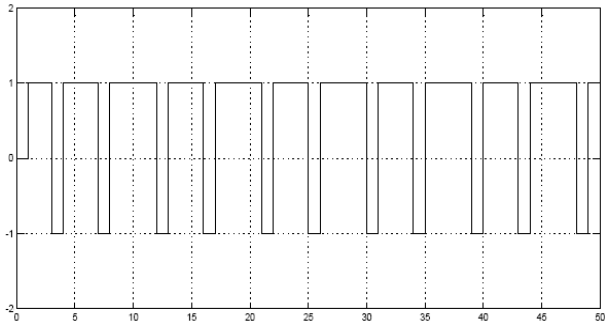

Fig. 9. Plot of the global modulator's output signal of Matlab Simulink model

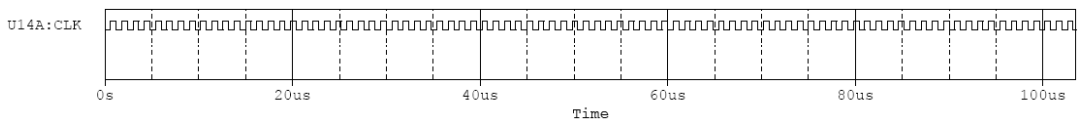

Fig.10. Plot of the modulator's digital clock synchronization signal on the PSpice model for 74HC74 flip-flop

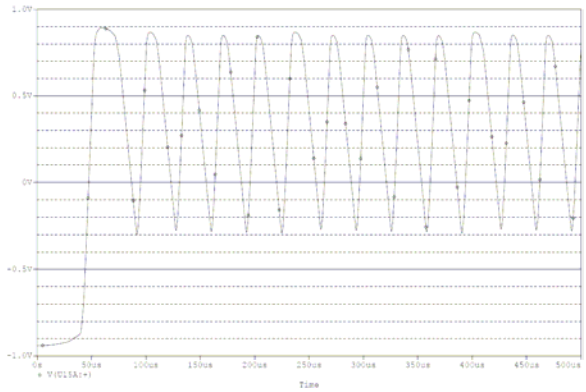

Fig. 11. Plot of the loop filter's output signal on the PSpice model

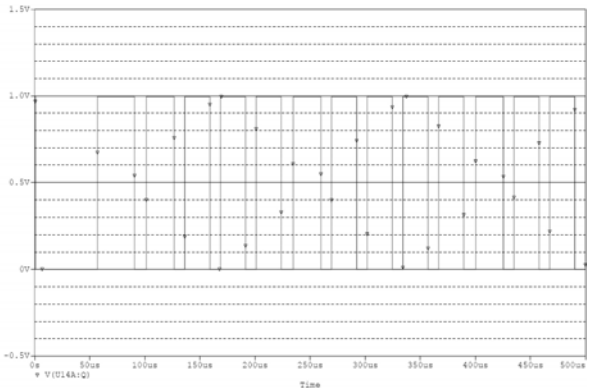

Fig. 12. Plot of the global modulator's output signal on the PSpice model

On Fig. 8,9,11 and 12 a comparison between the obtained results for both Simulink and PSpice models is presented. For every model a plot of its loop filter output and global modulator output is given. As it can be seen from the figures the models behave in a similar fashion when the same initial and parameter conditions are applied. On Fig. 10 is given a plot of the modulator's clock signal that is used for the PSpice model and in the hardware implementation.

4. CONCLUSION

The electronic realization of the presented third order sigma-delta modulator appeared to be working fine and without problems, which make it ready for future incorporation within the laboratory practice of TEE.

5. REFERENCES

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