A METHOD TO DEFINE THE LOSSES IN AUDIO-AMPLIFIER CLASS D

Plamen Angelov Angelov

Faculty for Computer Science, Engineering and Natural Studies, Burgas Free University, 62 San Stefano Street, 8001 Burgas, Bulgaria, office phone: +359 56 900404, GSM: +359 898 663819, e-mail: pangelov@bfu.bg

The following article offers a method to define the loss with low-frequency amplifiers class D. A method to choose the outlet switch transistors, having in mind parameters such as: transition resistance – Rds, maximum working voltage – Umds and maximum drain current – Imd is being discussed

Keywords: power loss, MOSFET audio amplifier

1. INTRODUCTION

With class D audio-amplifiers the outlet transistors working like a switch and for this reason their dissipation power is much lower than that of other working classes. No cooling radiator is used for voltage up to 4 W and in this way the system is minimized [1]. This makes the use of battery feeding and the installation of the amplifier in micro-systems possible.

2. TASK OF THE ARTICLE –A METHOD TO DEFINE THE EFFICIENCY OF THE POWER TRANSISTORS

The efficiency of an LFA is expressed by the extent to which the energy consumed by the feeding source is transmitted to the outlet as a useful signal and by the amount of it that is lost as warmth. At present the known LFA are the amplifiers, working in classes B and AB, the effective work in this case is good but is accompanied by a higher non-linear distortion and a limited dynamic range of the output signal [1]. To

2.1. Outlet switch transistors – basic parameters

The basic loss in class D low-frequency amplifiers are in the outlet electronic switches. The quick outlet function of the switch is one of the basic parameters for the arm function and that is why MOSFET transistors are most frequently used since they have the quickest function compared to the other classes BJT, IGBT.
For function with a minimal loss other parameters such as:

Vds [V] - Drain-Source Breakdown Voltage;
Id [A] - On state drain current;
Rds [Ω] - Static Drain-Source On-Resistance;
Ciss [F] - Input Capacitance;
Coss [F] - Output Capacitance FET;
tr [S] - Turn-On Rise Time;
tf [S] - Turn-Off Fall Time;

Qrr [C] - Body Diode Reverse Recovery Charge;
Qg [C] - Total Gate Charge.
All the other MOSFET transistor parameters [1] have no relation to the present article and that is why have not been discussed here.

2.2. A method to define the power dissipation in the switch transistors with a class D amplifier

2.3. A method to define Drain-Source Voltage in the switch transistors with a class D amplifier

The equivalent of this voltage determines the choice of a particular MOSFET transistor. The increase in the working voltage results in the increase in its internal resistance. This increases the loss and reduces the efficiency. To achieve an optimum ratio between efficiency and output voltage transistors with maximal feeding voltage and minimum transition resistance – Rds are selected. Let us now define the value of the feeding voltage – Udd. To define this parameter we use the expression (1) of the output voltage

$$P_{out} = \frac{1}{T}.\int_0^{t_1} \frac{[U_{dd} - U_{ds}]^2}{2.R_{load}}.dt \approx \frac{1}{T}.\frac{U_{dd}{}^2}{2.R_{load}}.t_1 = \frac{U^2{}_{dd}}{2.R_{load}}.\delta\ [W]$$
$$\Rightarrow U^2{}_{dd} = \frac{2.P_{out}.R_{load}}{\delta} \Rightarrow U_{dd} = \sqrt{\frac{2.P_{out}.R_{load}}{\delta}}\ [V] \quad (1)$$

where:
Plout [W] –Effective output power;
Udd [V] –power supply;
Uds [V] –On Drein-Source Voltage;
Rload [Ω] – load;
T [s] –period of input squire signal – fig.2.;
t1 [s] –time of the impulse of the input series - fig2
$\delta = \frac{t_1}{T}$ - duty cycle;

After we determine the value of the feeding voltage, we select a suitable MOSFET transistor. Having defined the type of the chosen MOSFET transistor, we record all the parameters, mentioned in item 1. After that we determine the loss over the static output resistance – Static Drain-Source On-Resistance.

2.4. Loss over Static Drain-Source On-Resistance

The power dissipation of the output MOSFET transistor is in direct relation to the resistance Rds [Ω]. The personal resistance /Static Drain-Source On-Resistance/ Rds [Ω] is determined by technological parameters in the process of making the transistor. These parameters are mentioned in the producer's technical specifications.[2]
The power dissipation over the transition resistance can be defined like this:

(2) $P_{dRds} = \frac{1}{T}.\int_0^{t_1} I_d{}^2.R_{ds}.dt = I_d{}^2.R_{ds}.\delta\,[W]$

where:
Id [V] –Output current;
Rds [Ω] –Static Drain-Source On-Resistance;
T [s] –period of input squarewave signal;
t1 [s] – impulse time;
$\delta = \frac{t_1}{T}$ - duty cycle;

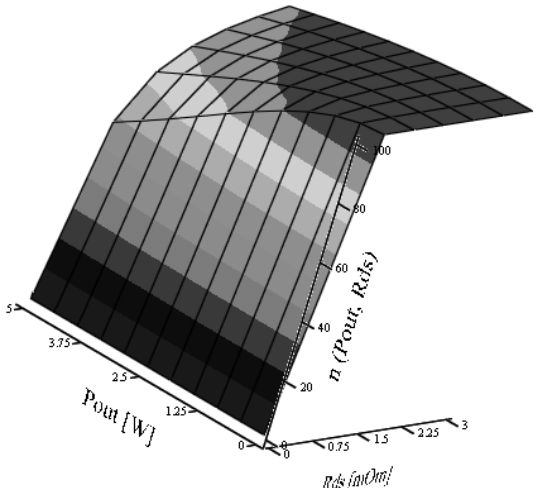

Fig.1. The efficiency coefficient depends on the two variables $n = F(P_{our}, R_{ds})$

Knowing this power dissipation, we can determine the efficiency of the arm according to this parameter with the help of the expression:

(3) $n(R_{ds}) = \frac{P_{out}}{P_{out} + P_{dR_{ds}}} = \frac{P_{out}}{P_{out} + I_d{}^2.R_{ds}.\delta}.100\,[\%]$

where:
Pout [W] –Effective output power;
Prds [Ω] –power dissipation on resistor *Rds*;

The efficiency coefficient depends on the two variables: Plout & Rds. This relation $n = F(P_{our}, R_{ds})$ has been shown in fig.1. The diagram shows the linear dependence of the function $n = F(P_{our}, R_{ds})$ with low output voltage, while with an increase in the voltage over 1 [W], the function assumes a non-linear character. Hence the following conclusion can be drawn: With an increase in the output voltage the efficiency drops down. To reduce power dissipation loss, we should choose a transistor with minimum Static Drain-Source On-Resistance.

2.5. Defining switching losses

These are caused by the transition processes in the switching over of the outlet transistor. In most general terms, switching loss can be defined by the expression:

(4) $P_{\sum_{n=1}^{2} P_n} = P_{sw} + P_{gate}\,[W]$

where:
Psw [W]- output switching losses;
Pgate [W]- input charging losses;

The graphic presentation of the transition processes has been shown in fig.2. The diagram shows the type of the main voltage transmitted to the switch and the transition commutation processes caused by this.

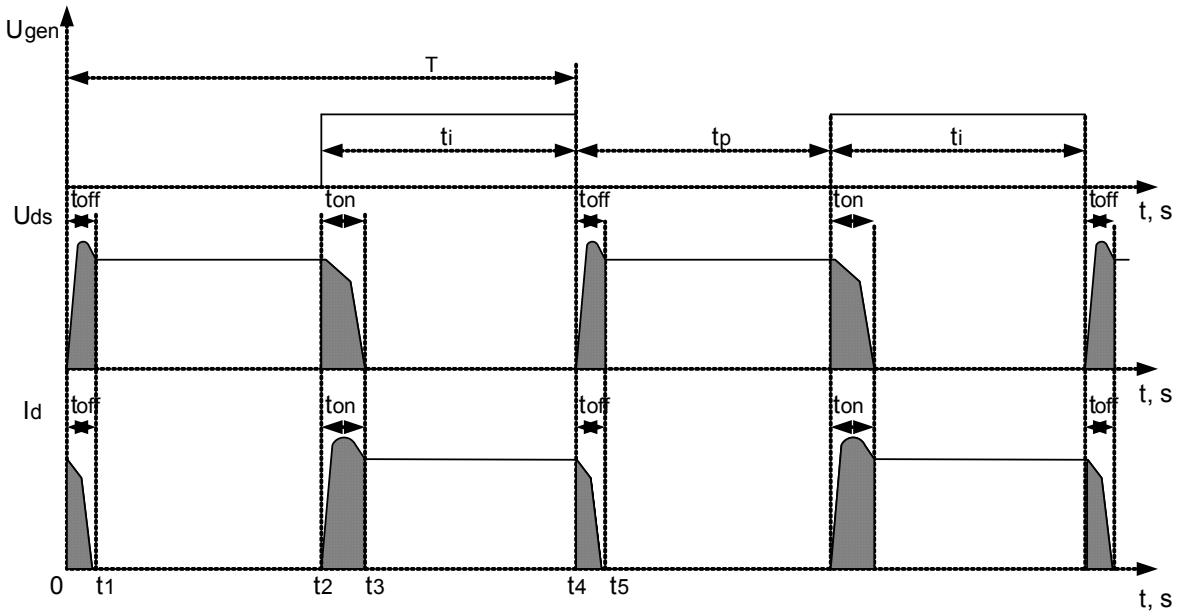

Fig.2 Characteristics of the transition processes in the transistor outlet

The switch loss Psw [W] is presented in the following way:

$$P_{sw} = \frac{1}{T}.\int_0^{t_1} P_{swoff}(t).dt + \frac{1}{T}.\int_{t_2}^{t_3} P_{swon}(t).dt = \frac{1}{T}.\int_0^{t_1} u_{ds}(t).i_d(t).dt + \frac{1}{T}.\int_{t_2}^{t_3} u_{ds}(t).i_d(t).dt =$$

(5)

$$= \frac{1}{T}.\int_0^{t_1} [\frac{I_d.U_{dd}}{2} + \frac{U^2{}_{dd}}{2.t}.C_{oss}].dt + \frac{1}{T}.\int_{t_1}^{t_2} [\frac{I_d.U_{dd}}{2} + \frac{U^2{}_{dd}}{2.t}.C_{rr}].dt \ [W]$$

where:

Pswon [W] – power dissipation when transistor switch turn on;

Pswon [W] –power dissipation when transistors switch turn off.

After we calculate expression(5), we get:

(6) $P_{sw} = f_{sw}.\frac{I_d.U_{dd}}{2}.(t_r + t_f) + f_{sw}.\frac{U^2{}_{dd}}{2}.C_{oss}.\ln(t_f) + f_{sw}.\frac{U^2{}_{dd}}{2}.C_{rr}.\ln(t_r)[W]$

If we substitute $C_{rr} = \frac{Q_{rr}}{U_{dd}}[F]$ in expression (6), we will get:

(7) $P_{sw} = f_{sw}.\frac{I_d.U_{dd}}{2}.(t_r + t_f) + f_{sw}.\frac{U^2{}_{dd}}{2}.C_{oss}.\ln(t_f) + f_{sw}.\frac{U_{dd}}{2}.Q_{rr}.\ln(t_r)\ [W]$

where:

tr [s] - rise time;

tf [s] –fall time:

Coss [F] –Output Capacitance (FET + Schottky);

Qrr [C] –Body Diode + Schottky Reverse Recovery Charge [4].

In the contemporary MOSFET electronic switches a backward linked diode which prevents backward voltage is installed to protect the transistor. In this way if the voltage Uds [V] turns negative, this diode unblocks and protects the transistor. On the other hand, the use of the diode increases the output capacity of the scheme Coss [F] [3] and shortens the commutation time. For this reason the outlet diode is shottki.

Having defined the value of the output switching losses, let us determine the value of the input charging losses

(8) $$P_{gate} = f_{sw} \frac{U_g.Q_g}{2}.[\ln(t_f) + \ln(t_r)]\ [W];$$

where:

Ug [V] – input squarewave signal;

Qg [C] –Total Gate Charge.

Substituting (7) & (8) in expression (4), for switching losses we get:

(9) $$P_{\sum_{n=1}^{2} P_n} = P_{sw} + P_{gate} = f_{sw}.\frac{I_d.U_{dd}}{2}.(t_r + t_f) + f_{sw}.\frac{U^2{}_{dd}}{2}.C_{oss}.\ln(t_f) + ...$$
$$... + f_{sw}.\frac{U_{dd}}{2}.Q_{rr}.\ln(t_r) + f_{sw}\frac{U_g.Q_g}{2}.[\ln(t_f) + \ln(t_r)]\ [W]$$

2.6. Defining the overall efficiency.

On the basis of the conducted analysis of outlet transistor loss, we can write down the following equation:

(10) $$P_{d\sum} = P_{dRds} + P_{\sum_{n=1}^{2} P_n} = P_{dRds} + P_{sw} + P_{gate} = f_{sw}.\frac{I_d.U_{dd}}{2}.(t_r + t_f) + f_{sw}.\frac{U^2{}_{dd}}{2}.C_{oss}.\ln(t_f) + ...$$
$$... + f_{sw}.\frac{U_{dd}}{2}.Q_{rr}.\ln(t_r) + f_{sw}\frac{U_g.Q_g}{2}.[\ln(t_f) + \ln(t_r)] + I_d{}^2.R_{ds}.\delta\ [W]$$

where:

Pd∑ [W] –the overall power dissipation loss in the outlet transistors

Hence what we get about the efficiency of outlet transistors is:

(11) $$n(P_{d\sum}) = \frac{P_{out}}{P_{out} + P_{d\sum}}.100\ [\%]$$

3. CONCLUSIONS

1. Two parameters – maximum output voltage of the amplifier and working voltage should be observed while choosing the working voltage of a MOSFET transistor.
2. The increase in the output voltage requires a higher-voltage transistor which in turn increases the output capacity. The increase in this parameter results in an increase in the switch-over period of the transistor and the efficiency drops down.
3. To improve the efficiency when using outlet transistors, transistors with minimum transition resistance and minimal commutation time should be selected.

4. REFERENCES

[1] Eric Galas „Class D Audio Amplifiers" Analog Dialogue 40-06, June (2006)

[2] Alfa&Omega Semiconductor "AO4916A Dual N-Channel Enhancement Mode Field Effect Transistor with Schottky Diode"]

[3] Jorge Cerezo, Class D Audio Amplifier Performance Relationship to MOSFET Parameters, International rectifier]

[4] Guerra A., Andoh K. and Fimiani S. "Ultra-fast Recovery Diodes Meet Today quirements for High Frequency Operations and Power Ratings in SMPS Applications". International Rectifier White Paper. http://www.irf.com