APPLICATION OF GENERAL-PURPOSE CIRCUIT SIMULATORS TO AUTOMATED DESIGN AND INVESTIGATION OF CLASS E POWER AMPLIFIERS

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In the present paper an approach is proposed to computer-aided design and investigation of class E power amplifier using the possibilities of general-purpose circuit analysis programs such as PSpice. Power amplifiers performance is rated in terms of the characteristics concerning the amplifier efficiency.

1. INTRODUCTION

In this paper a procedure for automated design and investigation of the class E power amplifier is developed using the possibilities of a general-purpose circuit analysis program such as *PSpice*. The integration of the design and analysis stages allows reuse of the design procedure as well as fast power amplifier components sizing and characteristics assessment.

Power amplifiers are the most power consuming building blocks of RF transceivers. Their efficiency is expressed by the part of the dc power, which is converted to RF power. The main parameters for power amplifier efficiency assessment and comparison are the drain efficiency (*DE*), power-added efficiency (*PAE*) and overall efficiency [1]. In the present paper they are automatically calculated from the simulation results using postprocessing in the graphical analyzer *Probe*. In addition, based on parametric analysis, the efficiency characteristics and the output power are automatically obtained as a function of the supply voltage, operating frequency, number of the transistor gates, etc. Based on macrodefinitions in Probe, calculation of RMS input and output powers is accomplished.

Examples are presented illustrating the applicability of the proposed approach to computer-aided design and investigation of the class E power amplifiers. It allows an adequate and fast obtaining of the amplifier characteristics, comparison of variants, as well as performance optimization at the design stage.

2. AUTOMATED DESIGN OF CLASS E POWER AMPLIFIERS

Class E power amplifiers provide a large output power with high efficiency working in switch mode [2]. A power amplifier could be defined as class E if a few criteria are fulfilled: the voltage across the switch remains low when the switch turns off; when the switch turns on, the voltage across the switch should be zero; the first derivative of the drain voltage with respect to time is zero, when the switch turns on. The first two conditions suggest that the power consumption by the switch is zero.

The last condition ensures that the voltage-current product is minimized even if the switch has a finite switch-on time. A typical configuration of a class E power amplifier is shown in Fig. 1.

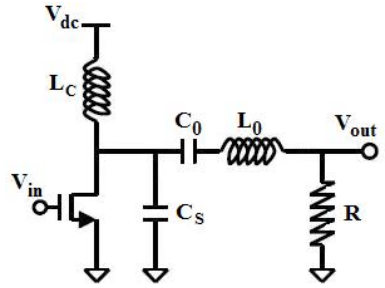

Fig. 1. Class E power amplifier basic circuit

The procedure for automated design of class E power amplifier using general-purpose simulator is based on the approach for investigation of class E amplifier with nonlinear capacitance for any output quality factor Q and finite dc-feed inductance [3] and its realization in *PSpice* is presented in [4]. This approach takes into account the fact that at high operating frequencies the parasitic capacitance of the switching device is dominant in the shunt capacitance C_s (Fig.1) and in the extreme case it is entirely formed by the transistor output capacitance. The following assumptions are made: the shunt capacitance consists of only the parasitic capacitance on the MOSFET; the switching time of MOSFET is enough small to be neglected; the MOSFET has infinite OFF resistance and nonzero ON resistance R_s, which is included in the list of input design parameters. Since the power MOSFET contains a p-n junction body diode, the parasitic capacitance C_{ds} can be expressed by:

$$C_{ds} = \frac{C_{j0}}{\left(1+\frac{v_s}{V_{bi}}\right)^m} \tag{1}$$

where V_{bi} is the built-in potential, v_s is the drain to source voltage, C_{j0} is the capacitance at v_s=0, and m is the grading coefficient of the diode junction.

The basic input parameters of the procedure are: the operating angular frequency $\omega=2\pi f$; the resonant angular frequency $\omega_0=2\pi f_0$; the ratio of the resonant to operating frequency $A=f_0/f$; the ratio of resonant to parasitic capacitance on MOSFET transistor $B=C_0/C_{j0}$; the ratio of resonant to dc-feed inductance $H=L_0/L_c$; the loaded quality factor $Q=\omega L_0/R$; the switch-on duty ratio of the switch D. The parameters H, Q, R, V_{dc}, V_{bi}, m, R_s, and D are given as design specification. The cofficients A and B are determined to meet the class E switching conditions: $v_s(t)=0$ and $dv_s(t)/dt=0$ when the switch turns on. In [4] the optimal values of A and B are derived by parametric analysis with two independent variables. Since the *PSpice* simulator allows only one variable defined into a parametric sweep, setting of two independent variables is reduced to parametric analysis with respect to one common variable *NAB*. The application of a parametric analysis in combination with the time domain analysis allows the use of a standard *PSpice*-like simulator for determination of the optimal coefficients A and B. They are obtained for the parameter *NAB* value corresponding to the minimal value of the product of the voltage $v_s\ (t)$ and the current $i_{cs}(t)$ (proportional to the derivative dv_s/dt) when the switch turns on. The determination of A and B is accomplished in the graphical analyzer *Probe*.

In the common case of the grading coefficient m the capacitance current i_{cs} is obtained from the expression:

$$i_{cs}(t) = \frac{\mathrm{d}}{\mathrm{d}t}\left(C_{j0}\left(1+\frac{v_s}{V_{bi}}\right)^{-m} .v_s(t) \right). \tag{2}$$

The equivalent circuit corresponding to (2) is shown in Fig. 2. The dependent voltage source V_1 is controlled by the capacitor voltage v_s and is described in the form:

$$V_1 = v_s(t)\left(1+\frac{v_s(t)}{V_{bi}}\right)^{-m} \tag{3}$$

The dependent current source J_1 is controlled by the current $i_1(t)$: J_1=1.$i_1(t)$. The *PSpice* realization of the model is shown in Fig. 3. The voltage controlled voltage source $E1$ describing V_1, is of EVALUE type. The current controlled current source $F1$ describing $J1$ is of FNOM type.

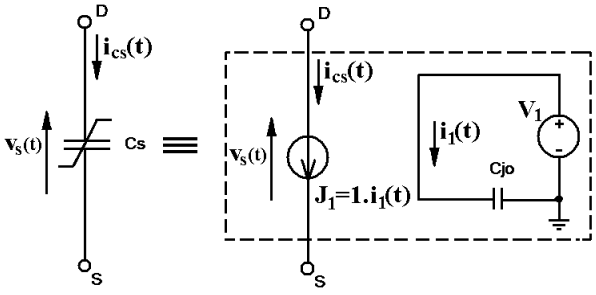

Fig.2. Equivalent circuit describing the nonlinear shunt capacitance

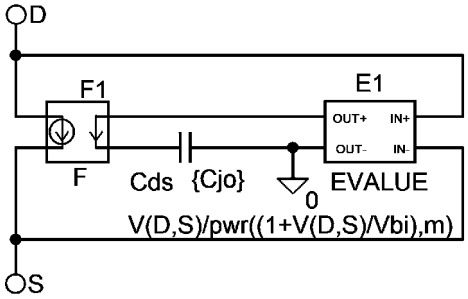

Fig.3. PSpice realization of the nonlinear capacitance model

3. EFFICIENCY ASSESSMENT

The following stage of the procedure for automated design and investigation of the Class E power amplifier is the assessement of the characteristics of the amplifier concerning its efficiency, and namely:

$$DE = \frac{P_{RFout}}{P_{DC}}, \quad PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}}, \quad \eta = \frac{P_{RFout}}{P_{DC} + P_{RFin}} \tag{4}$$

where P_{RFout} and P_{RFin} are the output and the input power at the desired frequency, and P_{DC} is the dc power supplied from the voltage supply source. They are automatically calculated using postprocessing in the graphical analyzer *Probe* [6].

A simulation example (Fig. 4) is used for demonstrating the possibilities of the procedure for automated design of a low-voltage class E power amplifier having the following UMTS application specifications: f=1.95GHz, V_{dc}=1.1V, P_{out}=0.5W. It is used a *PSpice* transistor model for a standard CMOS 0.35μm integrated technology.

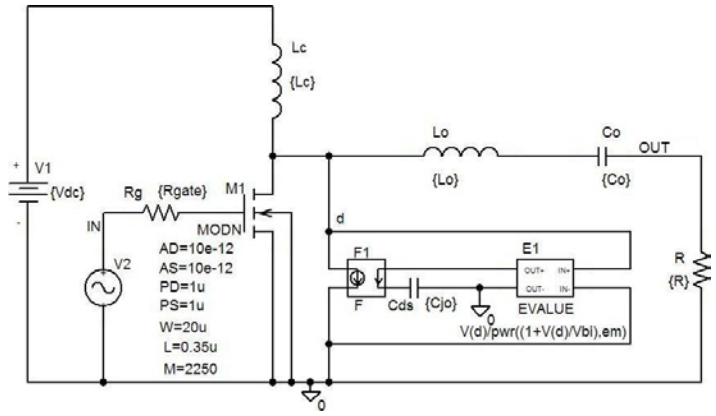

Fig.4. Simulation example circuit of class E power amplifier

The design specifications are defined in *PSpice* using the parameter statement PARAMETERS:

* *Design specifications*

.PARAM H=3; Q=5; R=0.84;s Rs=0.1; Rgate={W*Rsh/(3*L*M*M)}; Vdc=1.1;
+ Fc=1.95G; pi=3.141592654; Rsh=7; Vbi=0.69; em=0.34; Fo={A*Fc};
+ Wc={2*pi*Fc}; Wo={2*pi*Fo}; Lc={Lo/H}; Lo={Q*R/Wc};
+ Co={1/(Wo*Wo*Lo)}; Cjo={Co/B}

* *Determination of NA and NB*

.PARAM Amin=0.85; Amax=0.97; Bmin=0.2; Bmax=0.25; NAmax=5; NBmax=5;
+ NABmax={NAmax*NBmax}; NAB=22; DA={(Amax-Amin)/(NAmax-1)};
+ DB={(Bmax-Bmin)/(NBmax-1)}; A={(Amin+(NA-1)*DA)};
+ B={(Bmin+(NB-1)*DB)}; NB={(NAB-1E-6-NA)/NAmax+1};
+ NA={ NAmax*(atan(tan(((NAB-1E-6)/NAmax)*pi-pi/2))+pi/2)/pi}

The corresponding macro-definitions in *Probe* for the efficiency parameters are:

Pdc = -AVG(I(V1))*1.1
Pin = RMS(I(V2))* RMS(V(V2:+)-VS(M1))
Pout = RMS(V(OUT))*RMS(V(OUT))/0.84
DE = Pout/ Pdc
PAE= (Pout-(Pin/V(M)))/ Pdc
h=Pout/((Pin/V(M))+Pdc)

The visualization of the efficiency parameters in dependence of the supply voltage or the number of the gates of the transistor is accomplished using a parametric analysis and in the graphical analyzer *Probe* using the function YatX(1,X_value) where 1 is the circuit variable (voltage, current or macrodefinition) and X_value is a time point where the circuit has obtained its for the steady state. The achieved waveforms are shown in Fig.5 and Fig. 6 for the output and drain to source voltage and the dependence of the output power and *PAE* versus the supply voltage change.

The obtained results are compared with those published in [5]. The investigations in the present paper and in [5] are fulfilled at the same design specifications, input

driving voltage and value of the optimal load resistance. As a result the received power added efficiency and output power as the most indicative parameters are 82.8% and 504.3mW comparing to 81.8% and 483mW published in [5].

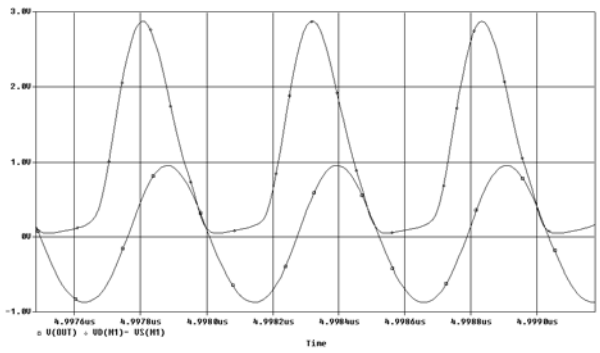

Fig.5. Output and drain-source voltage waveforms

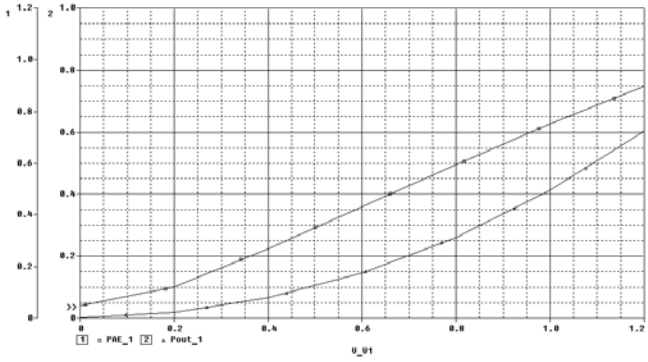

Fig.6. PAE and Pout vs. the supply voltage change

4. ACKNOWLEDGEMENT

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5. CONCLUSION

An approach has been presented to automated design and investigation of class E power amplifiers using the possibilities of general-purpose circuit analysis programs such as *PSpice*. The application of standard circuit simulators as a design tool allows reuse of the design procedure as well as taking into account the nonidealities of the active and passive circuit components.

6. REFERENCES

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