INTEGRATED ECG-PULSE MEASUREMENT CIRCUIT WITH LOW POWER CONSUMPTION

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In medical instrumentation the demand for small battery wearable measurement and control equipment is still growing. In the field of Electrocardiography 24 hour ECG recorders for medical applications and wireless pulse per minute measurement belts with watch displays for consumer applications are on the market. The discussed solution addresses high precision time measurement between ECG pulses. An integrated circuit was developed which measures the pulse duration with 12 bit resolution. The device includes preamplification, fully integrated bandpass filter, peak detector, time measurement unit and FSK modulator for wireless transmitter. The chip consumes 200uA at 3.3 Volt supply and occupies an area of 2.1 mm2 on a 0,35um CMOS DPTM Process with 0.5 mm2 core area only.

Keywords: Electrocardiography, Pulse duration, wireless transmission, low power consumption.

1. INTRODUCTION

Electrocardiographic signals show a typical signature with a peak for each heart beat (Fig. 1). For some heart diseases, like arhythmics, measurement of the duration between two peaks is very important. Using clinical ECG equipment these measurements can be done by calculations on the stored data. Our aim however was to develop a low power pulse duration measurement device witch is equipped with short distance wireless transmission. So the user may wear it quite unseen on his body with a receiver in his pocket, his watch or mobile phone for outdoor activities or a computer for indoor patient monitoring.



Fig. 1. Electrocardiogram

Typical ECG-Signal derived from the body by passive electrodes is defined by a maximum amplitude of 5 mVpp overlaid by a low frequency +/- 300 mV body voltage caused by muscle contraction and friction. To separate the peaks from the low frequency component is one of the critical tasks [1]. First we had to decide on the measurement resolution. An analogue decision error can be calculated by equation 1.

$$terr = \frac{Vreferr}{S} \tag{1}$$

Assuming a typical peak slope S of 15mV/ms for a normalized 0.5 V peak amplified by a factor of 100 and a noise floor on the reference voltage Vreferr of 5mV the analogue decision error is about terr = 0.33ms (Fig. 2). Based on the expected analogue accuracy we decided on a relaxed resolution of 1 ms for the digital time counter. This is good enough for consumer applications and for most clinical measurements, too. With a 12 bit time counter an ECG pulse time from 15 beats per minute up to more than 200 beats per minute can be evaluated.



Next the measurement bandwidth must be decided. The IEC IEC60601-2-47: "Medical electrical equipment" norm defines a measurement band width of 0.67 Hz to 40 Hz for portable applications. For high precision clinical applications an extended bandwidth of 0.6 to 250 Hz or even 1 kHz is recommended. For our peak detection application a reduced bandwidth of 0.8 Hz up to 20 Hz is quite enough. In this case an additional 50/60Hz power line notch filter is not necessary.

The module will be supplied by a lithium cell with 3.3 Volt and 24 mAh. Supply current for the total measurement module should be less than 1mA to guarantee a 24 hour operation. Fig. 3 shows a block diagram of the module consisting of a master clock generator, the measurement chip and an ASK-Modulator for a 128 kHz low frequency short distance transmission.



Fig 3. Module Block Diagram

2. CHIP ARCHITECTURE

2.1. General structure

One of the main requirements was to integrate as many elements as possible in the device. A block diagram of the IC is shown in Fig 4.



Fig. 4 Block diagram of chip architecture

A differential preamplifier with a gain of 10 is used for acquisition of the signal from the body. The following band pass is implemented with a switched capacitor high pass and a low pass function driven by a non overlapping clock of 500 Hz. The 3 dB-frequency of the high pass is specified with 0.8 Hz and 20 Hz for the low pass [4]. The filtered signal is amplified by the following stage by a factor of 10. The peak detector consists of a comparator function, a digital debounce circuit and a pulse former. Consequent pulses from the peak detector are used to start/stop the 12 bit gate counter. The pulse can be observed at pin R. A 16 bit serial data output frame is formed in the modulator block adding two leading und two trailing bits to the data. The 16 bit data word is transmitted three times for transmission security. FSK-modulated data is available on pin FSK for wireless transmission.

2.2. Operational Amplifier

A new type of operational amplifier RE_OB09 was designed for the application (Fig 5). [2,3]

Simulations show an open loop gain of 55 dB, GBW is 5.2 MHz and phase margin is 570 for a load of 1 pF. The OPAMP is optimized for low noise and low

power. A comparison between the new designed cell and library standard cells given in Table 1.



Fig 5: OPAMP RE_OB09

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OPAMP	Noise @10Hz	IDD			
	[nv/SqrtHz]	[uA]			
Standard OP	550	100			
LowNoise OP	100	290			
Wideband OP	150	1500			
RE_OP09	426	16			

Table 1: Noise over supply current

3. SIMULATION AND MEASUREMENT RESULTS

Fig. 6 shows the simulated bandwidth of the differential amplifier. Gain is 20.9 dB. The 3 dB frequency is 60 kHz and the power consumption is 50 uA. For the following SC- band pass filter a 3 dB frequency of 0.8 Hz was measured for the lower band and 11 Hz for the upper band. Figure 7 shows measured results for a square wave test signal of 1Hz at the differential input.

The lower curve (3) is measured at the output of the second amplifier, the middle curve (1) is the pulseoutput R of the peak detector and the upper curve (2) shows the burst of the 16 bit data word at pin SER transmitted 3 times. Figure 8 shows the data start peak R (1) for the measurement, the serial data (2) from the last measurement cycle and the FSK modulated output (3).



Fig 6: Frequency response of preamplifier





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of Fig. 7: Measured output for 1 Hz input signal



Fig. 9. The layout of IC.

Fig.	8:	Diagrams	for	serial	and	FSK
modu	ılat	ed data				

Heartbeat	Pulse	Serial Data	Error
[beats/min]	[s]	[digits]	[digit]
54.5	1.1 s	1096	- 4
60.0	1.0 s	1000	0
66.6	0.9 s	902	+ 2
75.0	0.8 s	798	- 2
85.7	0.7 s	702	+ 2

Table 2: Measured serial data output

From the measured serial data stream for different pulse signals with fixed frequency a total error of less than +/5 ms (=digits) can be expected.

4. CHIP DESIGN

The device is implemented on a 0.35um DPTM CMOS process. Analogue and mixed signal simulations are done with SPECTRE. The layout is shown in figure 9. Chip size is 1.4mm x 1.5mm.

5. CONCLUSION

A pulse measurement unit for electrocardiographic applications was developed, integrated and evaluated. A new operational amplifier was developed with a good noise performance and low power consumption. A fully integrated switched capacitor

high pass filter with a 3 dB frequency of 0.8Hz @ 500 Hz clock frequency was used to remove the low frequency signals.

6. REFERENCES

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