# SECONDARY EFFECTS IMPACT ON SUBMICRON MOS GENERIC WILSON CURRENT STRUCTURE

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*Abstract – Generic Wilson current structure exhibits performance of non-floating linear resistive element. This paper describes the impact of the secondary effects on submicron MOS generic Wilson current circuit. Subthreshold behavior, mobility degradation with both vertical and lateral field, velocity saturation and threshold voltage variation are analyzed. Simple analytical expressions are derived when it operates in subthreshold region and in the velocity saturation region as well. Simulation results, in MATLAB and PSpice, are given. One substantial implementation of the circuit is in all-MOS linear resistive grid for spatial retinotopic processing.*

**Keywords:** MOSFET, short-channel effects, subthreshold current, velocity saturation, Wilson current circuit

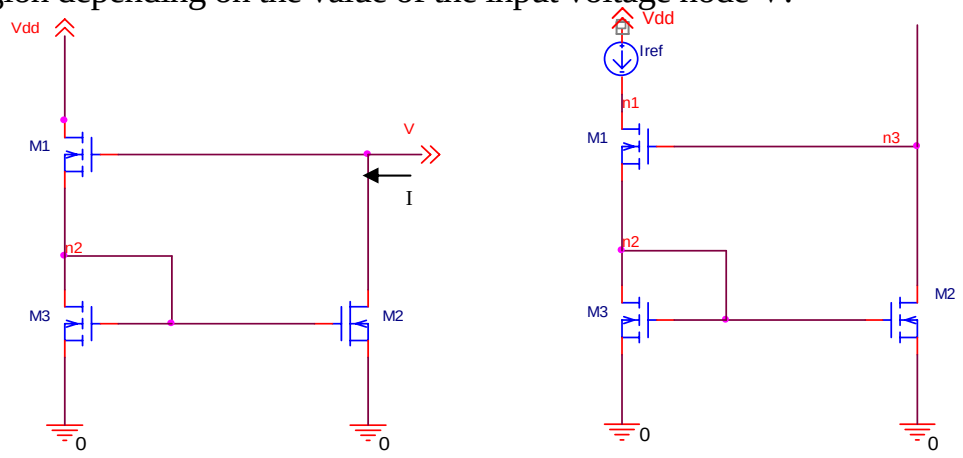
## 1. INTRODUCTION

To achieve higher operating speeds and increased packing densities, MOS-device structures have been subjects to greater and greater miniaturization. The decrease in MOS-device dimensions in itself can lead to major modifications in the observed device characteristics. Small-dimension effects, also referred to as short-channel effects [1-4], include, for example, shift in threshold voltage, velocity saturation and an increase in the subthreshold current. These modifications in device behavior are of major importance in practical applications. Many effects alter MOSFET device performance as the channel length shrinks. These effects arise as a result of a two-dimensional potential distribution and high electric fields in the channel region and a decrease in the physical separation between the source and the drain.

Wilson current mirror is an avoidable part of most analog and digital integrated circuits. Recently [5], it has been shown that generic Wilson current structure exhibits performance of non-floating linear resistive element. The aim of this paper is to describe the impact of the secondary effects on submicron MOS generic Wilson current structure. Firstly, we explore the subthreshold behavior including threshold voltage variation and mobility degradation with both vertical and lateral field and secondly we analyze the velocity saturation case. Simulation results in MATLAB and PSpice are presented. At last some important conclusions are given.'

## 2. SUBMICRON MOS GENERIC WILSON CURRENT STRUCTURE ANALYSIS

The MOS generic Wilson current structure is given in Fig. 1a. It differs from the original current mirror (Fig. 1b) in exclusion of a constant current source in the drain of M1 transistor, [6]. Actually, such circuit behaves as a voltage mirror circuit that exhibits linear resistive capability between the input node V and the ground. It comprises three MOS transistors: M1 and M3 are enhancement type and M2 is a depletion type MOSFET. Obviously, such arrangement is more suitable for the n-mos technology implementation. M2 operates in linear (ohmic or triode) region, while both enhancement type MOS transistors M1 and M3 operate either in the subthreshold region, or in the velocity saturation region depending on the value of the input voltage node V.




*(a)* *(b)*

***Fig. 1 a) MOS generic Wilson current structure b) Wilson current mirror***

### 2.1 Subthreshold region

The most important effects that arise from the two-dimensionality of the potential profile in short-channel devices are: threshold voltage reduction, mobility reduction by gate-induced surface field and degradation caused by subthreshold behavior [1-3]. In long-channel MOSFET [1], [2] the subthreshold drain current varies exponentially with $V_{GS}$ and it is independent of drain-source voltage ($V_{DS}$> *few kT/q* volts). In short-channel devices, the subthreshold drain current is found to increase significantly with increasing $V_{DS}$.

When input voltage V is less then $V_{TH1}+V_{TH3}$ ($V_{TH1}$ and $V_{TH3}$ are threshold voltages for M1 and M3, respectively), M1 and M3 are operating under the condition of weak channel inversion (subthreshold region). The current flowing through M1 and M3 is expressed as [4], [7]:

$$I_{D1} = \mu_0 C_d (w/L)_1 V_t^2 \exp(\frac{V_{GS1} - V_{TH1}}{nV_t}) = \mu_0 C_d (w/L)_1 V_t^2 \exp(\frac{V - V_G - V_{TH1}}{nV_t}) = I_{D3}$$
$$I_{D3} = \mu_0 C_d (w/L)_3 V_t^2 \exp(\frac{V_{GS3} - V_{TH3}}{nV_t}) = \mu_0 C_d (w/L)_3 V_t^2 \exp(\frac{V_G - V_{TH3}}{nV_t}) \quad , \qquad (1)$$

where, $\mu_0$ is the low-field carrier mobility, $C_d$ denotes the capacitance per unit area of depletion region under the gate, $(w/L)_1$ and $(w/L)_3$ are the gate geometry factor for M1 and M3, respectively, $V_t$ is the thermal voltage and $n$ is the subthreshold factor.

Expression (1) for subthreshold current takes into the consideration the variation of the body-source voltage $V_{BS}$ and it's valid if the drain-source voltage of MOS transistor is larger then $3V_t$. But, one must take care, the threshold voltage for short-channel MOSFET depends not only on the gate-source voltage, but also on the drain-source voltage and the gate dimensions. Short-channel effects are also included in the calculation of n. It can be found from (1) that the gate potential of transistor M2, $V_G$ is:

$$V_G = \frac{V}{2} + \frac{V_{TH3} - V_{TH1}}{2} + \frac{nV_t}{2} \ln[\frac{(w/L)_1}{(w/L)_3}]. \qquad (2)$$

For perfect match of the transistors M1 and M3, $V_G$ is proportional to the input voltage V ($V_G$=V/2). This is voltage mirroring effect, as an equivalent term with the term of current mirroring used in Wilson current circuit. Fig. 2a shows the disparity of the gate driving voltage $V_G$ from V/2.

### 2.2 Velocity saturation region

In the classical analysis of the long-channel MOSFET, there is no theoretical limitation on the velocity that carriers can attain in the surface channel. It is assumed that the velocity of the carriers is proportional to the channel electric field, independent of the value of that field. In other words, the carrier mobility is constant. However, in reality, at high electric field, the carriers fail to follow this linear model because mobility becomes field-dependent. When the electric field reaches some critical value, the velocity of the carriers tends to saturate. In silicon MOSFET with a channel length below 1 μm, only a couple of volts between drain and source are needed for carriers in the channel to reach a saturated velocity [3]. Limitation of the channel current due to velocity saturation is easily met in submicron short-channel devices.

When M1 and M3 are operating in the velocity saturation region and above subthreshold, the following equations for the channel currents hold:

$$\begin{aligned} I_{D1} &= v_{sat} C_{ox} w_1 (V - V_G - V_{TH1}) = I_{D3} \\ I_{D3} &= v_{sat} C_{ox} w_3 (V_G - V_{TH3}) \end{aligned}, \quad V > V_{TH1} + V_{TH3} \qquad (3)$$

where $v_{sat}$ is the saturated velocity of the carriers, $C_{ox}$ is the unit area oxide capacitance and $w_1$ ($w_3$) is the channel width of M1 (M3).

According to (3), the gate potential $V_G$ can be expressed as:

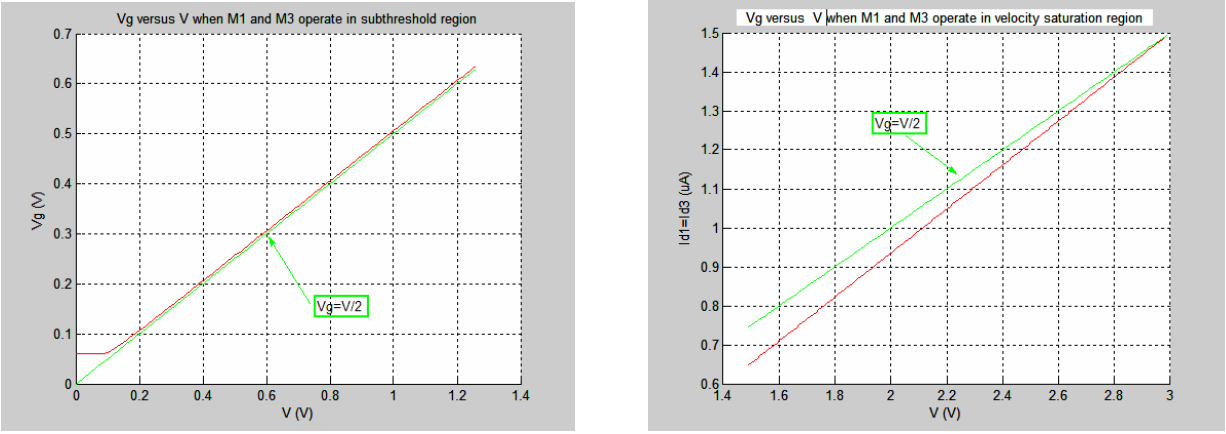
$$V_G = \frac{V}{1 + \frac{w_3}{w_1}} + \frac{(w_3/w_1)V_{TH3} - V_{TH1}}{1 + \frac{w_3}{w_1}} \qquad (4)$$

The disparity of the gate driving voltage $V_G$ from V/2, according to (4) is presented in Fig. 2b.

### 2.3 Wilson circuit as linear non-floating one-port resistive element

The drain current of M2, which represents the linear resistive element output current, when M1 and M3 are in subthreshold region is expressed as:

$$I = \frac{\mu C_{ox}(w/L)_2}{2}[V_{TH3} - V_{TH1} + 2|V_{TH2}| + nV_t \ln\frac{(w/L)_1}{(w/L)_3}]V \quad , \tag{5}$$




***(a)*** ***(b)***

***Fig. 2 Gate driving voltage of M2 for subthreshold operation (a) and velocity saturation (b)***

In the case when M1 and M3 operate in velocity saturation, the drain current of M2 is expressed as:

$$I = \frac{\mu C_{ox}(w/L)_2}{1+\frac{w_3}{w_1}}[(1-\frac{w_3}{w_1})\frac{V}{2} + \frac{w_3}{w_1}V_{TH3} - V_{TH1} + (1+\frac{w_3}{w_1})|V_{TH2}|]V \tag{6}$$

Relations (2) and (4) can be reduced to same mathematical form if $w_1 = w_3$ and $L_1 = L_3$ and can be rewritten as:

$$V_G = \frac{V}{2} + \frac{V_{TH3} - V_{TH1}}{2} \tag{7}$$

and the drain current of M2, can be expressed as:

$$I = \frac{\mu C_{ox}(w/L)_2}{2}[V_{TH3} - V_{TH1} + 2|V_{TH2}|]V \; . \tag{8}$$

At first glance, there is a linear dependence between current I and input voltage V. However, in submicron technology implementation one must take care of the effects due to the field-dependent mobility and the threshold voltage variation as well. Mobility reduction with both, lateral ($\mu$) and vertical field ($\mu_{eff}$) is usually modeled as [3]:

$$\mu = \frac{\mu_{eff}}{1+\frac{\mu_{eff}V_{DS}}{2v_{sat}L}} \; ; \; \mu_{eff} = \frac{\mu_0}{1+\Theta(V_{GS} - V_{TH})} \tag{9}$$

where $\mu_0$ is the low-field carrier mobility (bulk mobility) and $\Theta$ is the fitting parameter, while the threshold voltage variation must include shifts of the threshold voltage due to impact of several secondary effects such as body effect, narrow-channel effect, short-

channel effect and drain induced barrier lowering-DIBL [2], [4]. Fig.3 shows the impact of some of these effects on the drain current of transistor M2 when an ideal voltage mirroring occurs ($V_G$=V/2). Some of the BSIM3 MOSFET model equations [4], [7] are used in MATLAB simulation. Notice the difference in the drain current calculated with the classic equation for long channel MOS device in linear region (curve labeled as 4) and the one that includes short-channel effects (curve labeled as 1).

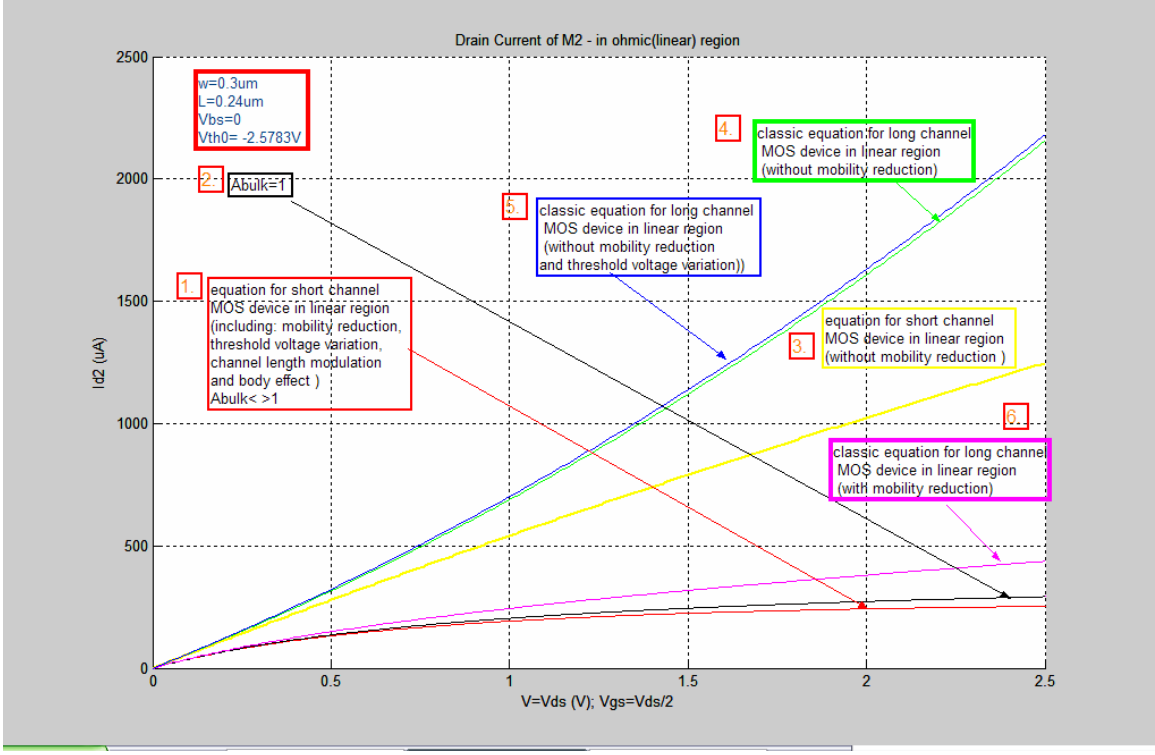



***Fig. 3 The impact of some secondary effects on the drain current of transistor M2***

## 3. BSIM3V3.0 SIMULATIONS

In the following we present the simulations taken from PSpice using BSIM3 MOSFET modeling. Output current, $I_{D2}$, for short channel versus long channel of M2 (M1 and M3 have same w/L ratio: $(w/L)_1=(w/L)_3$=0.3μm/0.25μm; w2=0.3μm) is given in Fig. 4, while the dependence of the output current, resistance and gate drive voltage on the input voltage V are shown in Fig. 5.

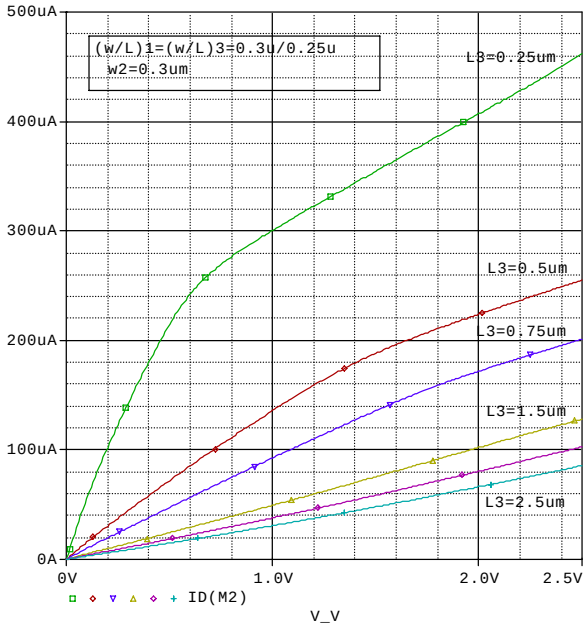
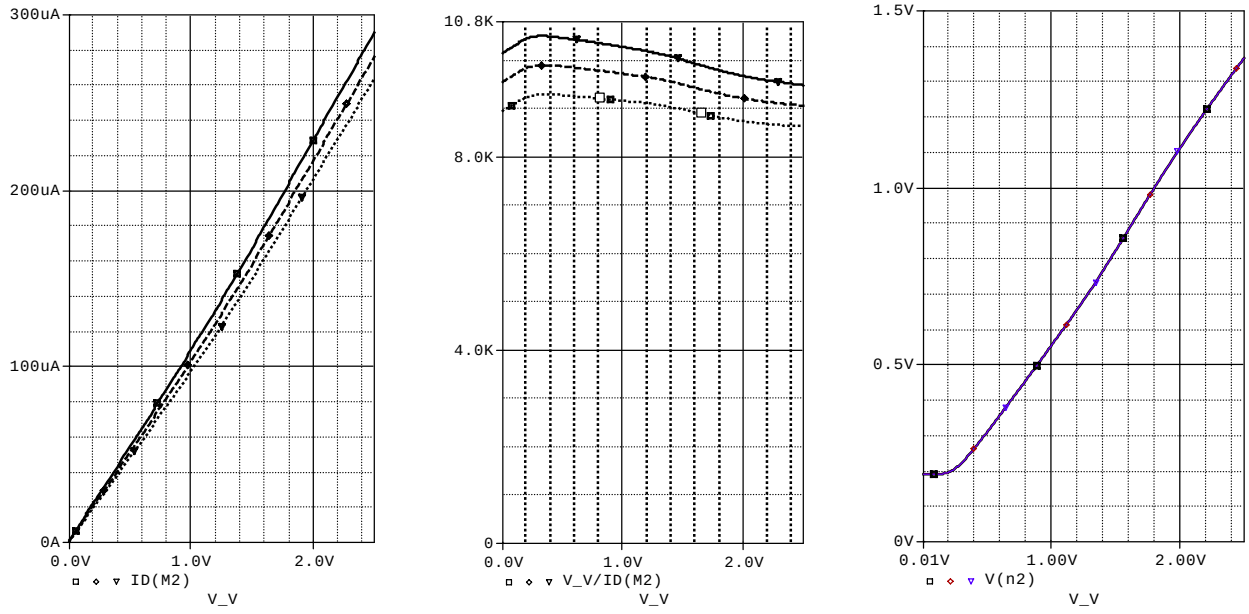



***Fig. 4 Short channel versus long channel of M2 output current $I_{D2}$ comparison***




***(a)*** ***(b)*** ***(c)***

***Fig. 5 Dependence of the output current (a) resistance (b) and gate drive voltage (c) on the input voltage V***

## 4. CONCLUSION

The impact of the secondary effects on submicron MOS generic Wilson current structure was presented. Subthreshold behavior, mobility degradation with both vertical and lateral field, velocity saturation and threshold voltage variation were analyzed. Simple analytical expressions were derived when it operates in subthreshold region and in the velocity saturation region as well. Simulation results, in MATLAB and PSpice using BSIM3 MOSFET modeling, are given.

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