CLASS E POWER AMPLIFIER FOR BLUETOOTH APPLICATIONS

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The main purpose of this paper is to present the design of a class E power amplifier for Bluetooth Class 1 application. The power amplifier has to provide 20 dBm output power and as high as possible power efficiency at 1.5V power supply voltage, for 0.35µm CMOS Austria Microsystems (AMS) technology.

Keywords: Class-E, CMOS, monolithic inductors, power amplifier

1. INTRODUCTION

The increasing role of wireless communications entails design and optimization of power amplifiers (Pas). Pas are the most power consuming part and main contributor of distortion products in a transceiver chain due to their inherent nonlinearity. They are widely used because of the large amount of output power with high efficiency they provide when working in switching mode. A power amplifier could be classified as a class E if a few criteria are met. The voltage across the switch remains low when the switch turns off. When the switch turns on, the voltage across the switch should be zero. Finally, the first derivative of the drain voltage with respect to time is zero, when the switch turns on. The first two conditions suggest that the power consumption of the switch is zero. The last condition ensures that the voltage-current product is minimized even if the switch has a finite switch-on time. A typical configuration of a class E power amplifier is shown in Fig. 1. L_1 acts either as an RF choke or as a finite dc-feed inductance. Class E power amplifiers theoretically achieve 100% efficiency in the expense of poor linearity performance.

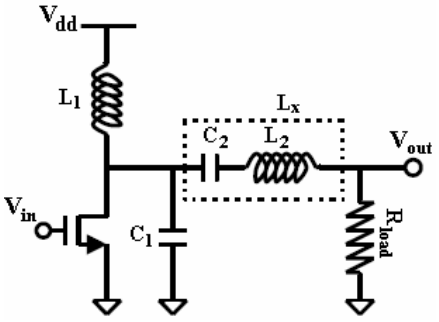

Fig.1. Class E power amplifier configuration.

Power amplifier performance is rated in terms of two basic groups of characteristics concerning the amplifier linearity and efficiency. Important parameters to estimate linearity include second order interception point (IP2), third interception point (IP3), and the 1 dB compression point. The main advantage in using the interception point is that it gives a figure to predict distortion level for given bias.

Power Added Efficiency (PAE), Drain Efficiency (DE) and overall power efficiency (η) are used to evaluate circuit efficiency:

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}}, \quad DE = \frac{P_{RFout}}{P_{DC}}, \quad \eta = \frac{P_{RFout}}{P_D - P_{RFin}}.$$

In this paper the results obtained by designing class E power amplifier for Bluetooth Class 1 wireless communication application are presented. The power amplifier is designed to provide 20dBm output power and as high as possible power efficiency at 1.5V power supply voltage, for 0.35μm CMOS Austria Microsystems (AMS) technology. The class E amplifier is designed in two versions – fully integrated (with integrated inductors designed from AMS) and partially integrated (with external inductors). Comparison between the two power amplifiers defining the possibilities of the used technology is made as well.

2. CLASS E POWER AMPLIFIER DESIGN PROCEDURE

The component values can be calculated using the following equations [1]:

$$L_X = \frac{\pi V_{dd}^2 \left(\pi^2 - 4\right)}{2\omega P_{out}\left(\pi^2 + 4\right)} \tag{1}$$

$$C_1 = \frac{P_{out}}{\pi \omega V_{dd}^2} \tag{2}$$

$$R_{load} = 0.577 \frac{V_{dd}^2}{P_{out}} \tag{3}$$

where P_{out} is the output power, V_{dd} is the supply voltage, $\omega=2\pi f$ is the operation frequency of the circuit. These equations are derived by the fact that the switch is either turned on or off. They are valid only for class E power amplifiers and R_{load} is not necessary the same for all cases of power amplifier [2]. R_{load} is usually called optimum load (R_{opt}) and is defined as a loading presented to the power amplifier for a desired output power with the highest efficiency. The optimum load is designed according to the specification on output power and the supply voltage.

Usually in the class E analysis L_1 is assumed to be an RFC ($X_{L1} > 10X_{C1}$). Indeed L_1 acts as either a RF choke (RFC) or as a finite DC-feed inductor because the serial resistance of the inductor is reduced with a smaller inductance value which provides higher efficiency than an RFC with the same output power and the same supply voltage [3]. The operating frequency can be pushed higher with a finite DC-feed inductor since the parasitic capacitors associated with the transistors are resonated out by the inductor. The capacitor used to fulfill the class E operation, C_1, can be

implemented by the parasitic capacitance of the transistor. Therefore, L_1, can be calculated by the resonant equation of a LC tank.

$$L_1 = \frac{1}{\omega^2 C} = \frac{1}{\omega^2 \left(C_p - C_1\right)} \tag{4}$$

where C is the total capacitance at the drain of the transistors, C_p, minus the required parasitic capacitor, C_1, in fulfilling the operating condition of a class E power amplifier.

The optimum load is typically about several ohms and can be obtained with the supply voltage and the output power fixed according to the specification of a wireless standard. In order to match the 50Ω loading is necessary to be implemented an up-conversion matching network to transform the optimum load to 50Ω load. The modified schematic of a class E power amplifier with an up-conversion matching network is given in fig.2.

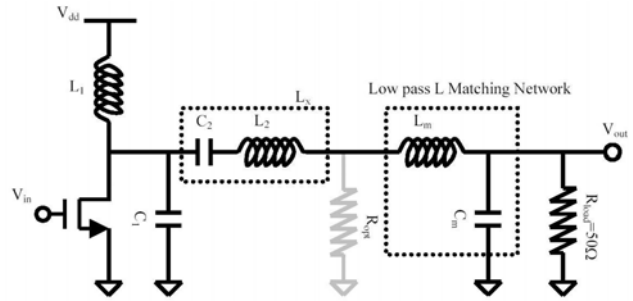

Fig.2. Class E power amplifier complete schematic.

The values of the matching network components L_m and C_m can be calculated using the following equations:

$$L_m = \frac{\sqrt{R_{opt}\left(R_L - R_{opt}\right)}}{\omega} \tag{5}$$

$$C_m = \frac{\sqrt{\left(R_L - R_{opt}\right)/ R_{opt}}}{R_L} \tag{6}.$$

Since the power amplifier is designed for class 1 Bluetooth application, the output power is 20dBm, 100mW. The target output power is designed to be 110mW to provide margin for some losses due to parasitics and the supply voltage is set to 1.5V. The parasitic capacitance associated with the transistor should be known before the calculation of L1. As a result, the size of the transistor should be designed first in order to find out the value of L1. It can be calculated by the current equation:

$$I_d = \frac{\mu C_{ox}}{2} \frac{W}{L} \left(V_{gs} - V_{th}\right)^2 \tag{7}$$

The parasitic capacitance drain-source per unit area is calculated by the following equation:

$$C_{ds(p.u.a.)} = \sqrt{\frac{q.k_s.\varepsilon_0.C_B}{2(V_{ds} + \phi_B)}} \quad (8)$$

where q is the elementary electronic charge, k_s is silicon dielectric constant, ε_0 is the permeability of free space, C_B is the epitaxial layer background concentration, V_{ds} is drain to source voltage, and ϕ_B the diode potential.

3. SIMULATION RESULTS

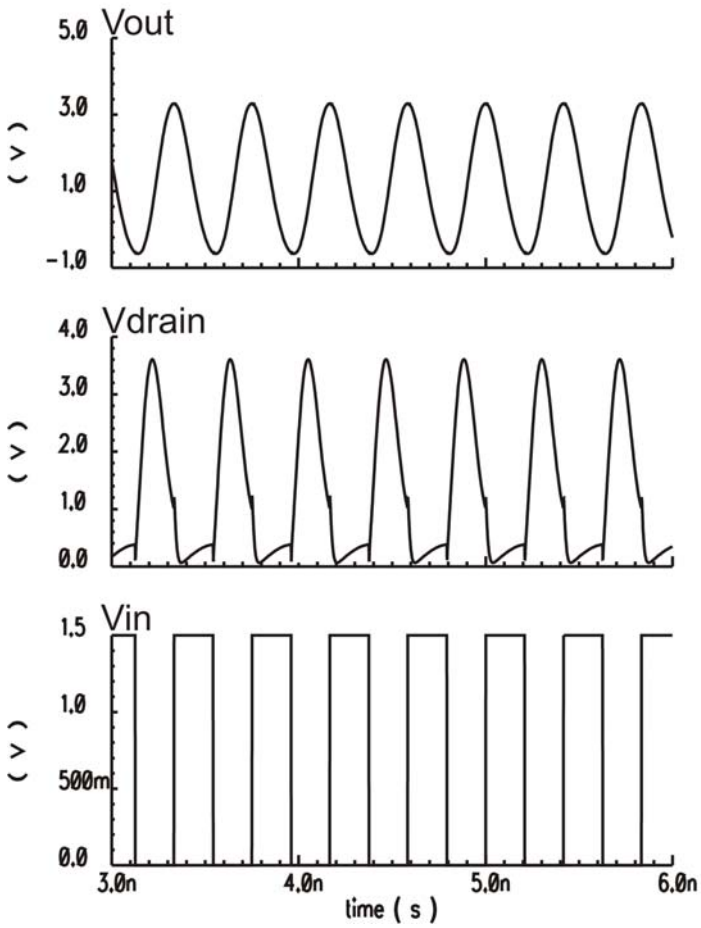

Fig.3. Simulated input and output characteristics..

The circuit is drawn in Virtuoso Schematic Composer for AMS 0.35μm CMOS technology using analogLib library for the ideal components (gnd, the load resistor, DC voltage (1.5V), V-pulse (1.5V)) and PrimLib library for the remaining real components and a RF transistor from the respective RF library. Using (7) and (8) we calculate the required parameter values. To achieve these values we have to utilize 200 RF transistors grouped in 20 cells of ten transistors in each cell. Circuit simulation was performed in Cadence Analog Design Environment. The results of the

Transient analysis are shown in Figure 3 (drain voltage = 3.6V and output voltage = 4.1 V @ frequency = 2.4 GHz. Additional data is provided in Table 1.

The results in the first row show high efficiency and output power because of the ideal inductors used. Second and third rows are show results for circuit with real inductors, and the differences observed are due to having examined the circuit before and after extraction. That is why the efficiency is lower (44,6 %).

Table 1. Results from transient simulation.

Scheme	η [%]	Distortion [dB]	2-nd harmonic [dB]	3-d harmonic [dB]	Output power [mW]		Number of transis-tors
					[mW]	[dBm]	
RF-Transistors & ideal inductors	71,6	-21,83	-38,98	-55,82	105,8	20.24	140
RF-Transistors & real inductors	68,7	-21,76	-38,98	-53,38	102,5	20.11	200
RF-Transistors & ideal inductors; extracted	44,6	-21,14	-34,82	-45,05	66,87	18.25	200

The layout is created with Cadence Virtuoso XL. First we have removed all ideal elements and created a cell view for the scheme. Than we implement the new scheme in Cadence Virtuoso XL. Next comes layout generation, where placement of elements is the bottleneck. The parasitic capacitances originating from the connections present compromise the circuit performance. This one of the reasons to have an output power of 18.25 dBm and not the desired 20 dBm value. The second reason to obtain lower efficiency is the layout was created using monolithic indictors.

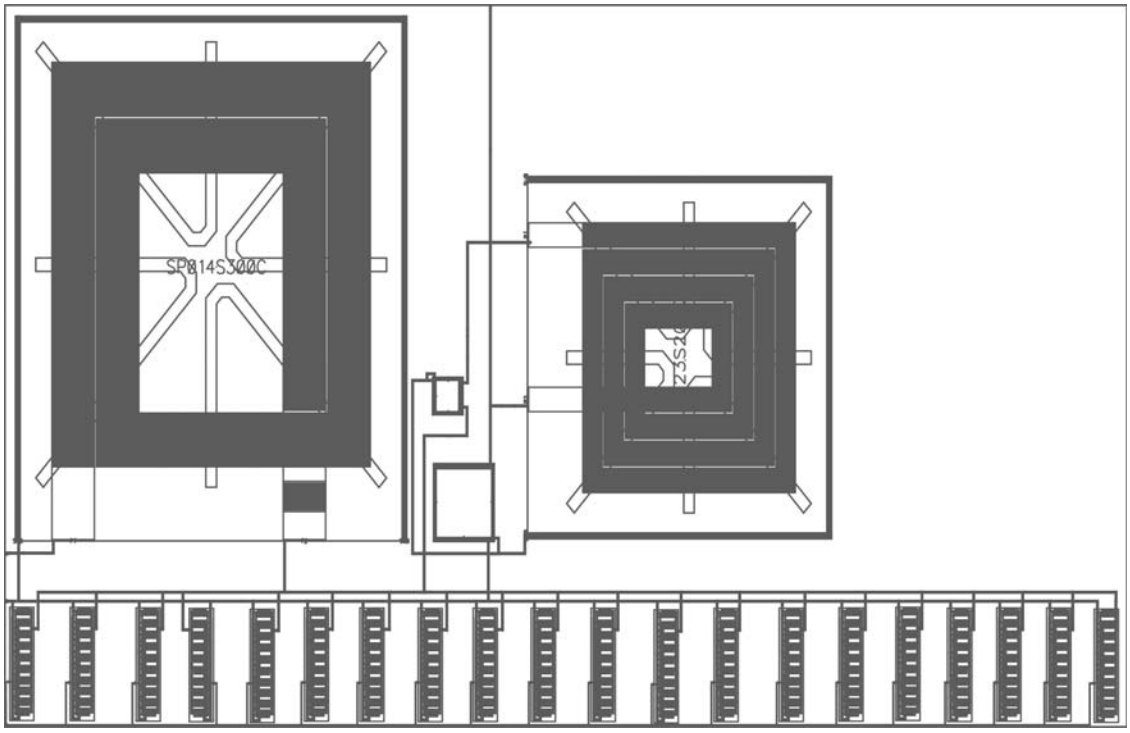

Fig.4. Layout of the scheme.

4. CONCLUSION

We have presented a Bluetooth class E power amplifier design in AMS 0.35μm CMOS technology. The required output power of 20 dBm at 1.5V power supply voltage was reached with 91 % accuracy — we have designed a class E PA with output power of 18.25 dBm. Providing simulation results for circuit with ideal elements we show that the lower output power is mainly due to the presence of parasitic capacitances in the interconnections.

5. REFERENCES

[1] Sokal N., A. Sokal, *Class E – A New Class of High-Efficiency, Tuned Single-Ended Switching Power Amplifier,* IEEE J. Solid-State Circuits, vol. Sc-10, no. 3, pp. 168-176, June 1975.

[2] Gupta R., B. M. Ballweber, D. J. Allstot, *Design and Optimization of CMOS RF Power Amplifiers*, IEEE J. Solid-State Circuits, vol. 36, no. 2, pp 166-175, Feb. 2001.

[3] Zulinski R. E., J. W. Steadman, *Class-E power amplifiers and frequency multipliers with finite dc feed inductance*, IEEE Transitions on Circuits and Systems, vol. CAS-34, no. 9, pp. 1074-1087, September 1987.