BUILDING BLOCKS FOR MODERN ACTIVE COMPONENTS DESIGN

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ABSTRACT: Special building blocks for the fast modular design of modern active devices specially developed for current mode signal processing have been developed in AMIS CMOS07 technology. They allows easy to create the circuits as CDTA [1] and CCTA [4] as well as many other functional blocks and structures by connecting various types of input and output stages to satisfy optimally an application demands. The blocks as the current conveyors, current amplifiers, transimpedance and transconductance stages and others are designed to create special IP library in CMOS technology.

The CMOS technology is preferably used by the reason of usage this technology in modern SoC designs to comply the digital circuits needs as the priority.

Keywords: Signal processing, current mode, modern active blocks

1. INTRODUCTION

The ever growing scale of integration and possibility to design and use low-power circuits leads to high popularity of SoC circuits, when almost all system is realized on a single chip. Mostly they are the hybrid mixed mode designs. Decreasing of the minimum silicon elements dimensions leads to dominant using of digital solution in the signal processing. It is caused by many advantages of the digital circuits against the analog ones, e.g. lower sensitivity for interference, noise or technology process changes.

With regard to the facts the main effort in technology research was pointed to the digital signal processing and many new technologies are optimized for digital circuits. In despite of there are some relevant reasons why analog circuits are still demanded. The main reason is that the real world is analog. Almost all signals are analog and they need some analog preprocessing before main digital processing. It means that the accuracy of full processing is mostly determined by quality of the analog circuits.

For SoC the digital and analog circuits as well must work in the same technology (mostly CMOS). It means the modern analog circuits are requested to work in "digital" low-power and low-voltage technologies. To satisfy high performance and accuracy of the analog circuits the new circuit principles have been developed as switched capacitors, switched currents and current mode as well. The design of the modern active analog devices by modular building blocks is introduced in this paper.

2. MODERN CURRENT MODE ACTIVE DEVICES

As the modern current mode devices we consider mainly such active devices like the COA (*Current Operational Amplifier*) [1], CDTA (*Current Differencing Transconductance amplifier*) [2] and CCTA (*Current Conveyor Transconductance*

amplifier) [4,5]. This work is focused to design of CDTA and CCTA, because the COA can be always reached by a convenient connection of CDTA or CCTA with "infinity" gain. The above mentioned circuits are mostly designed as two-stage (input-output) devices. It allows us to design the input and output stages as independent **modules** designed in consideration of simple mutual connection. Such a way designed blocks can be then simply combined to create CDTA, CCTA and many other possible devices with regards to desired performance parameters like power, speed accuracy etc.

2.1 CDTA short description

The CDTA has difference low-impedance current inputs p and n. The difference of input currents flows out of the z-terminal into an outside load. The voltage across the z-terminal is converted through a transconductance gm into a current that is generally led in a number of copies into the out-terminals. The transconductance can be either fixed or given by external component or controlled electronically from an auxiliary terminal as well.

2.2 CCTA short description

CCTA is designed for usage mostly in current mode circuits but it is also good choice in case of hybrid (voltage-current) circuits. The CCTA consists from two basic blocks. The first stage is represented by the current conveyor CCIII that is followed by double output transconductance "*gm"* stage. The input behavior is mostly given by properties of the CCIII conveyor. Conveyor output current flows out of the CCTA terminal "z" into an outside load. The voltage across the z-terminal is processed like in CDTA and it is converted through a transconductance gm into a two output currents with opposite polarity.

3. PRINCIPLE SCHEMATICS OF BUILDING MODULE EXAMPLES

As an example of the **input stages** the *current conveyor CCIII* and *current differencing stage* are shown in fig. 1,2 as the input stages of CCTA and CDTA respectively.

With tendency to fulfill various demands to **output stage**, more *output transconductance modules* can be designed. Some of them are introduced in fig. 3.

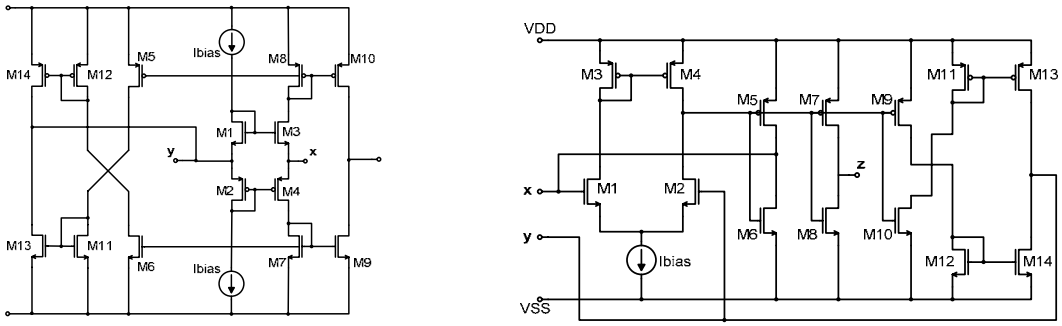


Fig. 1: a) CCIII based on current mirrors b) CCIII based on operational amplifier

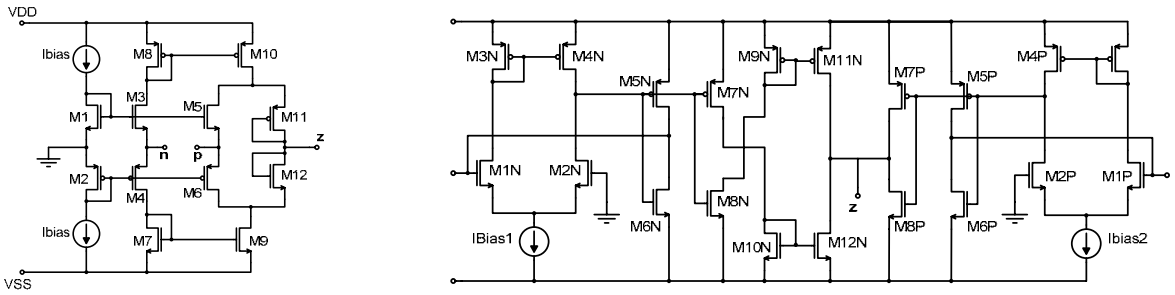


Fig. 2: Current differencing stage a) based on current mirrors
b) CCIII based on operational amplifier

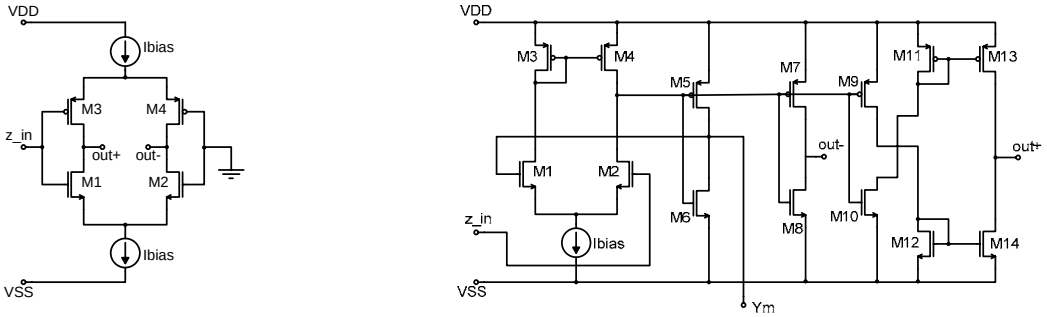
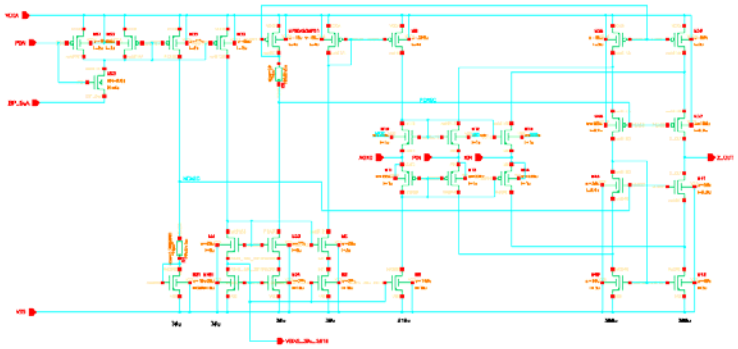


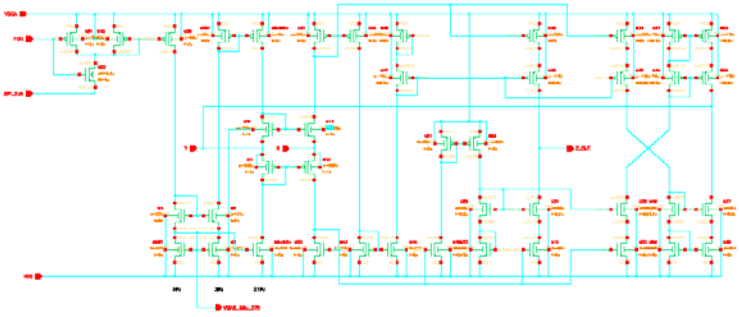
Fig. 3: a) Tranconductance stage with fixed gain
b) Tranconductance stage with *gm* gain controlled by external admittance connected to net Y_m

4. CDTA AND CCTA DESIGN IN CMOS07 TECHNOLOGY

The basic building blocks of the modern CDTA and CCTA circuits have been designed in AMIS CMOS07 technology based on the above mentioned principle schematics. This design was prepared for manufacture and currently is processed in foundry. The topologies were improved by the cascode connection to reach higher accuracy and output impedance. The Cadence schematic examples are shown in Fig.4. and simulated results can be seen in Table 1.



a)



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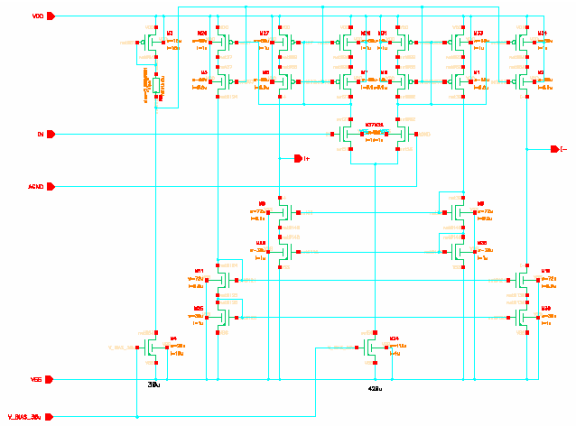


c)

Fig. 4: Cadence schematics of the modules designed in CMOS07
a) Current differencing stage based on current mirrors
b) CCIII based on current mirrors
c) Transconductance stage with fixed gm

Table 1: Simulated results of the designed blocks

	Supply Voltage V_{dd} = 5V, Max. processed current I_{max} = 200μA					
	V_{in} range (V_{pp})	V_{out} range (V_{pp})	Z_{in} (*I inputs*)	Z_{out}	Gain	BW(-3dB)/GBW
CCIII	1V	1V	160 Ω	3.5 MΩ	B_0 = 1	BW = 100MHz
Diff Iamp	1V	1V	220 Ω	5 MΩ	B_0 = 1	BW = 180MHz
Gm stage	400 mV	1V	∞	2.4 MΩ	*gm* = 1.1 mA/V	BW = 220 MHz
CCTA	1V	1V	160 Ω	2.4 MΩ	B_0 = 3800	GBW = 28 MHz
CDTA	1V	1V	220 Ω	2.4 MΩ	B_0 = 5500	GBW = 35 MHz

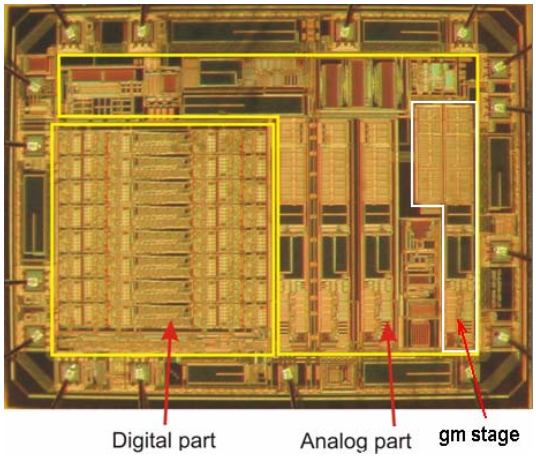
Note: a) BW(-3dB) is measured as the 3dB bandwidth when current outputs are connected to low impedance nets
b) GBW is introduced for compensated (stable) circuit with Phase Margin PM = 60 deg

5. CONCLUSION

Many types of building blocks and their topologies can be designed with this manner. Their combinations make large set of various active circuits working in voltage and/or current mode as well. At the beginning the above mentioned modern current mode devices has been prepared for chip prototype. Up to now only one of these blocks was manufactured. Just the external admittance controlled transconductance stage was designed in AMIS CMOS07 technology as a part of the measurement chain on chip for electrochemical sensor output signal processing. This circuit design was based on the rail-to-rail input stage opamp with AB class output (because of the lower consumption and current matching offset). Unfortunately it is impossible to measure all its parameters because of building this block into complete

system but results of full measuring chain are correct. The Cadence simulated results are introduced below as well as the photo of the chip.

GBW	1 MHz
Phase margin (PM)	63°
Systematic offset between I_{ref} a I_{out}	<1%
Matching offset between I_{ref} a I_{out}	4μA pro 4σ
Input voltage range V_{in}-range	VSS ÷ VDD
Output voltage range V_{out}-range	VSS+0.4V ÷ VDD-0.4V
Max. output current I_{outmax}	±1mA



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