METHODS FOR COMPUTING HARMONIC DISTORTION IN LOW FREQUENCY POWER AMPLIFIER

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This paper presents few different methods for computing the nonlinear distortion of an amplifier and compares each other, in order to find the simpler one that gives an acceptable precision. An approximate method for computing the amplifier distortion is introduced. The method is based on the five-point distortion analysis and allows the designer to identify the most important low frequency power amplifier elements from the distortion point of view. This method, implemented as an Excel spreadsheet, considers almost all the dependencies in the circuit and proposes some design strategies that reduces the total harmonic distortion factor.

Keywords: Harmonic Distortion, Power Amplifier.

1. INTRODUCTION

The harmonic distortion is one quality parameter of the amplifiers. To improve the THD factor, the power amplifier is studied in order to determine the modification that should be made in the design.

In this paper the three stages power amplifier was considered [3]. The driver stage, a large signal common emitter voltage amplifier, determines the nonlinear or harmonic distortions of the whole circuit, because the transconductance curve of the transistor is nonlinear for large signals. The negative feedback reduces significantly the THD.

Few different methods for computing the nonlinear distortion of the amplifier are presented and compared each other:

- the theoretical determination of harmonic distortion factor for the large signal common emitter stage, based on the exponential relationship between the collector current and the base-emitter voltage of the bipolar junction transistor (BJT);
- the five-point distortion analysis, developed by the author, used to determine the second, the third and the fourth harmonic distortion factor for a given wave shape;
- the Fourier analysis as part of the simulation process used to determine different harmonic distortion factors and the total harmonic distortion THD factor.

2. THE HARMONIC DISTORTION OF THE COMMON EMITTER STAGE

One of the simpler approaches is to estimate the harmonic distortion of the common emitter (CE) driver stage starting from the exponential characteristic of the BJT.

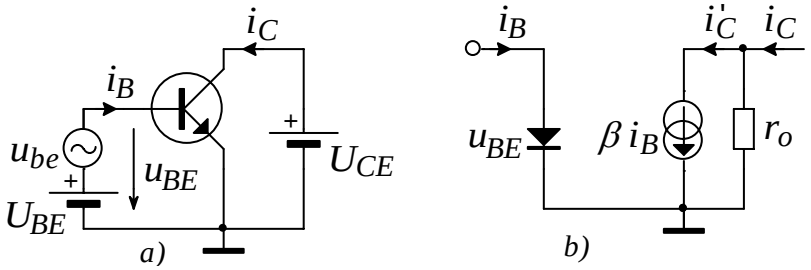

Fig.1. The simpler common-emitter stage for *npn* BJT.

For a sine input voltage with U_{BE_p} peak voltage, the BJT saturation current I_S, and the thermal voltage U_T (25 mV at 290 K), the exponential equation of the collector current can be approximated by keeping the first two terms of the Taylor series:

$$i_C = I_S \exp\frac{u_{BE}}{U_T} = I_C \exp\frac{u_{be}}{U_T} \cong I_C\left[1 + \frac{u_{be}}{U_T} + \frac{1}{2!}\left(\frac{u_{be}}{U_T}\right)^2\right] \tag{1}$$

Replacing the sine input voltage in (1), the second harmonic distortion factor of the collector current can be computed:

$$HD_2 = \frac{I_{c2}}{I_{c1}} = \frac{U_{be\_p}}{4 \cdot U_T} \tag{2}$$

If one considers the third term of the Taylor series, the 2nd and the 3rd harmonic distortion factors and the total harmonic distortion factor can be computed:

$$HD_2 = \frac{U_{be\_p}}{4 \cdot U_T} \frac{1}{1 + \frac{1}{8}\left(\frac{U_{be\_p}}{U_T}\right)^2}, \quad HD_3 = \frac{1}{24}\left(\frac{U_{be\_p}}{U_T}\right)^2 \frac{1}{1 + \frac{1}{8}\left(\frac{U_{be\_p}}{U_T}\right)^2} \tag{3}$$

$$THD \cong \sqrt{HD_2^2 + HD_3^2}\,. \tag{4}$$

The *THD* factor is slightly less than the *HD2* factor approximated by equation (2).

$$THD \cong HD_2 \cong \frac{U_{be\_p}}{4 \cdot U_T}. \tag{5}$$

One can see that this factor depends on the peak base-emitter voltage, and the result can be very simple expressed: The harmonic distortion factor in percent equals to the base-emitter voltage amplitude expressed in milivolts.

3. THE SIMPLER METHOD TO COMPUTE THE POWER AMPLIFIER DISTORTION

The procedure proposed to compute the THD factor for the power amplifier consists on the following steps:

- determine the driver stage current limits for the nominal output,
- compute the base-emitter voltage amplitude and the THD factor for the driver stage, this can be considered to be the distortion factor of the open loop amplifier,

- compute the amount of feedback and the distortion factor of the closed loop amplifier.

In order to keep the calculus simpler some approximations are considered:

- all the harmonics of the signal are considered to be in phase, that means all the capacitive effects are disregarded, the coupling and bypass capacitors are considered to be short-circuits and the internal capacitances of the transistors are neglected (considered to be open-circuits);
- all the harmonic distortion are considered to be introduced by the driver stage only, the preamplifier and the final stage distortion are neglected (theirs distortion being much lower);
- the simplified large signal π-hybrid model was considered for the transistors with its parameters determined in the same manner than for the small signal equivalent circuit, e.g. small variations around the peak value of the signal were considered.

The last approximation is not a usual one and it will be confirmed by simulation.

The limits for the driver stage current, I_{Cmax} and I_{Cmin}, are computed considering the peak values of the output voltage for the nominal power in the nominal load, [2]. The output voltage is considered to be a sine one because the THD factor for the closed-loop amplifier is reduced to a very low value by the feedback. To determine the driver input voltage limits the simplified schematics in figure 1*b)* can be used. The output resistance of the driver transistor is considered because the driver operates for large voltage variations.

From the driver stage equations:

$$i_C^{'} = I_S \exp\frac{u_{BE}}{U_T}, \quad r_o = \frac{U_A}{i_C} \tag{6}$$

with U_A being the transistor Early voltage, one can compute the internal current i'_C:

$$i_C^{'} = i_C - \frac{u_{CE}}{r_o} = \frac{i_C}{1+\frac{u_{CE}}{U_A}} \tag{7}$$

where u_{CE} is the driver output voltage.

The nominal base-emitter voltage amplitude can be derived from the internal current limits:

$$\frac{I_{C\max}^{'}}{I_{C\min}^{'}} = \exp\frac{\Delta u_{BE\max}}{U_T}, \tag{8}$$

$$U_{be\_p} \cong \frac{\Delta u_{BE\max}}{2} = \frac{U_T}{2}\ln\frac{I_{C\max}^{'}}{I_{C\min}^{'}}. \tag{9}$$

The result of (9) gaves the peak value of the nominal base-emitter voltage of the driver stage; equation (5) gave the THD factor of the driver current which can be considered to be the open-loop THD factor. The closed-loop amplifier THD factor is reduced by the amount of feedback:

$$THD_f = \frac{THD}{1+T} = \frac{THD}{1+ab}. \quad (10)$$

where T is the loop gain, a and b are the open-loop gain and the feedback factor, respectively.

In order to reduce the distortion factor some condition should be met:

- the maximum to minimum current ratio in the driver stage transistor should be reduced; for example if I_{Cmax} is twice I_{Cmin}, then from (9) the base-emitter voltage amplitude is 8.6 mV and from (5) the THD is 8.6% approximately;
- the amount of feedback should be increased, usually by increasing the open-loop gain, the feedback factor being imposed by the input and output project data.

The first condition can be fulfilled by increasing the bias current in the driver stage transistor; for a passive load the resistor in the transistor collector should be reduced. On the other hand greater the current greater the power dissipated in the transistor. A good compromise should be a *dc* current at least twice the minimum necessary.

Increasing the amount of feedback will enhance most of the parameters of the amplifier, including THD. In order to do this, the current gain in the final stage of the amplifier should be increased (by utilizing the Darlington transistors in the final stage) and the bootstrap configuration or of a current mirror should be utilized as a driver stage load; both these conduct to the increase of the driver load resistance and the driver stage voltage gain. On the other hand, a too great amount of feedback will reduce the stability of the whole amplifier and will be more difficult to compensate.

4. THE FIVE POINTS METHOD

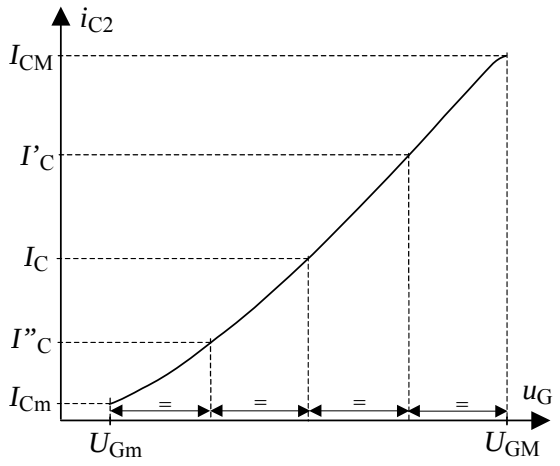

Fig.2. The transfer characteristics of the driver stage.

This method is based on the transfer characteristic $i_{C2} = f(u_G)$, i_{c2} is the driver transistor current and u_G is the input generator voltage. This characteristic is plotted considering few points for the nominal regime, points that should include the limits of the current. The precision of the characteristic increases with the number of points, but the calculus volume increases also. Seven points are the better choice, but at least five points can be used. The five points are given by the collector currents computed for load currents from $-I_{o\_p}$ to I_{o_p} in steps of $I_{o\_p}/3$.

The proposed method is based on harmonic analysis and utilizes the transfer characteristics. The U_{Gm} ... U_{GM} interval is divided in 4 equal parts. The 5 points on the axis gave 5 collector currents that will be labeled as in figure 2.

For a sine generator voltage:

$$u_g = U_{g\_p} \cos \omega t , \tag{11}$$

The phases for the 5 points are: -π/2, -π/4, 0, +π/2, +π/2 respectively. Considering the *dc* component, the fundamental and the first 3 harmonics of the signal, the driver transistor collector current is:

$$i_C = I_{C0} + I_{c1} \cos \omega t + I_{c2} \cos 2\omega t + I_{c3} \cos 3\omega t + I_{c4} \cos 4\omega t \tag{12}$$

Five equations can be write for the five phases that corresponds to the 5 points on the current axis. The 5 equations system is solved for the 5 harmonic components of the collector current. The results are:

$$\begin{aligned}
I_{c0} &= \frac{I_{CM} + I_{Cm} + 2 \cdot \left(I_C^{'} + I_C^{"} \right)}{6} \\
I_{c1} &= \frac{I_{CM} - I_{Cm} + I_C^{'} - I_C^{"}}{3} \\
I_{c2} &= \frac{0{,}5 \cdot \left(I_{CM} + I_{Cm} \right) - I_C}{2} \\
I_{c3} &= \frac{I_{CM} - I_{Cm} - 2 \cdot \left(I_C^{'} - I_C^{"} \right)}{6} \\
I_{c4} &= \frac{I_{CM} + I_{Cm} - 4 \cdot \left(I_C^{'} + I_C^{"} \right) + 6 \cdot I_C}{12}
\end{aligned} \tag{13}$$

With the harmonic components, the harmonic distortion factors can be determined:

$$DH_2 = \frac{I_{c2}}{I_{c1}}, \; DH_3 = \frac{I_{c3}}{I_{c1}}, \; DH_4 = \frac{I_{c4}}{I_{c1}} \tag{14}$$

To compute the closed loop distortion factors the previous results are divided by the amount of feedback. The amount of feedback is not a constant value, it depends on different factors such is the output signal level. The worst case analysis utilizes the minimum value T_m and the THD factor for the open-loop amplifier can be computed:

$$THD_f = \sqrt{\sum_{i=2}^{4} \left(\frac{DH_i}{1 + T_m} \right)} . \tag{15}$$

Based on this method an Excel workbook was developed for computing the distortion factors. Some of the formulas used to design the power amplifier are given in [3]. A print-shot of the worksheet is given in fig. 3.

The driver transfer characteristics plot can be seen in the down-left corner. On the right of this plot the harmonic distortion are computed with the proposed method for: the driver collector current, base current and the base-emitter voltage. The row labeled

δ(%) contains the result of the 5 point analysis. In the row labeled with δ2(%) the 3 points analysis results are computed; that method was not presented in this paper.

S22 =SQRT(S28*S28+S29*S29+S30*S30)

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X
1	NrLinPr	7																						
2	Pu	RL	Cd	UonM	Ucc	IonM	Io(m)	RE	TpTz	Cfg	Cfg1	βFvt	IiFM(m)	UB	UA	UBM	UAM	R7	R6	Ic2(m)	β2	R3	βBF0	R8
3	40	8	2.0	25.30	64.0	3.17	40	0.53	T2	2	0	6325	0.50	33.20	53.73	60.98	79.03	18047	9023	1.14	300	2295	6111	100
4						3.16								32.53	53.51									
5		UBE0	rB		Pi		UBE0	rB	RBE(k)				IR7(m)		0.33	UA2	UBE20(m)	rB2(k)	Rg(k)		β1		UBE10(m)	rB1(k)
6		0.5	1		3.1416		0.6	5	-				1.16			80	450	0.1	2.29		250		590	0.1
7																								
8	Io		β6	iB6(m)	UBE6	ic4(m)		β4	iB4(m)	UBE4														
9	iF		β7	iB7(m)	UEB7	ic5(m)	(BD1xx)	β5	iB5(m)	UEB5	iiF(m)	βF	iR7(m)	ic2(m)	β2	UCE2	iB2(μ)	UBE2(m)	UGe(m)	ic1(m)	β1	iB1(μ)	UBE1(m)	UB1e(m)
10	3.17	63.2	63.2	50.09	0.65	73.49	100.0	100	0.73	0.60	0.73	4307	1.05	0.32	274.8	58.39	0.67	439.7	441.3	0.19	218	0.88	586.9	593.07
12	1.58	126.4	126.4	12.52	0.58	26.75	88.9	89	0.30	0.57	0.30	5261	1.11	0.81	282.1	44.92	1.83	465.9	470.1	0.20	218	0.94	588.5	595.11
14	0.04	200.0	200.0	0.20	0.46	5.00	81.7	82	0.06	0.53	0.06	654	1.16	1.16	287.4	31.81	2.89	478.0	484.6	0.21	218	0.97	589.3	596.09
16	-1.58	101.1	101.1	15.65	0.59	21.53	87.2	87	0.25	0.56	-0.25	6409	1.21	1.45	291.8	17.94	4.07	487.0	496.3	0.22	218	0.99	589.9	596.87
18	-3.17	50.6	50.6	62.61	0.67	69.31	100.0	100	0.69	0.59	-0.69	4566	1.25	1.95	299.2	4.42	6.16	498.0	512.1	0.22	218	1.02	590.7	597.90
19																53.97		-58.3					-3.8	-4.83
20												Amplif.	în tens.	--->	-11178	-926		15.22						
21											δ2(%)	δa/2(%)	--->	1.77		0.76	9.59	15.60	11.12	11.12		11.18	12.89	12.52
22												δ(%)	--->	7.78		1.02	12.26	20.07	15.50	15.50		15.57	17.40	17.00
23												Fndm.	-->	0.76		-26.98	2.58	26.44	32.36	0.01		0.06	1.74	2.20
24												Arm2	--->	-0.01		-0.20	0.26	-4.54	-3.94	0.00		-0.01	-0.25	-0.30
25												Arm3	-->	0.05		0.00	0.17	2.69	3.08	0.00		0.01	0.17	0.22
26												Arm4	--->	0.02		0.19	0.05	-0.52	-0.41	0.00		0.00	-0.03	-0.03
27												Cmp.cc		1.13		31.42	3.11	473.93	481.05	0.21		0.96	589.04	595.82
28												δ2(%)	--->	1.90		0.76	10.21	17.18	12.18	12.18		12.24	14.18	13.76
29												δ3(%)	-->	7.24		0.01	6.52	10.18	9.51	9.51		9.53	9.97	9.87
30												δ4(%)	--->	2.12		0.69	1.88	1.96	1.25	1.25		1.27	1.59	1.52
31																								
32																								

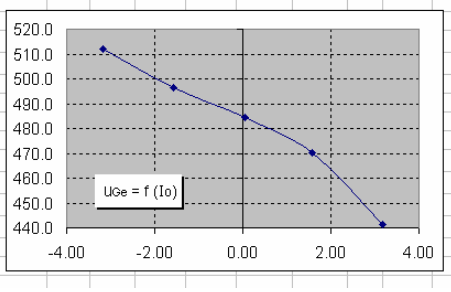

Fig. 3. The Excel workbook that computes the harmonic distortion (40 W / 8 ohm amplifier).

5. SIMULATION WITH SPICE

In order to validate the results of the proposed method, the SPICE simulation was used. Based on an example, the results were compared with the simulation results and the differences can be considered acceptable: the driver collector current distortions are: computed with the simplified method 18.5%, simulated 16% and computed with the 5 points analysis 12.3%.

The THD computed factor is less than 2% and the simulated one is 1.2%

6. CONCLUSIONS

This paper proposes an approximate method for computing the amplifier distortion. The method is based on the five-point distortion analysis and it allows the designer to identify the most important low frequency power amplifier elements from the distortion point of view. This method, implemented as an Excel spreadsheet, considers almost all the dependencies in the circuit and proposes some design strategies that reduces the total harmonic distortion factor.

7. REFERENCES

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