METHODOLOGY OF THE MULTI-MODE DIGITAL RECEIVER DESIGN BY USING CAD'S TOOLS

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The some ways of the wireless receivers design by using modern CAD tools are discussed. An effective definition of the most important parameters of obtained by using linear and nonlinear analysis are represented. The possibility of multistandard UHF direct-conversion receivers creation on the modern integrated circuits basis are shown.

Keywords: direct-conversion receiver, CAD's Tools, harmonic balance simulator, envelope simulator.

1. INTRODUCTION

There are following basic features of development of digital communication are observed now:

- using signals with the complex modulation forms,
- miniaturization of the receivers devices,
- power supply reduction,
- development of the digital signals processors (DSP) for multi-mode operation,
- creation of the RF, LF and digital blocks on the single-chip technologies basis.

To solve difficult scientific and technical problems is not possible now without using of the CAD's tools, which allow to decrease time and cost of the design process. In the presented paper the basic design steps of the universal UHF receiver with digitally QPSK-modulated signals, various bitrate (30 - 120 kBaud) and wide radio-frequency band are considered. The design process has been realized as sequence of the steps by using Advanced Design System (ADS) from Agilent Technologies:

1. A choice of receiver structure and the basic RF, LF and digital integrated circuits.
2. Creation and definition of linear and nonlinear models of the basic RF and LF blocks.
3. Simulation by using of the small-signal analysis in frequency domain.
4. Simulation by using nonlinear steady-state analysis (harmonic balance methods) in the frequency domain.
5. Simulations of the RF, LF and DSP circuits in the time domain by using envelope methods with modulated sources on RF input and bit error rate definition.

2. DESIGN STEPS

2.1. A choice of receiver structure

During design process the architecture of direct conversion receiver (DCR) has been chosen. These receivers allow to solve effectively a problem of reception of digital signals with various types of modulation and speed of data transmission. There are following features of DCR structure: exception of a problem of a image frequency rejection, necessity of using only one local oscillator, that minimizes quantity of sources of phase noise, very low supply current and dimensions.

2.2 Linear and nonlinear models of the basic RF and LF blocks definition

At designing of UHF-receiver it has been used the RF, LF and digital integrated circuits from famous vendors. These basic components were represented in the form of linear and nonlinear functional blocks. The network of analog paths of DCR is shown on fig. 1 [1].

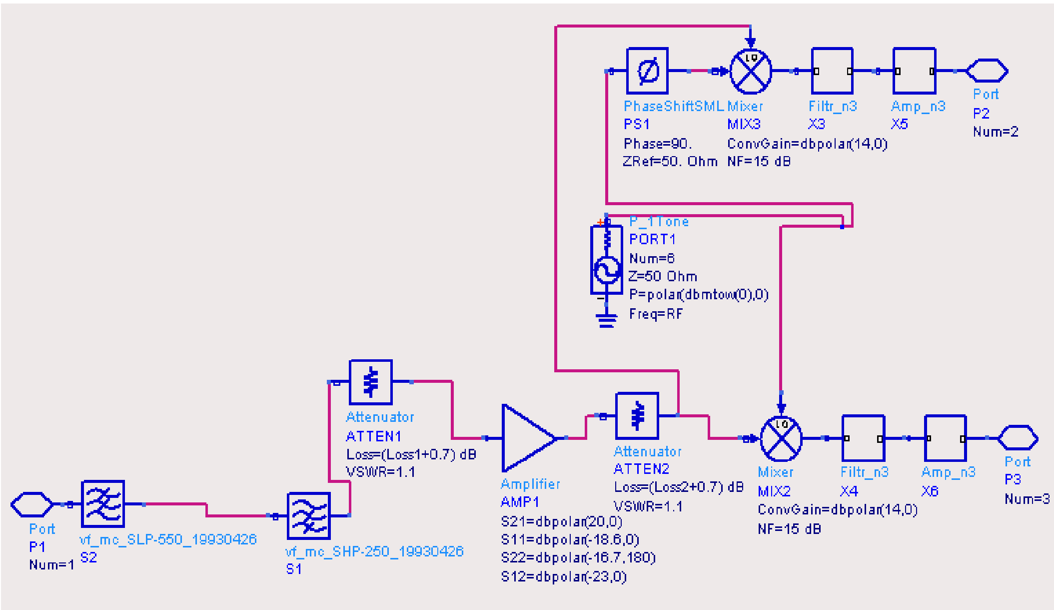

Fig. 1 Model of UHF-receiver in ADS Schematic

The brief description of receivers model is given below. Low pass and high pass frequency filters included on an input (denoted as *S2* and *S1*) completely correspond on parameters to Mini-Circuits components (SLP-550, PHP-250) and provide allocation of the useful frequencies in a range at 300 to 500 MHz. Low noise amplifier (*AMP1*) was defined in conformity with following data on device SGA-2486 from Sirenza: power compression point on output - *P1db* = 8,5 dBm, 3-rd order intercept point on output - *OIP3*=20 dBm, noise factor - *NF*=2,7 dB, power gain - *G*=20 dB. Elements *ATTEN1*, *ATTEN2* reflect the work of attenuators HRF-AT4511 from Honeywell with forward attenuation varying in a range from 0,7 to 15 dB everyone. The function chart analog I-Q- demodulator RF2721 from RF Micro Devices was modelled by inclusion of phase-shifting part PS1 and two frequency mixers (*MIX3, MIX2*) with following parameters: conversion gain *G*=14 dB, *NF*=15 dB, *OIP3*=10 dBm, 2-rd order intercept point on output - *OIP2*=30 dBm.

Macromodels *X3, X4* includes in itself baseband analog low pass filters of the bottom frequencies realized on low-noise operational amplifiers OP484, AD8606 from Analog Devices. At model definition of the most important parameters including linear, nonlinear and noise properties have been considered.

2.3 Simulation by using of the small-signal analysis in frequency domain

During this step of design small-signal simulation methods in frequency domain have been used and accuracy of the received results was defined by adequacy of the set parameters of the component models in a considered frequency range. The primary goals which have been solved at this stage are following: verification of characteristics of the library models, definition magnitude- and phase-frequency characteristics (*MFC* and *PFC*) and noise factor of a radio-frequency path of receiver; the baseband filters parameters optimization and the necessary gain in low-frequency IQ-paths definition. From the calculated frequency characteristics of the RF filters it has been established, that losses on the central frequency is equal to 1,5 dB and increased up to 2,0 dB to edges of the frequency range, and frequency dependence of group time delay was practically uniform - its hits were observed far outside a passband. From the most important parameters of the active low-pass filters realizing Chebyshev's transfer function on the base of the 4 operational amplifiers was defined, as it is shown on fig. 2. Non-uniformity in a passband equal to 60 kHz has not exceeded value 0,5 dB, and rejection on frequency of the adjanced channel at bias equal 800 kHz has been received not less than 90 dB.

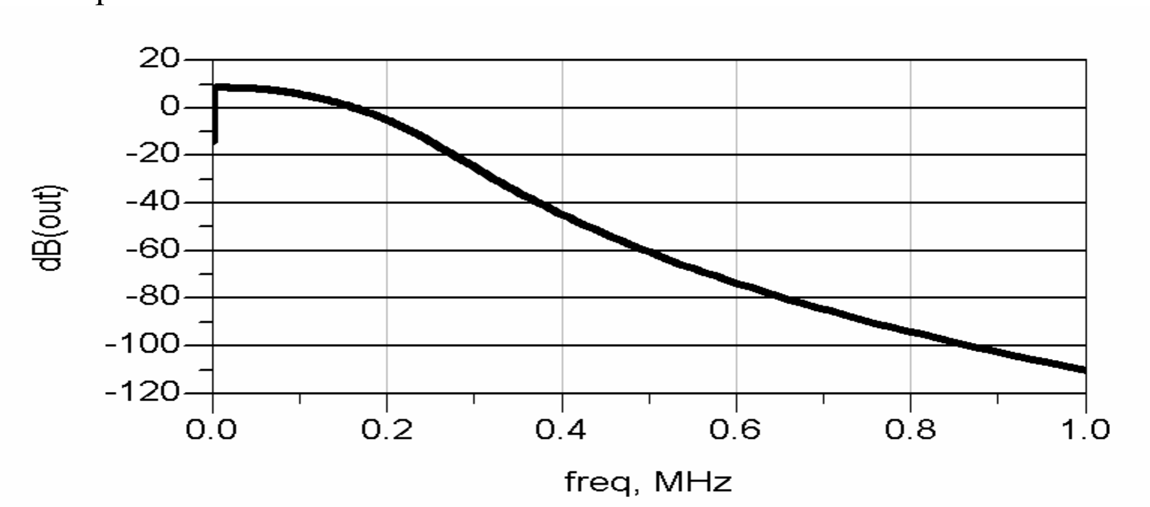

Fig. 2 Transfer function of the active filter

2.4 Simulation by using of the nonlinear steady-state analysis (harmonic balance methods) in the frequency domain

This step of design included application of nonlinear simulation methods. The given stage has been executed, mainly, by using of harmonic balance (HB) methodes [2] which is widely used recently in modern CAD's system for the spectral analysis of nonlinear circuits. Below the list of the primary goals which have been solved with application of the given method is resulted: total estimation of dynamic characteristics; an estimation of such nonlinear parameters as *P1dB, OIP2, OIP3* ; an estimation *MFC, PFC, NF* with the strong RF-signals levels; an estimation of influence of passing of parasitic signals in the different paths of receiver; primary estimation of the adjanced channel selectivity, co-channel rejection and blocking immunity; definition of the signal-noise relation (*SNR*) on analog I-Q-outputs necessary for designing of the digital demodulator.

For research dynamic and spectral properties frequency of input signal has been chosen equal central frequency of RF band of the receiver plus bias equal 10 kHz to prevent influence of DC blocking effect appearing at zero intermediate frequency. The local oscillator frequency has been accepted equal input carrier frequency. Calculation was fulfilled at the account of 4 harmonics on signal and local oscillator frequencies. In view of the large dimension of a solved problem on iterations of the HB method , the Krylov-subspace method [2] has been used. Results of calculation of a voltage on I-Q- outputs at change of input signal power from -120 dBm up to -20 dBm are shown on fig. 3. At carrying out of modelling inclusion of 3 cascades of automatic gain control which was provided with change of factors of easing in high-frequency attenuators and resistance of a feedback in operational amplifiers was considered.

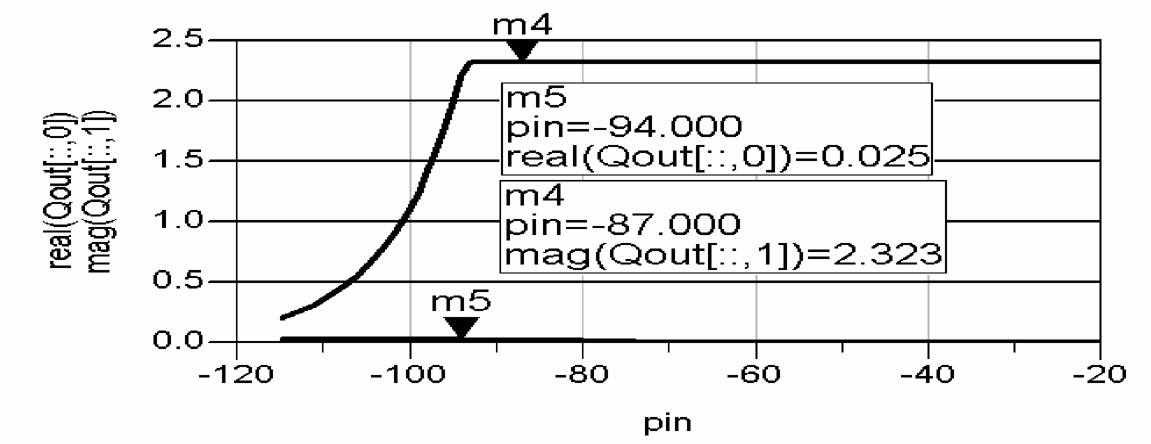

Fig. 3 Estimation of signal level and DC voltage on output

From results of the analysis it is visible, that the amplitude of a pressure on output frequency 10 kHz has been defined equal 2,3 V (see marker *m4*), that satisfies to optimum operating modes of channel analog-digital converters on an input of the digital demodulator. On behaviour of dependence of DC output voltage level (see marker *m5*) it is possible to make a conclusion, that it does not exceed value 25 mV (nearly 1 % of signal amplitude), that as have shown the further simulations it has appeared quite enough for qualitative demodulation of a digital signal with value of a bit error rate (*BER*) equal to 0,001. Calculation of the total noise factor was fulfilled in a nonlinear mode at the fixed power of an input signal (-80 dBm) in RF frequency range. Its value has not exceeded value 6 dB and in the further has been used for the approached estimation of sensitivity. At an estimation of the noise characteristics contributions of all functional blocks, active resistance, operational amplifiers, and also phase noise to the local oscillator have been considered. For the approached estimation of selectivity has been prepared network for modelling for 2 frequency input operation. The quantity of considered harmonics on in HB method has been chosen, equal to 3. As a result of selectivity on adjanced channel (offset from carrier frequency of signal - 800 kHz) equal to 72 dB has been received. Co-channel selectivity on the frequencies corresponding subharmonics and harmonics of the local oscillator frequency has not exceeded value 80 dB.

2.5 Simulations of the RF, LF and DSP circuits in the time domain

The basic methods of carrying out of researches РПУ at the given design step were the forward methods of numerical integration of the circuit nonlinear equations in the time domain and Envelope method for effective simulation circuits with modulated input signal [2]. The network for an estimation of *BER* value is shown on fig. 4.

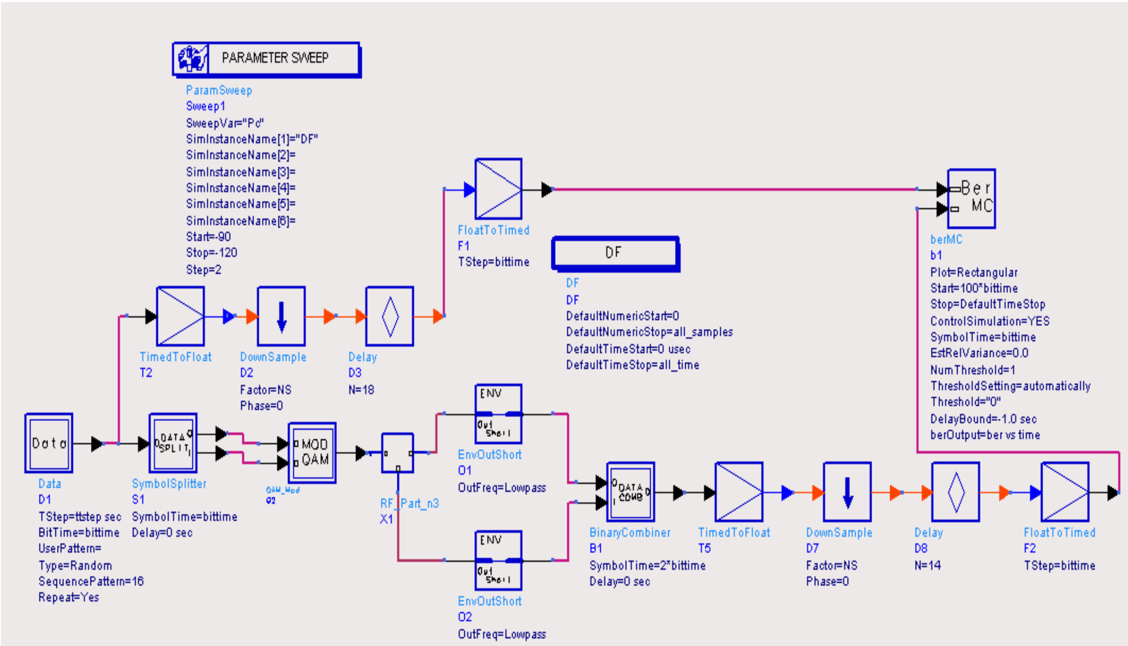

Fig. 4 Model for *BER* estimation

Following functional blocks have been included in total model of receiver: source of the modulated signal, subcircuit of an analog part of the receiver (fig. 1), the digital QPSK demodulator with analog-digital converters on inputs, the block of comparison of input and output bit streams and *BER* calculation. Gere's method with the included option of the noise analysis was used for simulations. The quantity of considered harmonics on frequency of a signal and local oscillator for HB method as part of Envelope simulator has been established equal to 3, that has appeared quite sufficient for maintenance of convergence of the decision at greater levels of input signal power.

From fulfilled simulations following values of sensitivity for control level BER equal to 0,001 were received: -100 dBm, -104 dBm and -108 dBm for bits stream speads equal to 120 kBaud, 60 kBaud and 30 kBaud respectively.

3. CONCLUSION

By results of the executed design stages of direct-conversion receiver (with RF band from 300 MHz to 500 MHz) has been fabricated on the basis of integrated circuits produced by using of the modern microelectronic technologies. This receiver is very adaptive to various speeds of the digital signals. The universal digital demodulator of the baseband section has been realized on a basis of programmable logic integrated circuit XC2V250 from Xilinx. Comparison of experimental and simulations results have shown a high efficiency of the used design steps. For example, the error of the sensitivity definition did not exceed value 1 - 2 dB.

4. REFERENCES

[1] HP Advanced Design System. User's Guide, HP Part No. E8900-90078, January, 1999.

[2] Kundert K. Introduction to RF Simulation and Its Application//IEEE Journal of Solid-State Circuits. – 1999. – Vol. 34, No 9. – P. 1298 – 1319.