# PARAMETERIZED TOLERANCE MODELS OF SWITCHED-CAPACITOR CIRCUITS

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*In the present paper, parameterized models are developed for tolerance analysis of SC-circuits using standard PSpice-like circuit simulators. They allow the assessment of the design component tolerances using Monte Carlo and Worst Case analyses. The tolerance models of the capacitor and operational amplifier are based on multiphase models in the z-domain and are realized in the form of multiport subcircuits. The tolerances are defined as model parameters. The description of the models is given in correspondence with the input language of the PSpice simulator. The tolerance field due to the design element tolerances and the histograms of the output characteristics are obtained in the graphical analyzer Probe. The developed models are verified using test examples.*

**Keywords:** tolerance analysis, parameterized PSpice models, SC-circuits

## 1. INTRODUCTION

Switched-capacitor (*SC*) circuits are widely used in many signal processing applications in telecommunication systems. The growing demand for portable and wireless electronic systems requires the design of analog-discrete circuits with a high degree of integration. The design and optimization of high-precision *SC*-filters is based on CAD products for simulation taking into account the real parameters of the circuit elements [1,2]. The tolerance analysis gives the possibility for comparison of different structures with respect to sensitivity [3], non-faulty limits investigation of test quantities in the *SC*-circuit diagnosis [3], etc.

In the present paper, parameterized models are developed for tolerance analysis of *SC*-circuits using standard *PSpice*-like circuit simulators. They allow the assessment of the design component tolerances using Monte Carlo and Worst Case analyses. The tolerance models of the capacitor and operational amplifier are based on multiphase models in the *z*-domain and are realized in the form of multiport subcircuits. The description of the models is given in correspondence with the input language of the *PSpice* simulator.

## 2. PARAMETERIZED MODELS OF CAPACITORS FOR TOLERANCE ANALYSIS OF SC-CIRCUITS

The equations describing the two-phase capacitor model in the *z*-domain for *SC*-circuit analysis have the form [1]:

$$I_1 = C\left(V_1 - z^{-1/2}V_2\right)\ ;\ I_2 = C\left(V_2 - z^{-1/2}V_1\right)\,. \tag{1}$$

The corresponding model is shown in Fig. 1 [1]. The model parameters are the commutation frequency $F_C$ and the capacitance value $C$. Based on this equivalent circuit, the parameterized *PSpice* model for the analysis in the frequency domain is in the form [2]:

```
.SUBCKT SC2_C A1 A2 B1 B2 PARAMS: FC=1k C=1nF
G_G1  B2 A2 LAPLACE {V(A1,B1)} {C*exp(-s/(2*FC))}
R_R1  B2 A2  {1/C}
R_R2  B1 A1  {1/C}
G_G2  B1 A1 LAPLACE {V(A2,B2)} {C*exp(-s/(2*FC))}
.ENDS
```

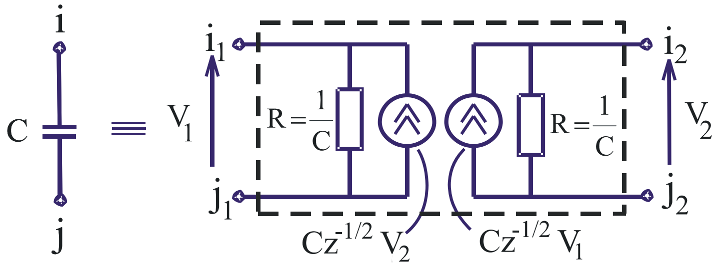



Fig. 1

The tolerance *SC*-circuit models are developed taking into account the following specificities:

1. The values of 2*N* model elements depend on the parameter *C*, where *N* is the number of phases. The tolerance $\varepsilon_C\%$ has to be assigned to each of the these elements;

2. When constructing the tolerance models, the limitations of the input language of the *PSpice* simulator have to be taken into account: design tolerances can be defined on passive elements (*R, L, C*) but not on dependent sources;

3. The tolerances of the elements in the capacitor model depending on the parameter *C* are to be defined in the mode of simultaneous variation as they correspond to the same circuit component – capacitor element. For this purpose the tolerances have to be assigned using the LOT mode in the .MODEL statement;

4. The value *C* and the corresponding tolerance $\pm\varepsilon_C\%$ of each *SC*-capacitor have to be defined as parameters, accessible for changing by the user.

The equations describing the two-phase capacitor model in the *z*-domain for *SC*-circuit tolerance analysis have the form:

$$I_1 = C(1\pm\varepsilon_C)\left(V_1 - z^{-1/2}V_2\right)\ ;\ I_2 = C(1\pm\varepsilon_C)\left(V_2 - z^{-1/2}V_1\right). \tag{2}$$

The corresponding two-phase model is shown in Fig. 2, where:

$I_{1a} = \left(V_1 - z^{-1/2}V_2\right)$ ; $I_{2a} = \left(V_2 - z^{-1/2}V_1\right)$ ; $R_{tol1} = R_{tol2} = 1\Omega \pm 1\%$ ; $R_{m1} = R_{m2} = -1\Omega$.

As a result:

$$\begin{aligned} I_1 &= C(V_{1a} \pm \varepsilon_C V_{1b}) = C(1\pm\varepsilon_C)\left(V_1 - z^{-1/2}V_2\right) \\ I_2 &= C(V_{2a} \pm \varepsilon_C V_{2b}) = C(1\pm\varepsilon_C)\left(V_2 - z^{-1/2}V_1\right). \end{aligned} \tag{3}$$

The elements $R_{tol1}$ and $R_{tol2}$, defined in the mode of simultaneous variation for satisfying the requirements 2 and 3, model a tolerance of $\pm1\%$ for the capacitance. The mode LOT in the .MODEL statement is used for this purpose in the form [5,6]:

.MODEL RLOT RES(R=1 LOT/GAUSS 1%)

The parameter $C$ and the corresponding tolerance $\pm\varepsilon_C\%$ are included in the description of the dependent sources $I_1$ and $I_2$ thus satisfying the requirement 4.

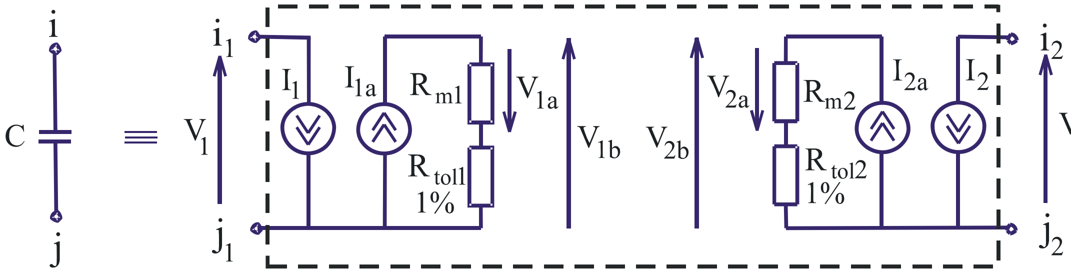



Fig. 2

The description of the corresponding parameterized *PSpice* model for the tolerance analysis in the frequency domain is in the form:

```
.SUBCKT SC2_C_TOL i1 i2 j1 j2 PARAMS: Fc=1k C=1nF  TOL={TOL}
G_G1a    A1a j1 LAPLACE {V(i2,j2)} {exp(-s/(2*Fc))}
G_G1b    j1 A1a i1 j1  1
R1       A1b j1 Rlot 1
R1m      A1a A1b -1
G_G1     i1 j1 VALUE {(V(A1a,j1)*TOL+V(A1b,A1a))*C}
G_G2a    A2a j2 LAPLACE {V(i1,j1)} {exp(-s/(2*Fc))}
G_G2b    j2 A2a i2 j2 1
R2       A2b j2 Rlot 1
R2m      A2a A2b -1
G_G2     i2 j2 VALUE {(V(A2a,j2)*TOL+V(A2b,A2a))*C}
.MODEL RLOT RES(R=1 LOT/GAUSS 1%)
.ENDS
```

The model parameters are the commutation frequency $F_C$, the capacitor value $C$ and the tolerance TOL.

## 3. Parameterized Models of Operational Amplifiers for Tolerance Analysis of SC-Circuits

The equations, describing the OpAmp model for two-phase *SC*-circuit analysis, taking into account the finite value of the open-loop DC gain $A_0$, have the form:

$$V_{out1} = A_0.V_{in1} \;\; ; \;\; V_{out2} = A_0.V_{in2}. \tag{4}$$

The model is presented in Fig. 3. The model parameter is the gain $A_0$. The description of the corresponding *PSpice* model has the form:

```
.SUBCKT SC2_OPAMP0 j1 j2 i1 i2 k1 k2  PARAMS:A0=100E3
E_E4  k2 0 VALUE {A0*V(j2,i2)}
E_E3  k1 0 VALUE {A0*V(j1,i1)}
.ENDS
```

The equations, describing the OpAmp model for the two-phase *SC*-circuit tolerance analysis, have the form:

$$V_{out1} = A_0(1\pm\varepsilon_A).V_{in1} \;\; ; \;\; V_{out2} = A_0(1\pm\varepsilon_A).V_{in2}. \tag{5}$$

The development of the tolerance SC-OpAmp model is accomplished, satisfying the same requirements as for the capacitor model. The realization of the two-phase model is presented in Fig. 4, where:

$$I_{1a} = 1.V_{in1} \;\; ; \;\; I_{2a} = 1.V_{in2} \quad R_{tol1} = R_{tol2} = 1\Omega \pm 1\% \; ; \; R_{m1} = R_{m2} = -1\Omega.$$

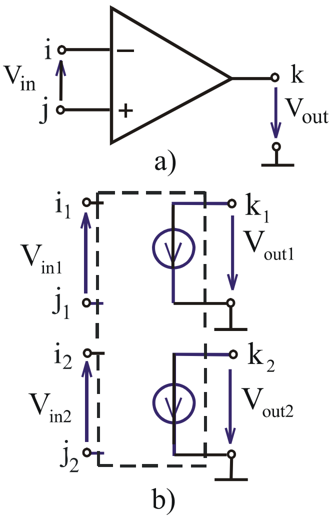


Fig. 3

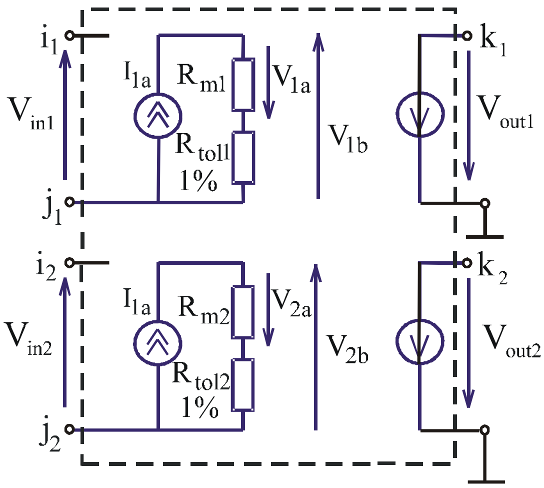


Fig. 4

Hence

$$V_{out1} = A_0\left(V_{1a} \pm \varepsilon_A V_{1b}\right) = A_0\left(1 \pm \varepsilon_A\right).V_{in1}$$
$$V_{out2} = A_0\left(V_{2a} \pm \varepsilon_A V_{2b}\right) = A_0\left(1 \pm \varepsilon_A\right).V_{in2} \; . \qquad (6)$$

The elements $R_{tol1}$ and $R_{tol2}$, defined in the mode of simultaneous variation for satisfying the requirements 2 and 3, model a tolerance of $\pm 1\%$ for the gain. The LOT mode in the .MODEL statement is used for this purpose in the form:

```
.MODEL RLOT RES(R=1 LOT/GAUSS 1%)
```

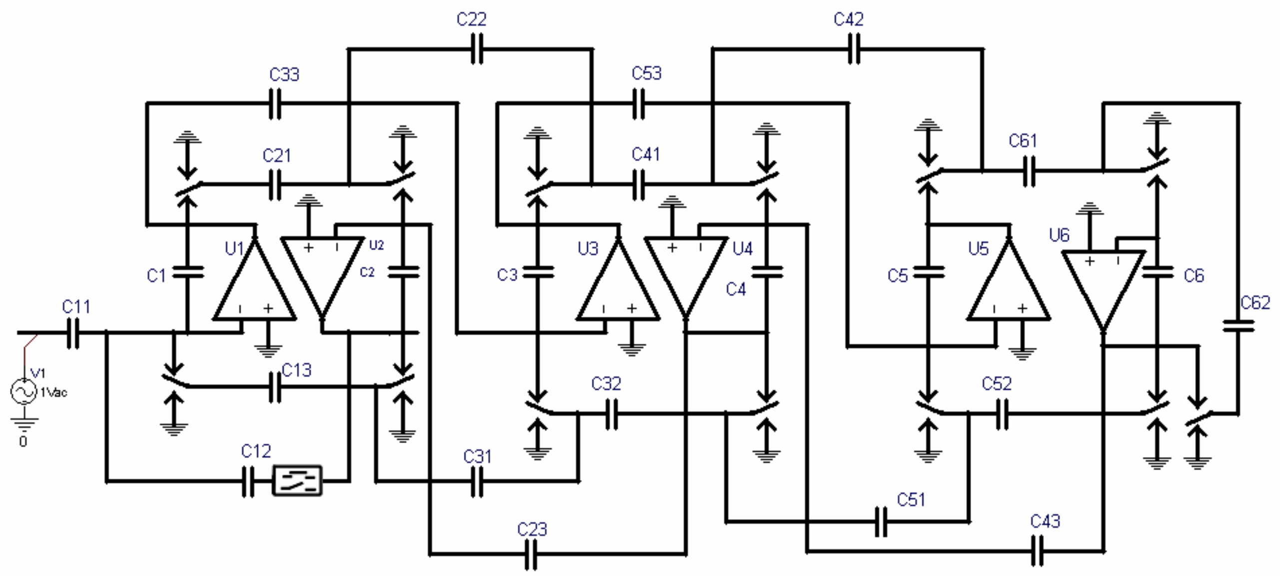
The model parameter $A_0$ and the corresponding tolerance $\pm \varepsilon_A\%$ are included in the description of the dependent sources $V_{out1}$ and $V_{out2}$, thus satisfying the requirement 4. The corresponding parameterized *PSpice* model for the tolerance analysis in the frequency domain is in the form:

```
.SUBCKT SC2_OPAMP_TOL j1 j2 i1 i2 k1 k2 PARAMS:A0=1k TOLA={TOLA}
G_1  j1 A1a j1 i1 1
R1   j1 A1b RLOT 1
R1m  A1a A1b -1
E_E1 k1 0 VALUE {(V(A1a,j1)*TOLA+V(A1b,A1a))*A0}
G_2  j2 A2a j2 i2 1
R2   j2 A2b Rlot 1
R2m  A2a A2b -1
E_E2 k2 0 VALUE {(V(A2a,j2)*TOLA+V(A2b,A2a))*A0}
.MODEL RLOT RES(R=1 LOT/GAUSS 1%)
.ENDS
```

The model parameters are the gain $A_0$ and the corresponding tolerance TOLA.

## 4. EXAMPLE

The application of the developed parameterized models of the *SC*-elements is illustrated by tolerance analysis in the frequency domain of the band-pass *SC*-filter of 6-th order, shown in Fig. 5. The design tolerances of the components are $\varepsilon_C\% = 1\%$ and $\varepsilon_A\% = 20\%$ with Gaussian statistical distribution. The magnitude response of the nominal circuit is shown in Fig. 6 and the detailed characteristic in the passband is presented in Fig. 7.




| | | | | |
|---|---|---|---|---|
| $C_1$ = 87.10 pF | $C_{21}$ = 11.9 pF | $C_{32}$ = 11.51 pF | $C_{43}$ = 3.67 pF | $C_6$ = 68.26 pF |
| $C_{11}$ = 84.20 pF | $C_{22}$ = 16.7 pF | $C_{33}$ = 7.48 pF | $C_5$ = 87.1 pF | $C_{61}$ = 18.0 pF |
| $C_{12}$ = 72.17 pF | $C_{23}$ = 22.26 pF | $C_4$ = 87.1 pF | $C_{51}$ = 17.03 pF | $C_{62}$ = 9.75 pF |
| $C_{13}$ = 1.0 pF | $C_3$ = 87.1 pF | $C_{41}$ = 13.04 pF | $C_{52}$ = 8.73 pF | $C_{62}$ = 9.75 pF |
| $C_2$ = 71.01 pF | $C_{31}$ = 9.53 pF | $C_{42}$ = 7.81 pF | $C_{53}$ = 25.39 pF | $A_0 = 100 \times 10^3$ |

Fig. 5

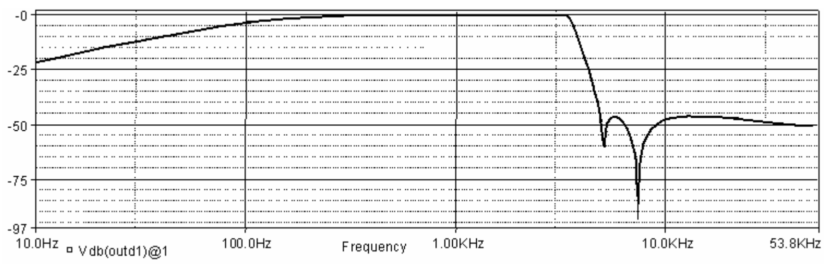



Fig. 6

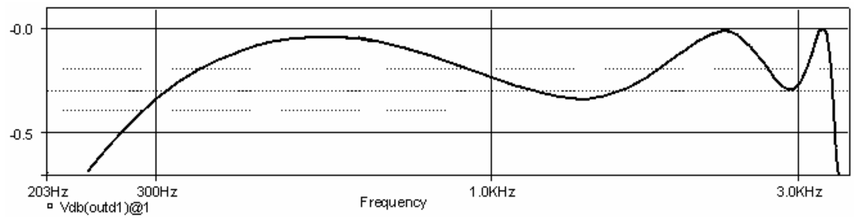



Fig. 7

The results for the circuit with tolerances, obtained using Monte Carlo analysis, are presented in Fig. 8 and Fig. 9 respectively. The histogram of the filter bandwidth is shown in Fig. 10.

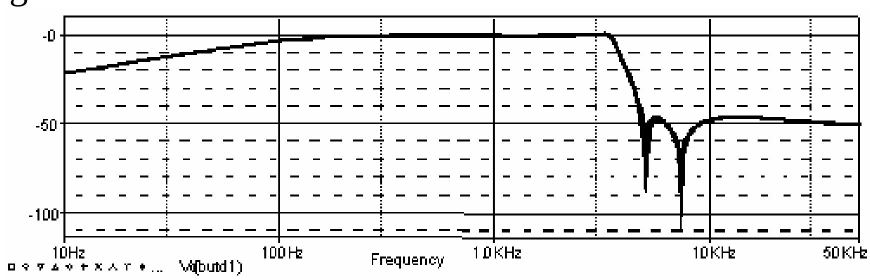



Fig. 8

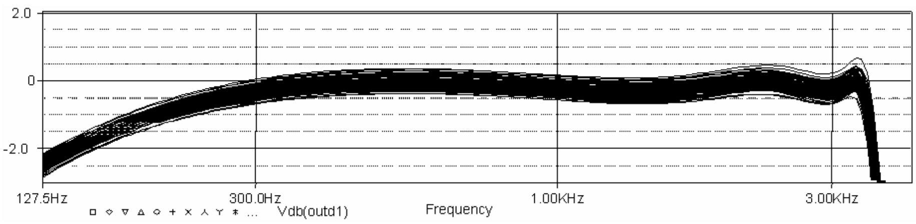



Fig. 9

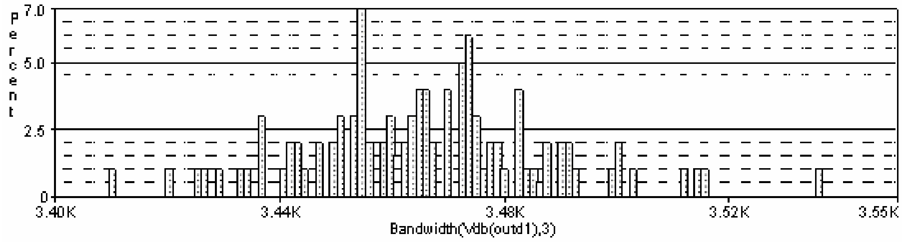



Fig. 10

The developed *PSpice* models are also applicable to Worst Case tolerance analysis. The results for the limits of the design tolerance bound of the magnitude characteristics in the passband are shown in Fig. 11.

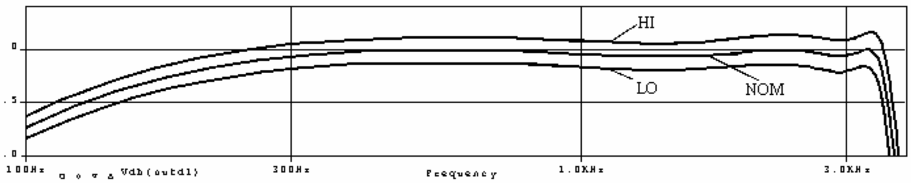



Fig. 11

## 5. CONCLUSIONS

Parameterized models for tolerance analysis using general-purpose circuit simulators are developed for the building blocks of *SC*-circuit elements. The description of the equivalent circuits is given in accordance with the input language of the *PSpice* simulator. The tolerance field of the output characteristics due to the design element tolerances is obtained in the graphical analyzer Probe using Monte Carlo and Worst Case analyses.

## 2. REFERENCES

[1] Liou, Y., M. Kuo, J. Kasinskas, *Exact Analysis of Switched-Capacitor Circuits with Arbitrary Inputs*, IEEE Trans. on Circuits and Circuits, vol. CAS-26, No. 4, 1979, pp.213-223.

[2] Farchy, S., E. Gadzheva, T. Kouyoumdjiev, Switched-Capacitor and Digital Circuits Modelling Using General Purpose Analysis Programs, 39 Intern. Wissencshaftliches Kolloquium – Informatik und Automatisierung, 27-30 Sept. 1994, S. 80-85.

[3] Yuan, F., A. Opal, Noise and Sensitivity Analysis of Periodically Switched Linear Circuits in Frequency Domain, IEEE Trans. on Circuits and Circuits – I. Fundamental Theory and Applications, vol. CAS-47, No. 7, July 2000, pp. 986-998.

[4] Farchy, S., E. Gadzheva, L. Raykovska, T. Kouyoumdjiev, *Nullator-Norator Approach to Analog Circuit Diagnosis*, International Journal of Circuit Theory and Applications, John Wiley and Sons, Ltd., vol.23, pp. 571-585, 1995.

[5] *PSpice Reference Guide*, Cadence PCB Systems Division, USA, 2000.

[6] *PSpice User's Guide*, Cadence PCB Systems Division, USA, 2000.