# ECONOMETRIC MODEL OF USING THE DESIGN-FOR-TESTABILITY APPROACH FOR MIXED-SIGNAL ELECTRONIC CIRCUITS

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*This paper proposes approach to cost's estimation of mixed-signal integrated circuits test. Considered economics model allows comparing different test realizations from the cost point of view, which spent on test preparation, manufacturing and execution. Such comparison provides selection of the most usable test solution for each particular design taking into account its features such as manufacturing volume, used integrated technology and die area, and so on. The model proposes possibilities to investigate the influence of different characteristics and parameters of a mixed-signal design and used test solution on testing cost.*

**Keywords:** mixed-signal circuits, DFT economics, cost estimation

## 1. INTRODUCTION

Test and diagnosis of integrated circuits (IC) are essential and necessary stages of devices realisation. In different estimations, for instance, from 40 till 80 % of design and realization time of mixed-signal integrated circuits is spent on testing. Testing time is very critical parameter, which has essential influence on total time-to-market costs and defines both reliability and post-production economical success of electronic devices.

Nowadays the testing time decrease and appropriate cost reduction can be realized using two approaches: 1) design-for-testability (DFT) and 2) automated test pattern generation (ATPG). Design-for-testability is the most popular and effective approach, which is used for testing of state-of-the-art electronic devices. This approach consists in simultaneous design of IC and search of test solutions, which will be able to simplify the circuit testing. In the framework of DFT approach on early stages of electronics device design the following tasks are decided: 1) selection of modes and conditions of next test realization; 2) definition of test kind; 3) test circuitry generation and its integration in the original design, etc.

The ATPG approach proposes automated generation of input test signals for specified design depending on selected test mode (exhaustive, random, pseudorandom, and so on), and also estimating completeness of obtained tests.

The qualitative assessment of proposed test solutions in both approaches is realized as rule using the following parameters: 1) completeness; 2) test time and speed; 3) complexity; 4) universality (flexibility), etc. Meanwhile in practice one of the most important parameters of test and its realization is the cost. The economical part exerts influence on practical application of a test solution in dependence on its characteristics and features of the project at whole.

To the present time there are several methods of estimation test economics and DFT cost for digital circuits [1] – [6].

In proposed paper the ways of cost estimation of testing mixed-signal electronics circuits are considered. The economics model taking into account application DFT and ATPG approaches at design stage allows to compare different solutions with each other and to select the most appropriate test mechanism from the cost point of view. During such selection a lot of different parameters such as used integrated technology, manufacturing volume, IC complexity (die area), ratio of analog and digital subcircuits areas and others are considered.

## 2. TEST COST MODEL

In common case the cost of testing electronic circuit is defined by the following three main components: 1) the cost of test preparation, 2) the cost of test manufacturing, and 3) the cost of test execution. Thus, test cost may be estimated by expression 1

$$C_{total} = C_{prep} + C_{manuf} + C_{exec}, \quad (1)$$

where $C_{total}$ is test cost, $C_{prep}$ is cost of test preparation, $C_{manuf}$ is cost of test manufacturing, and $C_{manuf}$ is cost of test execution.

Test preparation deals with solving several tasks such as test generation, test scenario (or test program) preparation and design of test circuitry. The test preparation cost item in equation 1 can be expressed as

$$C_{prep} = (C_{TGen} + C_{TScen} + C_{TestCirDes} + C_{ATPG})/Y, \quad (2)$$

where $C_{TGen}$ is cost of test generation, $C_{TScen}$ is cost of test scenario preparation, $C_{TestCirDes}$ is the test circuitry design cost, $C_{ATPG}$ is cost of used ATPG tools, and $Y$ is yield. The division on yield in expression 2 provides to calculate test preparation cost for good die only.

The test generation cost is the function of personnel cost and time on test generation:

$$C_{TGen} = (C_{pers} T_{TGen\_MSC})/V, \quad (3)$$

where $C_{pers}$ is personnel cost, $T_{TGen\_MSC}$ is time required for test generation of mixed-signal circuit, and $V$ is manufacturing volume of IC. Division on $V$ provides calculation of test generation cost per die.

The $T_{TGen\_MSC}$ is formed by times of test generation for digital and analog subcircuits correspondingly:

$$T_{TGen\_MSC} = T_{TGen\_DSC} + T_{TGen\_ASC}. \quad (4)$$

The test generation time depends on circuit complexity and die area. In the model the following equations are proposed for computing test generation times for digital and analog subcircuits of mixed-signal IC:

$$T_{TGen\_DSC} = R_{DSC} A_{DSC}^2, \quad (5)$$

$$T_{TGen\_ASC} = R_{ASC} A_{ASC}^2, \quad (6)$$

where $R_{DSC}$ and $R_{ASC}$ are constants reflecting complexity of test generation and dependent on complexity of digital and analog subcircuits accordingly, $A_{DSC}$ and $A_{ASC}$ are areas of digital and analog subcircuits. In equations 5 and 6 test generation times depend on square of digital and analog subcircuits area. Such dependence was established empirically. These equations may by specified for each particular application and used integrated technology.

Equation 3 relies that personnel cost of test generation for digital and analog subcircuits is the same. Really in practice they are differed. In this case the test generation cost should take into account such circumstance:

$$C_{TGen} = (C_{pers\_DSC} T_{TGen\_DSC} + C_{pers\_ASC} T_{TGen\_ASC})/V. \quad (7)$$

Test scenario preparation deals with definition of test flow, where unique test procedures are developed or existent test strategies are adapted to current design. The transformation of obtained test vectors or test patterns to a format used by test equipment is performed also.

If test scenario is prepared simultaneously with test generation then $C_{TScen}$ cost may be estimated as fraction of test generation cost:

$$C_{TScen} = K_{intens} C_{TGen}, \quad (8)$$

where $K_{intens}$ is coefficient of test scenario preparation intention in cost of test generation.

If test generation and test scenario preparation are two separate tasks, then cost $C_{TScen}$ is computed as following:

$$C_{TScen} = (C_{pers\_DSC} T_{TScen\_DSC} + C_{pers\_ASC} T_{TScen\_ASC})/V, \quad (9)$$

where $T_{TScen\_DSC}$ and $T_{TScen\_ASC}$ are times spent on preparation of test scenarios for digital and analog subcircuits accordingly. These values of time depend on complexity of digital and analog subcircuits.

The cost of test circuitry design is spent on design of new testing subcircuits or adaptation of existent solutions to current project. This item may be computed as following:

$$C_{TestCirDes} = (C_{TestDSC} + C_{TestASC})/V, \quad (10)$$

where $C_{TestDSC}$ and $C_{TestASC}$ are costs on design of test circuitries for digital analog subcircuits correspondingly. The cost of testing subcircuits design deals with their complexity and features of mixed-signal IC. These values may be expressed via test circuitry area as following:

$$C_{TestDSC} = C_{DigitalDes} A_{TestDSC}, \quad (11)$$

$$C_{TestASC} = C_{AnalogDes} A_{TestASC}, \quad (12)$$

where $C_{DigitalDes}$ and $C_{DigitalDes}$ are costs of digital and analog design for the unit of area, $A_{TestDSC}$ and $A_{TestASC}$ are areas of digital and analog test circuitries accordingly. These parameters depend on used integrated technology, and also on selected test solution.

The cost $C_{ATPG}$ is dealt with ATPG software application for test generation and takes into account software price, periods and cost of active use, idle time and depreciation.

$$\begin{aligned} C_{ATPG} = &[C_{SW\_Act} + C_{SW} K_{derp} / T_{hy} \times \\ &\times (1 - K_{SW\_use}) / K_{SW\_use}] \; T_{ATPG} / V \end{aligned}, \quad (13)$$

$$K_{SW\_use} = T_{ATPG} / T_{SW\_total}, \quad (14)$$

where $C_{SW\_Act}$ is cost rate for active use of ATPG software, $C_{SW}$ is the software price, $K_{depr}$ is the annual depreciation rate, $T_{hy}$ is the constant equal to a number of seconds in one year, $K_{SW\_use}$ is ATPG software use factor, $T_{ATPG}$ is total time required for automated test pattern generation for the current project, $T_{SW\_total}$ is the total time of ATPG software use.

The test manufacturing cost consists of two basic parts – cost of silicon overheads required for realization of test circuitry and cost of testing implemented test circuitry.

$$C_{manuf} = C_{silicon} + C_{siliconTest} / V, \quad (15)$$

$$C_{silicon} = C_{area} \left( \frac{A_{TestDSC} + A_{TestASC}}{Y_{TestCir}} - \frac{A_{TestDSC} + A_{TestASC}}{Y_{NoTestCir}} \right), \quad (16)$$

$$C_{area} = \frac{C_{wafer}}{\pi R^2 K_{use}}, \quad (17)$$

where $K_{use}$ is the factor of wafer use, $C_{area}$ is the cost of area unit, $C_{wafer}$ is the cost of wafer, $Y_{TestCir}$ and $Y_{NoTestCir}$ are yield of device with testing circuitry and without one correspondingly.

For model simplification the item $C_{siliconTest}$ may be considered equal to 0.

The test execution cost is defined by direct costs on exploiting and application of test equipment and tools. Such cost in the model is computed as following:

$$C_{exec} = (C_{Gen} + C_{ATE} + C_{TestTools})/Y, \quad (18)$$

where $C_{Gen}$ is the cost per die of using test generator, $C_{ATE}$ is the cost per die of using automated test equipment, and $C_{TestTools}$ is the cost per die of using special tools for testing.

The test generator use per die is computed as following:

$$C_{Gen} = T_{test}(C_{GenAct} + C_{GenInact}(1 - K_{GenUse})/K_{GenUse}), \quad (19)$$

$$K_{GenUse} = T_{GenUse}/T_{GenTotal}), \quad (20)$$

where $T_{test}$ is average time required for testing one die, $K_{GenUse}$ is the factor of generator use, $T_{GenUse}$ is the time of generator using for circuits testing, $T_{GenTotal}$ is the total time of generator exploiting, $C_{GenAct}$ is the cost of generator active use per second, $C_{GenInact}$ is the cost of generator idle per second.

The automated test equipment use per die is computed as following:

$$C_{ATE} = T_{test}(C_{ATEAct} + C_{ATEInact}(1 - K_{ATEUse})/K_{ATEUse}), \quad (21)$$

$$K_{ATEUse} = T_{ATEUse}/T_{ATETotal}), \quad (22)$$

where $K_{ATEUse}$ is the factor of ATE use, $T_{ATEUse}$ is the time of ATE using for circuits testing, $T_{ATETotal}$ is the total time of ATE exploiting, $C_{ATEAct}$ is the cost of ATE active use per second, $C_{ATEInact}$ is the cost of ATE idle per second.

The costs $C_{GenInact}$ and $C_{ATEInact}$ are calculated taking into account total price of devices and both depreciation period and rate.

The cost $C_{TestTools}$ is dealt with the cost of consumables required for test realization. Such test tools are changed as far as they wear out.

### 3. THE PURPOSE OF TEST COST MODEL

Design for testability provides improving the test quality at reduction total time costs (by definition). The use of test circuitry is the efficient solution from technical point of view, but sometimes it is not practically acceptable from position of costs spent on realization. The economical model allows estimating direct and indirect

costs dealt with design for testability. The analysis of testing cost at changing such mixed-signal project's parameters as volume, die area, digital and analog subcircuits' complexities, cost of used test equipment and others provides the choice of conditions for testing cost minimization and expediency of DFT application. Moreover, on the base of the model the choice among alternative test solutions in favor of such one that is economically more profitable may be done.

The use in the model of coefficients and cost criterions of specific manufacturing defines maximum precision of testing cost estimation.

## 4. CONCLUSION

In this paper the economic model of DFT and ATPG application for mixed-signal circuits is presented. In future the authors suppose to realize expert system using the proposed economical model. Such system will be the tool facilitating decision making about expediency of test circuitry use for each project taking into account its specific features and providing choice of economically sound test solutions for mixed-signal circuits.

## 5. REFERENCES

[1] J. M. Miranda, *A BIST and Boundary-Scan Economics Framework*, IEEE Design and Test of Computers, No. 3, 1997, pp. 17 – 23.

[2] B. P. Davis, *The Economics of Automatic Testing*, McGraw-Hill Book Co., London, UK, 1982.

[3] K. M. Butler, *Estimating the Economic Benefits of DFT*, IEEE Design and Test of Computers, No. 1, 1999, pp. 71 – 79.

[4] J. Turino, *Design for Test and Time to Market: A Personal Perspective*, IEEE Design and Test of Computers, No. 3, 1999, pp. 23 – 27.

[5] E. D. Boskin, C. J. Spanos, and G. J. Korsh, *Method for Modeling the Manufacturability of IC Design*, IEEE Trans. Semiconductor Manufacturing. Vol. 7, No. 3, Aug. 1994, pp. 298 – 305.

[6] P. K. Nag, A. Gattiker, S. Wei, R. D. Blaton, and W. Maly, *Modeling the Economics of Testing: A DFT Perspective*, IEEE Design and Test of Computers, No. 1, 2002, pp. 29 – 41.