

## PRACTICAL EXAMINATION OF RELATIONSHIPS BETWEEN DESIGN AND PERFORMANCE PARAMETERS OF CMOS AMPLIFIERS

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*The paper proposes a set of experiments with CMOS transistor array, which is a part of EDUCHIP test circuit. The goal of the experiments is to examine the dependence of the performance of CMOS amplifiers from bias current and W/L ratio of amplifying transistors. For that purpose different topologies of CMOS amplifying stages are presented and circuits for testing their basic small signal parameters and characteristics are discussed. Generalized tabular and graphical results from practical measurements are shown. They can be used in research and education on microelectronic circuits.*

**Keywords:** CMOS Analog Circuits, Design parameter, Performance parameter, Differential amplifier, Operational Transconductance Amplifier

### 1. INTRODUCTION

The practical investigation of semiconductor technologies is usually carried out by using specially designed test circuits with standard functional blocks [1], [2]. The studying of these blocks gives useful information for possible performance of electronic circuits implemented on the concrete technology.

The VLSI EDUCHIP was designed and manufactured by consortium from Central European Universities in Poland, Bulgaria, Slovakia and Hungary [3]. It is intended for the purposes of practical education, but also, gives possibilities to test and demonstrate the characteristics of the used technological process [4], [5], [6].

Fig. 1 shows both arrays (Analog Array 1 and Analog Array 2) with partially connected CMOS transistors. They are designed for EDUCHIP project at ECAD Laboratory of Technical University of Sofia [7] and allow integration of theoretical analysis and practical investigations of basic analog microelectronic circuits [8]. The students and engineers can carry out different experiments with these circuits, in order to study the basic principles of their functionality and to understand the limitations of the examined technology. Some of the experiments with Analog Arrays 2 are dedicated to investigation of relationships between design parameters and the performance of CMOS amplifiers. The both most important design parameters of integrated CMOS amplifiers are bias current and  $W/L$  ratio of amplifying transistor [9]. They influence on the gain, output resistance, frequency response, and slew rate of amplifiers.

The paper proposes a set of experiments with Analog Array 2 of EDUCHIP test circuit. The goal is to examine and demonstrate the relationships between performance parameters of CMOS amplifiers and bias current and  $W/L$  ratio of amplifying transistors.

To this aim, different topologies of CMOS amplifiers are presented and circuits for practically testing of their basic small signal parameters and characteristics are discussed. On the basis of practical measurements tabular and graphical results are generalized.

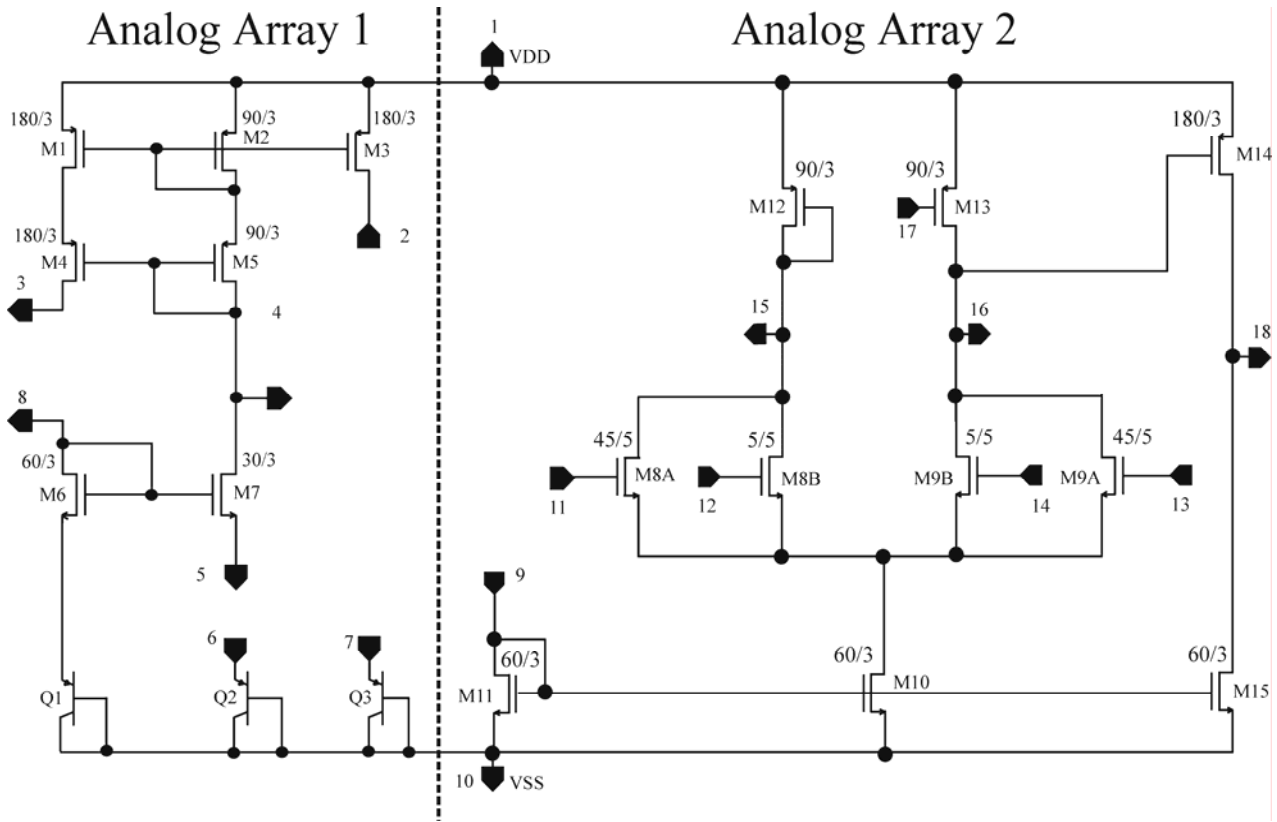


Fig. 1. Analog Array Architecture

## 2. DEVELOPMENT OF TEST CIRCUITS

To study the influence of the biasing current and  $W/L$  ratio of the amplifying transistors on the performance of the CMOS amplifiers, Analog Array 2 can be connected in three basic configurations.

The first topology is differential amplifier M8-M11 with diode-connected loads M12, M13 (Fig. 2, Fig. 3). It is implemented by connecting pin 16 and pin 17 of the array. Pin 16 is the output of the amplifier. The gain  $A_D$  of the discussed stage is approximately equals to [9]:

$$(1) \quad A_D \approx \frac{1}{2} \frac{g_{m8}}{g_{m12}} = \frac{1}{2} \frac{g_{m9}}{g_{m13}} = \frac{\sqrt{2k_n(W8/L8)I_{D8}}}{2\sqrt{2k_p(W12/L12)I_{D12}}} = \sqrt{\frac{k_n(W8/L8)}{4k_p(W12/L12)}} = \text{const.}$$

In the above formula  $g_m$  is transconductance,  $g_o$  is output conductance, and  $k_n$  and  $k_p$  are transconductance parameters of the transistors. The circuit is used to study the influence of  $I_{REF}$  and  $W/L$  on the gain of amplifier. By using external resistance  $R$  (between 20k and 250k), the current  $I_{REF}$  can be regulated between 10 $\mu$ A and 120 $\mu$ A. The  $W/L$  ratio can be controlled by using appropriate connections of the gates of transistors M8 and M9, as it is show on Fig. 2 and Fig. 3.

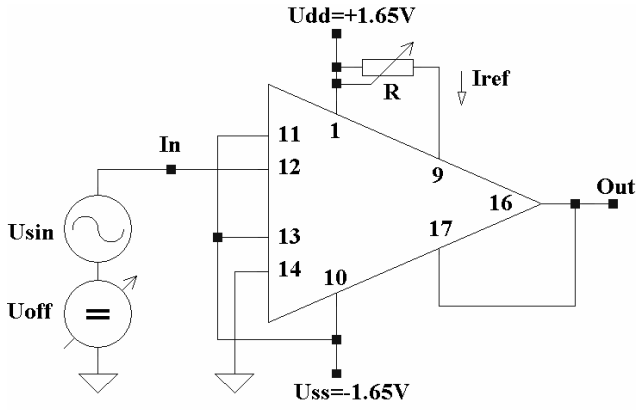


Fig. 2. Circuit for examination the gain  $A_D$  when  $W_8/L_8=W_9/L_9=5/5$

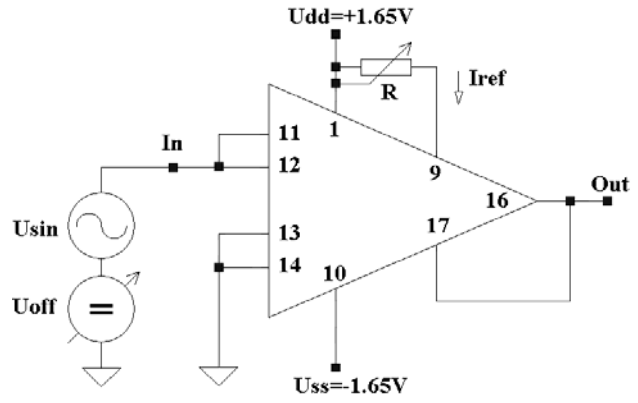


Fig. 3. Circuit for examination the gain  $A_D$  when  $W_8/L_8=W_9/L_9=50/5$

The second configuration is differential amplifier with current source load (Fig. 4). It is obtained by short connection of pins 15 and 17. The circuit is used to examine practically the relationships between  $I_{REF}$  and the gain  $A_{DIFF}$  of the amplifier. The formula for the gain is [9]:

$$(2) \quad A_{DIFF} = \frac{g_{m9}}{g_{o9} + g_{o13}} = \frac{\sqrt{2k_n(W_9/L_9)I_9}}{(\lambda_9 + \lambda_{13})I_9} = 2 \frac{\sqrt{k_n(W_9/L_9)}}{(\lambda_9 + \lambda_{13})\sqrt{I_{REF}}} = \frac{const.}{(\lambda_{14} + \lambda_{15})\sqrt{I_{REF}}}.$$

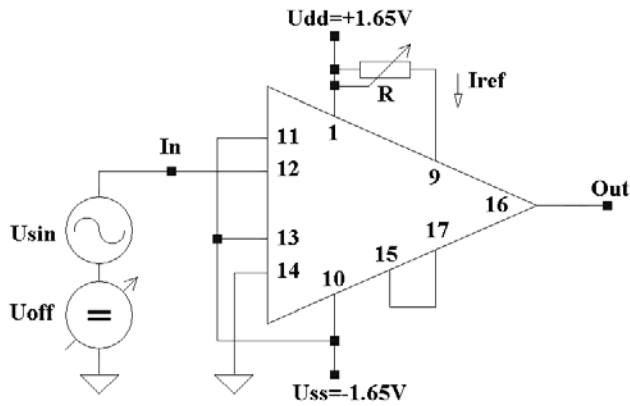


Fig. 4. Circuit for  $A_{DIFF}$  examination

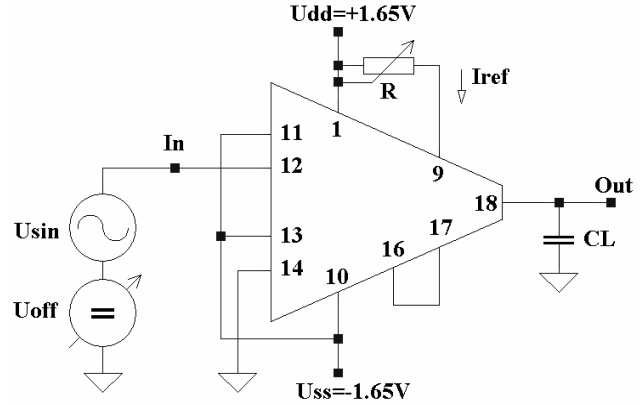


Fig. 5. Circuit for  $A_{OL}$  and  $f_C$  examination

The third topology is simple operational transconductance amplifier OTA (Fig. 5). All nodes in the amplifier are low impedance except the input and the output. This circuit usually drives only capacitive loads and does not require frequency compensation. It consists of differential amplifier with diode-connected load (M8B-M13) and common source output stage with active load (M14-M15). The open loop gain  $A_{OL}$  of OTA is equal to the product of the gain of differential amplifier  $A_D$  and of the gain of output stage  $A_{OUT}$ . The presented circuit is used to examine the influence of the bias current  $I_{REF}$  on the open loop gain  $A_{OL}$ , output resistance  $R_{OUT}$  and frequency response of OTA, as well as the gain of output stage  $A_{OUT}$ .

The formulas for  $A_{OL}$ , output resistance  $R_{OUT}$  and the critical (-3dB) frequency  $f_C$ , are [9]:

$$\begin{aligned}
 A_{OL} &= A_D A_{OUT} = \frac{1}{2} \frac{g_{m9}}{g_{m13}} \frac{g_{m14}}{g_{o14} + g_{o15}} = \frac{1}{2} \sqrt{\frac{2k_n(W_9/L_9)I_9}{2k_p(W_{13}/L_{13})I_9}} \frac{\sqrt{2k_n(W_{14}/L_{14})I_{14}}}{(\lambda_{14} + \lambda_{15})I_{14}} = \\
 (3) \quad &= \frac{1}{2} \sqrt{\frac{k_n(W_9/L_9)}{k_p(W_{13}/L_{13})}} \frac{\sqrt{2k_n(W_{14}/L_{14})}}{(\lambda_{14} + \lambda_{15})\sqrt{I_{14}}} = \frac{const.}{(\lambda_{14} + \lambda_{15})\sqrt{I_{REF}}}
 \end{aligned}$$

$$(4) \quad R_{OUT} = \frac{1}{g_{o14} + g_{o15}} = \frac{1}{(\lambda_{14} + \lambda_{15})I_{REF}} = \frac{A_{OUT}}{g_{m14}} = \frac{A_{OUT}}{\sqrt{2k_p(W_{14}/L_{14})I_{REF}}},$$

$$(5) \quad f_C = \frac{1}{2\pi R_{OUT} C_L} = \frac{(\lambda_{14} + \lambda_{15})I_{REF}}{2\pi C_L}.$$

The Equations 1÷5 can be used for comparison of practical behavior of amplifiers with theoretically expected characteristics.

### 3. EXPERIMENTAL RESULTS

Tabl. 1 shows the results from examination of voltage gain  $A_D$  of differential amplifier with diode-connected load (Fig.2 and Fig.3). The frequency of the input signal is 100Hz and the amplitude is about 500mV. As it is shown in Equation (1), the value depends only on  $W_8/L_8$  ratio of the input differential pair.

Tabl.1. Results from examination of the gain  $A_D$

$I_{ref}, \mu A$	20 $\mu A$	40 $\mu A$	60 $\mu A$	80 $\mu A$	100 $\mu A$
$A_D (\frac{W_8}{L_8} = \frac{W_9}{L_9} = 1)$	0.158	0.158	0.158	0.158	0.158
$A_D (\frac{W_8}{L_8} = \frac{W_9}{L_9} = 10)$	0.5	0.5	0.5	0.5	0.5

Tabl. 2 presents the results from examination of voltage gain  $A_{DIFF}$  of differential amplifier with current source load (Fig.4). The results demonstrate the inverse proportionality between the biasing current  $I_{ref}$  and the gain of amplifier, as it is shown in Equation (2).

Tabl. 2. Results from examination of the gain  $A_{DIFF}$

$I_{ref}, \mu A$	20 $\mu A$	40 $\mu A$	60 $\mu A$	80 $\mu A$	100 $\mu A$
$A_{DIFF} (\frac{W_8}{L_8} = \frac{W_9}{L_9} = 1)$	156	120	102	92	82

Tabl. 3. Results from examination of  $A_{OL}$ ,  $A_{OUT}$  and  $R_{OUT}$

$I_{ref}, \mu A$	20 $\mu A$	40 $\mu A$	60 $\mu A$	80 $\mu A$	100 $\mu A$
$A_{OL} (\frac{W_8}{L_8} = \frac{W_9}{L_9} = 1)$	62	48	40	36	33
$A_{OUT} = A_{OL} / A_D$	387.5	300	250	225	206.3
$R_{OUT}, M\Omega$	1.250	0.685	0.466	0.363	0.298

Tabl. 3 shows the results from practical examination of open loop gain  $A_{OL}$  of OTA circuit (Fig. 5) as well as the results from computation of the gain of output stage  $A_{OUT}$ . Graphics of  $A_{DIFF}$ ,  $A_{OL}$  and  $A_{OUT}$  are shown on Fig.6. The obtained trendlines demonstrate the inverse proportionality between  $\sqrt{I_{REF}}$  and the values of  $A_{DIFF}$ ,  $A_{OL}$  and  $A_{OUT}$ , as it is shown in Equations (2) and (3). The results in last row of Tabl.3 present the inverse proportionality between  $I_{REF}$  and output resistance  $R_{OUT}$  of OTA.

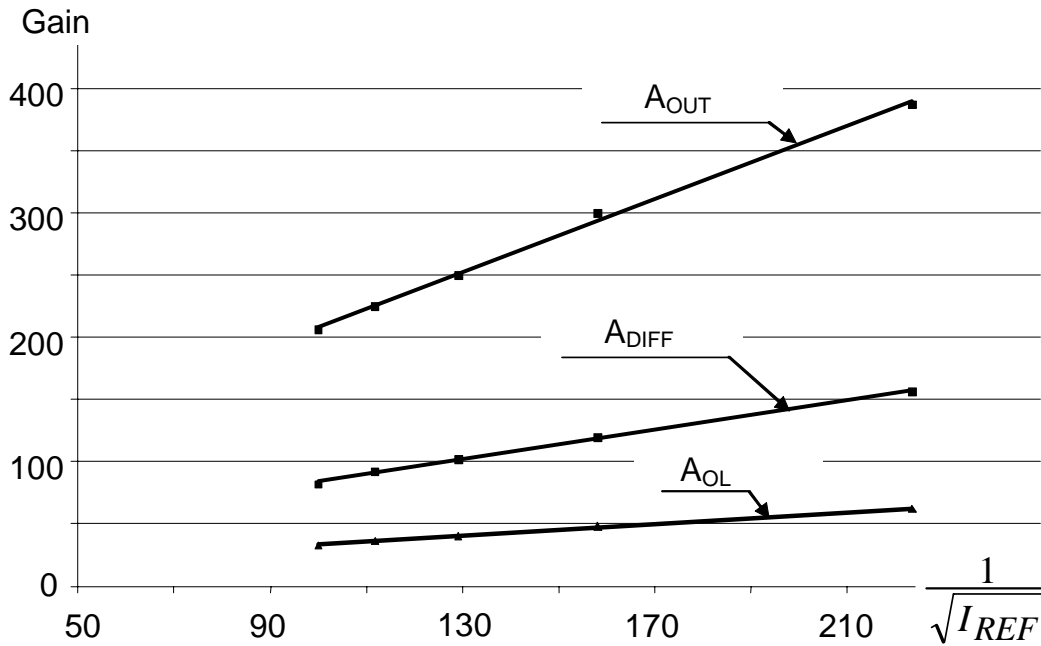


Fig. 6. Graphical representation of the results from investigation of small signal gain of amplifiers

The results from examination of critical frequency  $f_C$  of simple OTA for different values of capacitive load  $C_L$  are presented in Tabl.4 and Fig.7. They clearly show the direct proportionality between the critical frequency and the value of biasing current  $I_{REF}$ , which corresponds to Equation (5).

Tabl. 4. Results from examination of critical frequency  $f_C$

$I_{ref}, \mu A$	20 $\mu A$	40 $\mu A$	60 $\mu A$	80 $\mu A$	100 $\mu A$
$f_{C1} (C_L \approx 30 pF)$	4150	7100	9650	11900	14500
$f_{C2} (C_L \approx 45 pF)$	3150	5500	7650	9300	11200
$f_{C3} (C_L \approx 60 pF)$	2400	4300	6000	7300	8800

#### 4. CONCLUSION

The paper presents the results from practical examination of different CMOS amplifiers, which are implemented with Analog Array 2 of EDUCHIP test circuit.

Three basic topologies of amplifiers are studied and the obtained results are presented in tabular and graphical formats. They clearly demonstrate the basic relationships between most important design parameters (bias current and  $W8/L8$  ratio) and small signal gain, output resistance and critical frequency of CMOS amplifiers.

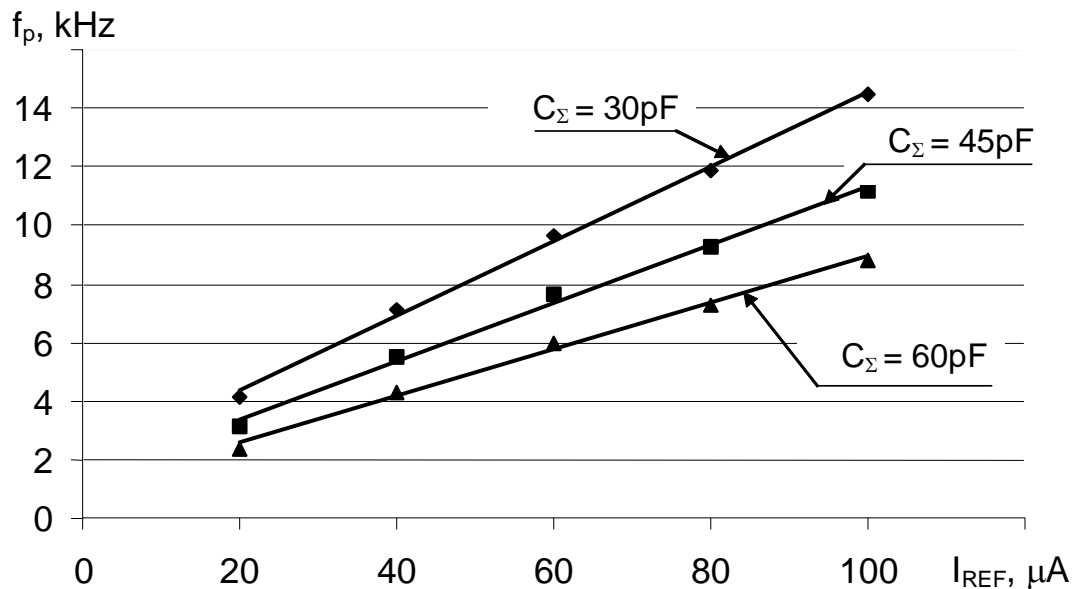


Fig. 7. Graphical representation of the results from investigation of critical frequency of amplifier

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