THE BASIC BUILDING BLOCKS OF 1.8 GHZ PLL IN CMOS TECHNOLOGY

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This paper deals with the design of elementary building blocks of frequency synthesizer (Phase-Locked Loop) – phase detector and voltage-controlled oscillator (VCO) in the radio frequency region (RF). They have been designed in the standard AMS 0.35μm CMOS technology, with analysis and optimisation performed using CADENCE tools (SpectreRF) and ASITIC software. The VCO was experimentally realised as test chip with A-MOS capacitance tuning circuit elements. The proposed LC oscillator is implemented in double-cross topology with the supply voltage of 2.7 V. Additionally, also a phase comparator design is discussed, implemented and investigated, as a very important part of the PLL structure for RF applications. The low phase noise PLL implementation is also presented.

Keywords: PLL, Phase-Locked Loop, VCO, phase detector, voltage-controlled oscillator

1. INTRODUCTION

The explosive growth in recent wireless communications has led towards increased demands for wireless products that would be low-cost, low-power, and compact in size. Moreover, extensive research and development in semiconductor industry in last years has shown that standard CMOS process, usually associated with the digital part of wireless systems, became more interesting as a choice for implementation of RF components such as low-noise amplifiers (LNAs), mixers, and voltage-controlled oscillators (VCOs) [1]. Today, deep-submicron advanced CMOS processes typically reach the f_t of 50 GHz and offer low noise devices, making them serious alternative for RF circuit integration. The further benefits include leveraging high-volume silicon CMOS fabrication capacity for RF products and the potential for achieving high-levels of RF, analog, and digital integration, rapidly approaching single-chip system implementations (smart systems, system-on-chip (SoC), etc.).

2. PHASE-LOCKED LOOP ARCHITECTURE

Phase-Locked Loop (PLL) is one of the advanced architectures used in different applications to fulfil various tasks. The concept of phase locking was invented in 1930s and swiftly found a wide use in electronic systems. Before discovery of monolithic integrated circuits, applications of PLL were limited only to very expensive precise measurement systems. Expansion of monolithic integrated circuits enabled a widespread use of PLL circuits in lot of electronic applications. Today, PLL circuits are irretrievable components of different electronic integrated systems. There are many options of PLL application in frequency synthesis. The crucial

circuits of a PLL frequency synthesizer (established by PLL) are a voltage-controlled oscillator and a phase detector (PFD). Figure 1 shows the basic concept of PLL. It consists of two essential parts: the VCO and the Phase detector. The phase detector is a circuit whose average output is linearly proportional to the phase difference between its two inputs. It compares the phase of the reference signal to that of the VCO and produces an output signal that is a function of their phase difference. Output signal is then filtrated by a loop filter and connected to the VCO. The VCO simply generates a signal whose frequency is a function of the control voltage. The general idea is that the output of the phase detector drives the VCO frequency in a direction that reduces the phase difference (a negative feedback system).

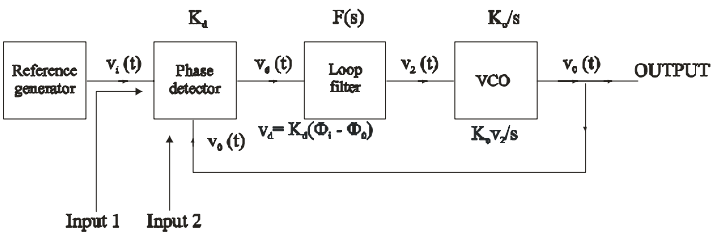

Fig.1. Basic block diagram of PLL architecture

3. THE PHASE DETECTOR DESIGN

This block is fed with two input signals. At Input1 the PLL reference frequency from the reference generator is applied and at Input2 represents feedback output signal of the VCO. The phase detector compares both frequency and phase of these two signals and its output signal, shaped further by other circuits (loop filter, charge pump…), drives the VCO. Average output of the phase detector is linearly proportional to the phase difference between its two input signals. Relation between the PFD output voltage and phase difference of its input signals is called gain constant of phase detector and defined by the following formula:

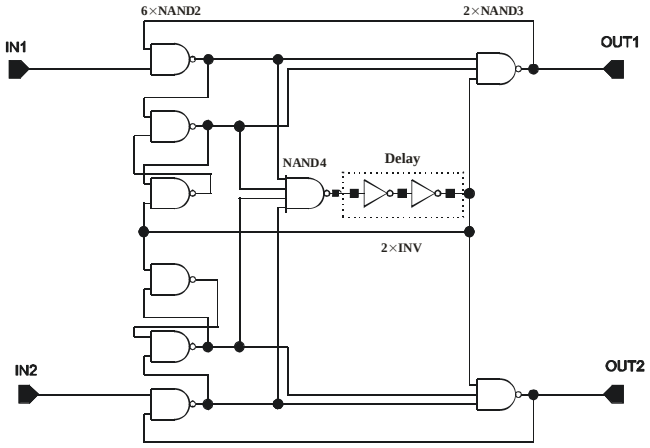

Fig.2. Proposed phase frequency detector

$$K_d = \frac{\partial V_{out}}{\partial \varphi} \text{ [V/rad]}, \tag{1}$$

where V_{out} is the output voltage and φ is phase difference of the input signals. The PLL uses the three-state PFD with the supply voltage of 2.7V. The PFD is designed to generate symmetrical charge-up and charge-down pulses. The proposed PFD is composed of nine NAND gates, as shown in Figure. 2. The potential dead zone is eliminated by the propagation delay of the two inverters that produces a minimum pulse width at the PFD output even when the phase error is zero. It is important to

provide a high reference frequency of PLL in order to fast retune of oscillating frequency of the VCO. The proposed PFD operates at the frequency of 100 MHz. Since the standard library logical gates are too slow for this frequency, proper circuits have been designed to satisfy this requirement. Figure 3 shows results of transient simulation of the designed PFD circuit. The reference frequency (Input1) is 100 MHz and the feedback signal frequency (Input2) 108 MHz. At the output OUT1, a pulse-width modulation determined by the phase/frequency difference of input signals is observed. On the other hand, only short pulses produced by logical gates toggling occur at the output OUT2. The operating range from -5.86 to 5.86 rad (from -336 to +336 degrees) and its gain constant of 0.45V/rad are achieved.

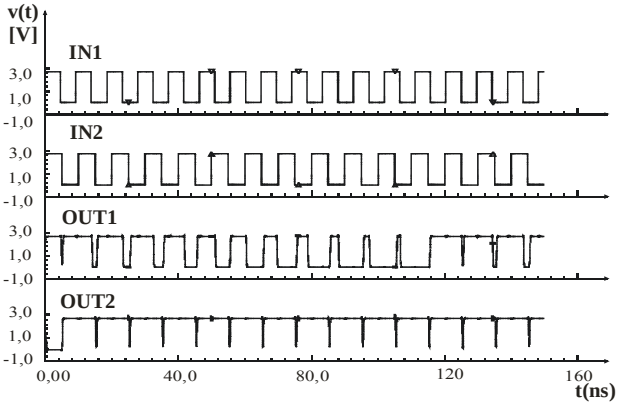

Fig.3. Signal waveforms of PFD.

4. VCO DESIGN

VCOs are key components in frequency synthesizers, phase-locked loops (PLL), and clock recovery circuits used in RF wireless applications and high-speed digital communications. Differential approaches are required mostly because these frequency sources are used to pump Gilbert-cell-type mixers. The oscillator design requires lots of compromises. In [2]-[3] several different types of VCO circuits, possibly to be implemented in CMOS technology, can be found. A standard approach to differential VCOs is the cross-coupled MOS transistor pair to generate a negative resistance. The solution should be sufficient to overcome the equivalent parallel resistance of the VCO tank circuit, and to generate the desired oscillation. Such VCO circuits are known as LC-tank VCOs. The complementary oscillator circuit is a result of using both pMOS and nMOS cross-coupled pairs in parallel. Proposed LC oscillators were implemented using double-cross topology with the supply voltage of 2.7 V, as shown in Figure 4. The LC-tank represents a combination of fixed inductors and tunable capacitors (varactors). Moreover, high quality factors of the inductor and the varactor are necessary to achieve low phase noise and low power

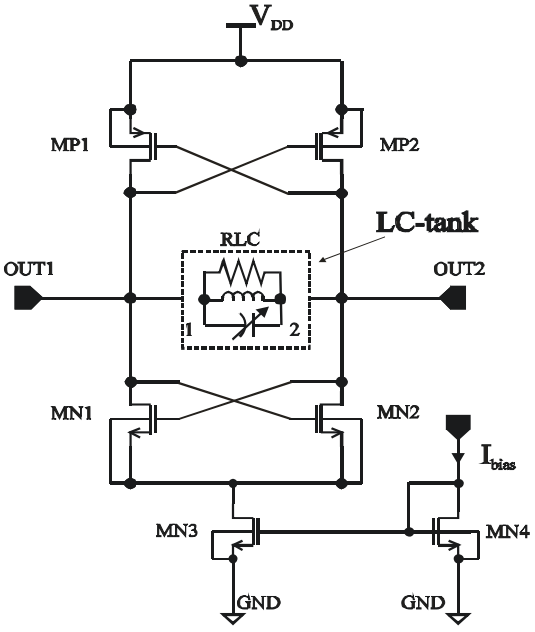

Fig.4. Designed LC oscillators with double - cross topology

consumptions of the VCO. Thus, the resulting behavior of the VCO depends on the quality factor of LC-tank and other parasitic elements of the VCO circuits.The total inductance of the resulting coil is 3.6nH, and its quality factor is 5.1 at 1.8GHz. The inductor was implemented in the highest METAL layer so that the series resistance and the total capacitance toward substrate could be decreased to the lowest possible values. The software called ASITC - Analysis of Si Inductors and Transformers, by Berkeley University, has been used as a convenient and fast tool for modeling integrated inductors. Unlike capacitors, inductors are not readily available in a standard CMOS technology because they are more complex devices due to existence of mutual interaction among the coils themselves, frequency dependent effects (skin effect), and substrate loss. Standard CMOS processes are not favorable because the substrate is highly conductive and thus increasing the eddy currents and lowering the quality factor. Concerning possible implementation of integrated capacitors in astandard CMOS process, it is well known that a MOS transistor with drain, source and bulk (D, S, B) connected together represents a MOS capacitor with a capacitance value dependent on the voltage V_{BG} applied between bulk (B) and gate (G) [4,5]. This fact was utilized in our VCO design. The proposed VCO uses a capacitor implemented by A-MOS structure. A- MOS is formed of a modified p-MOS transistor by removing p-diffusion areas of drain and source, and substituting them by n-diffusions. The dominant advantage of this structure is the higher tunable range of the capacitances and higher quality factor, because the mobility of electrons is approximately three times higher than the mobility of holes. More information about LC thank design can be found in [6]. The oscillator oscillates at 1.8GHz with the output signal amplitude of 790mV. The amplitude value of the output signal depends on the quality factor of the resonance circuit and on the tail current that flows through the current source MN3 (Figure 4). These attributes have dominant influence on the phase noise of the oscillator as well. The carrier frequency can be varied approximately between 1.5GHz and 2GHz in the tuning voltage range from 0V to 2.7V. In this range, VCO gain reaches values up to 480MHz. In Figure 5, the oscillation frequency and VCO gain of oscillator are displayed. The phase noise is one of the most important oscillator parameters. The proposed VCO was designed to offer very low phase noise, and simulation results show that the VCO phase noise of 133 dBc/Hz at 600kHz offset from the carrier frequency of 1.8GHz. is achieved for the A-MOS capacitor structure. Phase noise was simulated using SPECTRE RF with bsim3v.3 MOS transistor models. More detailed discussion about phase noise of oscillators can be found in [6], [7].

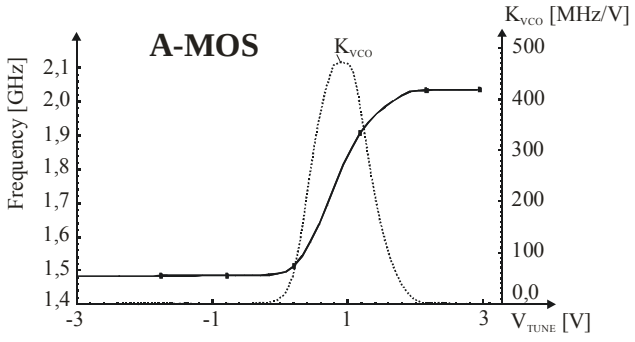

Fig.5. Oscillation frequency and gain of the oscillator with A-MOS structure as a function of tuning range

5. PLL IMPLEMENTATION

As mentioned, PLLs have became ubiquitous in modern communication systems. Several examples of PLL application can be found in [3]. In radio-frequency wireless transceivers, frequency synthesizers based on the PLL architectures are often used as local oscillators for up and down frequency conversions. PLLs are suitable for monolithic integration and thus, they can be of small size, of low cost, and power thrifty. Basic functional blocks of PLL's for frequency-synthesis applications include a phase detector, loop filter, VCO, and frequency divider that is embedded into a feedback of PLL. By varying the divide ratio of the frequency divider, the PLL can synthesize a new frequency based upon the reference input while retaining the stability, accuracy, and spectral purity of the original reference.

The major design considerations in the PLL systems are channel frequency spacing, frequency switching time, and phase noise. The following principal PLL conception is projected to satisfy mentioned demands (fig.6). The high reference frequency and wide bandwith of loop filter provide the phase noise suppression and the short frequency switching time. There are embedded three additional blocks in the feedback to satisfy narrow channel frequency spacing: the programmable divider, mixer and filter. The frequency synthesizer, as a part of DSP processor, generates the low stable frequency f_m with the low phase noise. This frequency determinates the frequency channel spacing. The filter suppresses spurious frequencies and the filtered signal is roughly divided by frequency divider. The output frequency can be calculated the following formula:

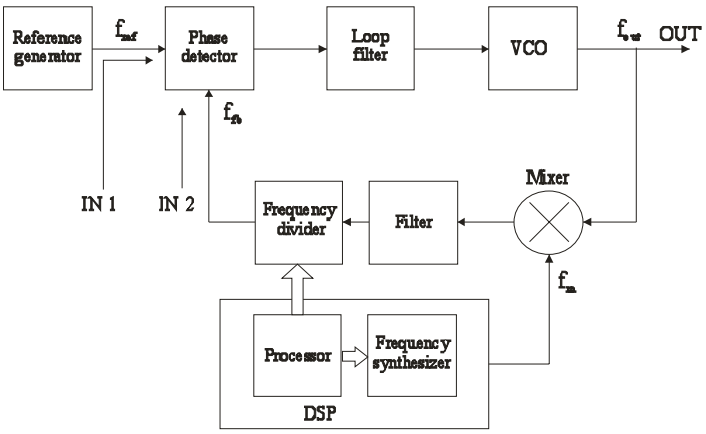

Fig.6. The block diagram of PLL system

$$f_{OUT} = N \times f_{ref} + f_m \qquad (2)$$

The proposed phase detector and VCO are dedicated to fast settling time–frequency synthesizers that are essential building blocks of modern communication systems e.g. DCS-1800 and GSM systems. These digital cellular mobile systems employ a combination of time-division duplex and frequency-division duplex techniques. In these systems, the downlink frequencies are placed in different bands with respect to uplink frequencies. In order to save cost and decrease the size of the handset, it is desirable to use the same frequency synthesizer to generate uplink and downlink frequencies.

6. CONCLUSION

In the presented work, basic parts of PLL circuit for RF application – a Phase detector and a voltage-controlled oscillator were designed and implemented in a standard CMOS process AMS 0.35μm. The proposed LC oscillator was designed and realized using double-cross topology with A-MOS capacitance tuning element with the supply voltage of 2.7V. The oscillator was analyzed and optimized using CADENCE tools (SpectreRF) and ASITIC software. The oscillator achieves -133 dBc/Hz phase noise at 600kHz offset from the carrier frequency. The tuning range of the proposed integrated VCO circuit is more than 500 MHz. Furthermore, the phase frequency detector was discussed, designed and investigated, as an extremely important part of PLL architecture.

The achieved results prove the possibility to implement successfully different high-performance RF building blocks also in a standard CMOS technology that would avoid the use of dedicated expensive RF processes.

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7. REFERENCES

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