THE INFLUENCE OF LAYOUT ON BASIC PARAMETERS OF INTEGRATED PASSIVE DEVICES

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This paper intends to point out some differences and consequences of using different layout geometry, shape and form of the passive devices. The research is made from the point of view of the layout influence on the basic parameters of the integrated passive devices. Resistors, inductors, and capacitors with structures created on different physical layers with various layer material properties are also studied, analyzed and presented.

Keywords: resistors, capacitors, inductors, RF, layout influence, research

1. INTRODUCTION

In modern submicron technologies, where can be fabricated high performance active devices, the importance of passive devices is often underestimated. The poor parameters and characteristics of passive devices degrade the excellent high-speed properties of active devices in RF and microwave integrated circuits. In addition, while active devices are continually shrinking and occupying less and less chip area passive devices still remain large and determine overall size and cost of the whole integrated circuit. Therefore, passive devices play a critical part in modern integrated circuit design.

Although, resistors and capacitors seems to be simple devices, in practical design and at high frequencies in particular, detailed structure, layout, technology and material properties of the passive devices must be taken into consideration, as well as their surroundings. Additionally, the use of passive devices such as inductors is traditionally most problematic and difficult to realize in integrated circuits.

On the other hand, the advantages of integrating RF circuits with active and passive devices are compelling. The fewer the external components, the smaller is the size of the entire circuit or system and perhaps the smaller the power consumptions. Furthermore, integration enhances the reliability of the end product as it minimizes the number of external connections that require soldering. Thus, it is necessary to study carefully the limitation of passive devices and their parasitics, respectively.

The main goal of this paper is to investigate the layout influence on basic parameters of integrated passive devices for two technologies, CMOS and SiGe BiCMOS 0.35µm, in order to derive a set of rules and guidance for their design, especially for high frequency applications. In order to accomplish that computer-aided system Cadence, Spectre circuit simulator and Diva verification tools are used.

2. RESISTORS

Resistors provide specific and controlled amounts of electrical resistance. They are useful in a variety of applications, ranging from current limiting to voltage

division. Analog circuits usually include many resistors, so it is fortunate that they are relatively easy to integrate. Most processes offer a choice of several different resistor materials. In case of AMS 0.35µm Si CMOS and AMS 0.35µm SiGe BiCMOS technologies, diffusion, polysilicon and high resistivity polysilicon resistors are available. Some are better suited to fabricating high-value resistors and others to fabricating low-value ones. The choice of resistor materials can have tremendous impact on circuit performance, so substitutions should not be mate without careful consideration on the consequences [1], [2].

Resistors with different values of width (W=1 μ m, 2 μ m, 3 μ m, 5 μ m, 10 μ m, 20 μ m) and length (L=10 μ m, 30 μ m, 60 μ m), and thus different resistance are investigated. In table 1 are compared and summarized the results for resistor with W/L=2 μ m/60 μ m using different resistor materials – p-diffusion and polysilicon layers with different implantation (i.e. different sheet resistance). It is evident, that polysilicon resistors are superior in comparison with the others. Resistors created on first polysilicon layer are more precise and have better quality factors in wide frequency range than the one created using high resistivity polysilicon layers.

Resistor material	R , Ω	R_{P1} (a) 1 GHz, Ω	Q _{P1} @1GHz	$R_{P1}@6GHz, \Omega$	Q _{P1} @6GHz
1 st polysilicon	1714	1711.83	34.33	1665.29	5.92
High resistivity polysilicon	4000	73822.2	1.13	1836.44	0.35
2 nd polysilicon	7200	7083.23	7.38	4992	1.84
Diffusion	3714	280.91	0.289	11.9767	0.07

Table 1. Resistance and quality factor for resistors created using different materials

In the table above R is extracted resistance of the structure. R_{P1} and Q_{P1} are derived resistance and quality factor from two-port Z and Y-parameters for one port driven circuit. In the case of a resistor the quality factor Q is the ratio of the real to the imaginary part of the impedance. The loss of resistance is the signal absorbed by the parallel reactance.

In table 2 are presented the results for folded (meander) resistor, employing three rectangular and 45° turns (called bands) using different spacing between turns S. First polysilicon layer is used, because it allows achieving better Q-factor and work at higher frequencies. From the presented results given in comparison with straight unfolded resistor with W/L=2 μ m/60 μ m is clear that unfolded resistors have highest Q-factor. On the other hand if the resistor is too long it is better to use 45° turns minimal spacing.

Table 2. Extracted resistance and length, and simulated resistance and Q-factor for resistors with 45° and 90° turns and different spacing between turns

Bands angle	Lum	Sum	R LO		P @6CHz O	Q _{P1} @1G	Q _{P1} @6GH
Danus angle	Γ , μπ	5, μπ	л, Ку2	$\mathbf{R}_{P1}(w)$ (G112, 52	K _{P1} @0G112, 52	Hz	Z
straight	60	-	1.714	1711.83	1665.29	34.33	5.92
45	60.04	0.5	1.715	1712.99	1628.22	26.61	4.47
45	61.54	1	1.758	1755.73	1663.07	26.27	4.3
45	64.54	2	1.844	1841.63	1739.42	26.83	4.41
90	60.1	0.5	1.717	1714.4	1622.56	26.22	4.15
90	61.6	1	1.76	1756.96	1655.9	25.46	3.90

90	64.6	2	1.846	1842.6	1731.28	24.55	3.90
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In table 3 are shown the results for meander polysilicon resistor with 45° turns, distance between turns S=0.5, and different number of bends. The result are also compared with straight unfolded resistor with $W/L=2\mu m/60\mu m$.

Table 3. Comparison of resistor length, resistance and Q-factor for polysilicon resistor with different number of bends

Number of bends	L, µm	R, Ω	R _{P1} @1GHz, Ω	R _{P1} @6GHz, Ω	Q _{P1} @1GHz	Q _{P1} @6GHz
none	60	1714	1711.83	1665.29	34.33	5.92
1	59.98	1714	1687.55	1178	9.06546	1.84959
2	59.96	1713	1676.46	1030.38	7.05565	1.36882
3	60.04	1715	1691.72	1230.13	9.99497	1.95001

In table 4 are depicted the results for the resistance, absolute (Δ) and relative deviations (δ) from the nominal value of one polysilicon resistor divided to several segments with matching in comparison with the same value folded resistor with three bends and 45°-angle. Using smaller and matched segments reduce the error caused by non uniform current distribution, although the accuracy improvement is small. Nevertheless they are preferred when resistors must operate at higher frequencies.

Table 4. Results from comparison of one polysilicon matched resistor versus the same value 3 bends and 45° -angle folded resistor

	f, GHz	1	2	3	4	5	6
45°-angle	R, Ω	2234.84	2190.24	2131.71	2050.87	1961.67	1875.26
	Δ, Ω	16.73	61.33	119.86	200.7	289.9	376.31
	δ, %	0.743037	2.723877	5.323397	8.91378	12.87546	16.71323
matched	R, Ω	2243.21	2204.18	2156.79	2089.9	2009.06	1919.86
	Δ, Ω	8.36	47.39	94.78	161.67	242.51	331.71
	δ, %	0.371296	2.104754	4.209507	7.180323	10.77071	14.73239

Comparison between simulated, extracted and measurement results is also made. The result for polysilicon resistor with $W/L=2\mu m/60\mu m$ is shown in table 5.

Table 5. Simulated, extracted and measured results for the resistance of polysilicon resistor in frequency range from 1 to 6 GHz and absolute and relative deviations from the measured value

f CIIa		Simulated			Extracted				
I, GHZ	R, Ω	Δ, Ω	δ, %	R, Ω	Δ, Ω	δ, %	R, Ω		
1	1711.09	73.24	4.104622	1711.09	73.24	4.104622	1784.33		
2	1704.99	74.83	4.204358	1701.82	78	4.382466	1779.82		
3	1694.11	79.61	4.488307	1689.32	84.4	4.758361	1773.72		
4	1675.28	97.12	5.479576	1673.68	98.72	5.569849	1772.4		
5	1658.01	106.69	6.045787	1648.47	116.23	6.586389	1764.7		
6	1632.8	121.02	6.900366	1623.25	130.57	7.444892	1753.82		

3. CAPACITORS

Capacitors are class of passive elements useful for coupling AC signals and for constructing timing and phase shift networks. They are relatively bulky devices that store energy in electrostatic fields. Analog circuits usually include at least one capacitor. Therefore, most processes offer different type of capacitors. The most commonly used one is the polysilicon capacitor. Two different polysilicon layers are used for its plates [1], [2]. It is available in AMS 0.35µm Si CMOS and AMS 0.35µm SiGe BiCMOS technologies, along with Metal-Insulator-Metal (MIM) and Metal-Oxide-Semiconductor (MOS) capacitors. For MIM capacitor the two plates are formed using different metal layers, and for MOS accumulation mode capacitor is implemented.

Capacitors with different form and values of width and length ($10\mu m$, $15\mu m$, $23.9\mu m$, $33.9\mu m$, etc), and thus, different capacitance (C = $100 fF \div 5pF$) are investigated. Analysis of the received results points out that square geometry is better than the rectangular one. In table 6 are summarized and compared simulated and extracted results for some square polysilicon capacitors. C and Q are derived from two-port Y-parameters for two-port driven circuit.

Canaditan	f,	R, C	Dhm	С,	fF	Q	
Capacitor	GHz	sim	ext	sim	ext	sim	ext
	1	17.27	16.954	84.695	85.480	108.835	109.844
	2	17.27	16.955	84.950	85.735	54.241	54.743
W_I_1_10	3	17.27	16.957	85.380	86.164	35.980	36.311
w=L=10 μm	4	17.27	16.959	85.989	86.773	26.793	27.038
	5	17.27	16.962	86.784	87.567	21.238	21.431
	6	17.27	16.965	87.777	88.559	17.498	17.655
	1G	13.489	13.343	193.154	194.205	61.099	61.431
	2G	13.489	13.344	194.489	195.539	30.333	30.497
W-I -15	3G	13.489	13.346	196.755	197.804	19.990	20.097
w=L=15 μm	4G	13.489	13.348	200.018	201.064	14.747	14.825
	5G	13.489	13.351	204.375	205.418	11.546	11.606
	6G	13.489	13.355	209.966	211.005	9.3658	9.413
	1G	11.685	11.610	490.792	492.377	27.758	27.848
	2G	11.685	11.611	499.501	501.080	13.634	13.677
W I 220	3G	11.685	11.614	514.728	516.294	8.821	8.848
$W = L = 23.9 \mu m$	4G	11.685	11.616	537.671	539.218	6.333	6.352
	5G	11.685	11.620	570.360	571.878	4.776	4.790
	6G	11.685	11.625	616.142	617.612	3.684	3.694

Table 6. Comparison of simulated and extracted results for capacitance, resistance and quality factor of polysilicon capacitor with different sizes

The parallel between simulated, extracted and measured results for the capacitance and the quality factor of capacitor with $W=L=33.9 \ \mu m$ is given in table 7. The results, received after extraction, are very close to the corresponding measurement values.

Table 7. Simulated, extracted and measured results for capacitance and Q-factor of polysilicon capacitor

f CUz	Simu	ılated	Extra	cted	Measured		
I, GHZ	C, pF	Q	C, pF	Q	C, pF	Q	
1	0.999048	39.8773	0.945714	98.0109	0.945714	99.0283	
2	1.03714	23.5704	0.945714	67.9584	0.945714	69.4875	
3	1.10571	9.38984	0.953333	44.0827	0. 941905	47.1438	
4	1.22	2.85765	0.953333	32.9618	0.945714	33.4764	
5	1.38381	2.45068	0.957143	26.9412	0.945714	26.9368	
6	1.69619	2.55095	0.960952	22.4498	0.949524	23.9804	

4. INDUCTORS

The rapid development of modern communication systems demands a higher

ELECTRONICS' 2005

level integration in the design of radio frequency integrated circuits (RFICs). In many cases, these designs cannot be realized without using the integrated spiral inductors. Thus, knowledge to realize high performance spiral inductors with desired inductance, Q-factor and self-resonance frequency (SRF) is very important. Recently, great efforts have been devoted to the modeling, optimization and design of the spiral inductors [3].

A thorough study on the performance trends of different spiral inductors is made in this paper. Inductors with various outer diameter $D_{out}=140\div300\mu m$, metal width $W=5\div20\mu m$, spacing between adjacent turns $S=2\div10\mu m$ and number of turns $N=1.75\div10$ are examined. Some of the results are presented in table 8. In the tables below L is spiral inductance, R_s is its series resistance and Q is the quality factor for one port drive operation.

Name and geometry parameters	f, GHz	1	2	3	4	5	6
SQ1	L, nH	2.075	2.091	2.115	2.15	2.196	2.256
D _{out} =250 μm, W=20 μm, S=3 μm,	R _s , Ω	3.19	3.667	4.497	5.726	7.429	9.718
N=1.75	Q	4.087	7.164	8.866	9.437	9.288	8.751
SQ2	L, nH	3.029	3.118	3.245	3.409	3.62	3.893
D _{out} =250 μm, W=10 μm, S=3 μm,	R _s , Ω	4.097	4.853	6.845	10.649	17.026	27.314
N=1.75	Q	4.646	8.075	8.937	8.047	6.68	5.373
SQ3	L, nH	2.313	2.38	2.469	2.589	2.751	2.972
D _{out} =250 μm, W=20 μm, S=3 μm,	R _s , Ω	6.258	6.8	7.905	9.637	12.11	15.51
N=2.75	Q	3.272	6.096	7.99	8.93	9.123	8.835
SQ4	L, nH	3.26	3.299	3.352	3.424	3.516	3.634
D _{out} =250 μm, W=10 μm, S=3 μm,	R _s , Ω	2.41	3.198	4.996	8.101	13.096	21.11
N=2.75	Q	6.04	9.351	9.315	8.031	6.6	5.31
SQ5	L, nH	3.611	3.742	3.94	4.209	4.569	5.057
D _{out} =250 μm, W=10 μm, S=10 μm,	R _s , Ω	4.387	5.323	7.922	13.22	22.834	39.916
N=2.75	Q	5.172	8.834	9.376	7.999	6.286	4.776

Table 8. L, R_s and Q for inductors with different geometry

The results given in table 8 present the trends that change with geometrical parameters. For example, with a fixed outer-dimension, Q_{max} is a decreasing function of spacing. For inductors with fixed outer-dimension (or with simultaneously varied inner- and outer-dimensions), increasing track width results in a higher Q_{max} , but a decreased L. Q_{max} is decreasing function of turn numbers, while L is an increasing function of turn numbers.

In addition, planar spiral inductors created using different metal layer and different shapes are also investigated. In table 9 are given the results from the comparison of three square spiral inductors with inner diameter $D_{in}=150\mu m$, W=20 μm , S=2 μm and N=2, created on different metal layers. While in table 10 are compared inductors with different shape – square and octagonal. It is evident that with the increase of the distance from substrate (e.g. using higher metal layer) improves the quality factor of the inductors, due to lower substrate parasitics. From table 10, it is also clear that with the use of octagonal inductors higher inductance values, lower series resistance and better quality factor can be achieved.

f CH7	SQ1 (metal4)			2	SQ2 (metal3	5)	SQ3 (metal2)		
I, GHZ	L, nH	R_s, Ω	Q	L, nH	R_s, Ω	Q	L, nH	R_s, Ω	Q
1	1.42	1.643	5.32	1.493	6.156	1.493	1.494	6.169	1.486
2	1.41	2.095	7.699	1.493	6.759	2.618	1.495	6.815	2.577
3	1.412	2.49	8.79	1.495	7.463	3.371	1.496	7.591	3.269
4	1.418	2.876	9.12	1.5	8.228	3.83	1.502	8.453	3.657
5	1.426	3.27	8.99	1.509	9.051	4.069	1.511	9.402	3.826
6	1.437	3.678	8.64	1.523	9.946	4.145	1.525	10.46	3.828

Utilization of thick metal layer in the given technology can increase the quality factor of the inductors. Thus, square spirals with Q-factor above 10 can be implemented.

Table 10. Comparison of square and octagonal spiral inductor and square spiral inductor created using thick metal layer

f GHz	1 (octagonal)				2 (square)		3 (square thick metal)		
I, GHZ	L, nH	R _s , Ω	Q	L, nH	R _s , Ω	Q	L, nH	R _s , Ω	Q
1	2.83205	6.47771	0.25641	2.83205	8.13873	0.17094	3.00579	4.09949	0.5128
2	2.83205	6.73877	0.55556	2.83205	8.16742	0.59829	2.98842	4.11957	1.2821
3	2.84942	6.75885	1.53846	2.81467	8.18177	1.19658	3.00579	4.16547	2.6496
4	2.83205	6.7818	2.00855	-	8.21906	1.66667	2.98842		3.4615
5	2.88417	6.33427	2.39316	2.83205	8.00103	2.17949	2.98842	4.19129	4.5299
6	2.88417	6.83344	2.94872	2.84942	8.25922	2.5641	3.02317	4.45235	5.1282

The effective series inductance L and quality factor Q are estimated for one port drive operation using Y-parameters and compared with measurement. The results are presented in table 11.

Table 11. Comparison of simulated and measured results for inductance and quality factor of a spiral inductor

	f, GHz	1	2	3	4	5	6
Simulatio	L, nH	4.64463	4.81051	5.07354	5.46389	5.9588	6.6334
n	Q	3.98864	6.54545	8.07955	7.69602	6.41761	4.93466
Measure-	L, nH	4.69703	4.82543	5.02859	5.42647	5.98134	6.6633
ment	Q	3.70739	6.62216	7.97727	8.02841	6.57102	4.9858

5. CONCLUSIONS

In this research were investigated the trends of integrated passive devices performance and electrical parameters variation influenced by different geometrical parameters and layout. These results can be a good guideline for practical design of passive components with application in RF integrated circuits.

6. REFERENCES

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