Optimizing the Design of a Switched-Capacitor Dynamic-Element-Matching Amplifier

A. Heidary, G. Wang and G.C.M. Meijer
Electronic Instrumentation Laboratory, Delft University of Technology
Mekelweg 4, 2628 CD Delft, the Netherlands.
Phone +31 15 278 6201 Fax: +31 15 278 5755
E-mail: a.heidary@ewi.tudelft.nl

Abstract: In this paper an optimization on recently designed switched-capacitor dynamic- element-matching amplifier is presented. The main problem of this circuit is switch-charge injection. The performance of the circuit has been improved by optimum design of the switches (acceptable R_{on} *and minimum charge injection) and measuring two different offsets to enable improved auto-calibration. The error voltages have been calculated versus the input voltage and the switch sizes. Optimal values for the switch sizes have been found. For experimental evaluation of the amplifier, a test chip has been designed in 0.7µm standard CMOC technology.*

Introduction: The main error sources in measurement system are offset and parameters drift by temperature and aging. However by using advanced techniques such as chopping and three-signal method we can get rid off any additive (offset) and multiplicative (gain) uncertainty [6]. It is only possible to design the core processing circuit with a high degree of linearity for a limited input range. Therefore, it is necessary to scale the input signal to an appropriate range before applying to the main circuit. Depending on signal levels, a voltage divider or an amplifier will be needed. Because these pre-scale circuits are outside of the three-signal loop, any inaccuracy in scaling factor will affect the accuracy of the whole system. Although the offset of a pre-scale circuit can still be eliminated, the accuracy of scaling factor is the main concern.
Nowadays, the most accurate amplifiers are realized by applying negative feedback (by means of passive element) around an active gain stage. The accuracy of the transfer function then is limited by the matching properties of the feedback elements.
Even when optimizing the matching property with a careful layout design, our accuracy requirements cannot be fulfilled.
Another technique for improving matching property of passive elements is trimming. However it is very expensive since it should be done on each circuit separately. Also it cannot guaranty long-term stability. Therefore, the best method for designing amplifier with accurate gain is using Dynamic Element Matching Feedback. This technique can guaranty long-term stability as well.

Dynamic Element Matching Feedback Amplifier

In [1] an instrumentation amplifier with resistive dynamic-element-matching feedback have been presented .The limited common mode range is the main problem of this circuit. However, we can handle rail-to-rail common mode voltage by applying a Switched – Capacitor - DEM Amplifier (Figure 1)[3]. On each cycle *N*-1 equal capacitors (equal in layout, but in reality there are some mismatches between them) are connected to the input and the remaining capacitor is connected to the output. So the average gain over *N* clock cycles equals

N-1 and in first order is independent of matching error (Equation 1)[7].

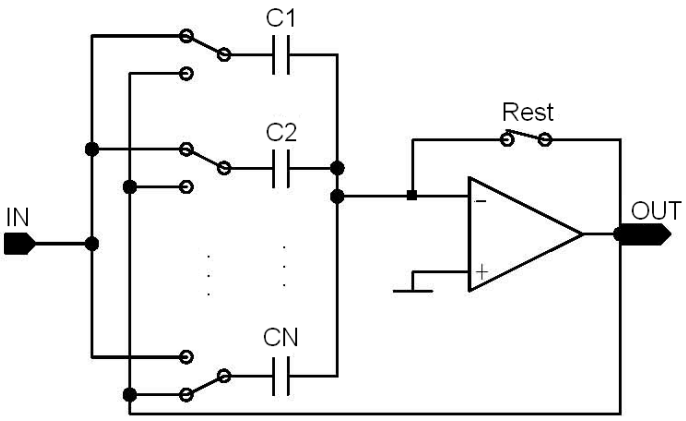


Fig. 1. Switched-Capacitor Dynamic-Element-Matching Amplifier

$$\overline{G} = \frac{1}{N}\sum_{j=1}^{N}\frac{\sum_{i=1}^{N} Ci - Cj}{Cj} \simeq N - 1 + \frac{1}{N}\sum_{j=1}^{N}\delta_j^2 \qquad (1)$$

Where δ_j is the relative mismatch between the capacitors with respect to the average value. The core processing circuit that we use, converts voltage to period and measures the period by micro controller. Therefore it can do averaging without any extra needs. The main problem of this circuit is switch charge injection. The performance of the circuit can be improved by optimum design of switches for acceptable R_{on} and minimum charge injection.

On resistance:

Figure 2 shows the output voltage of SC-DEM-Amplifier in the ideal case that $R_{on} = 0\Omega$. However, due to non-zero on-resistance of switches, the charge will pump in an exponential way. The remaining charge at the end of each period should be negligible in order not to deteriorate the accuracy of the circuit.

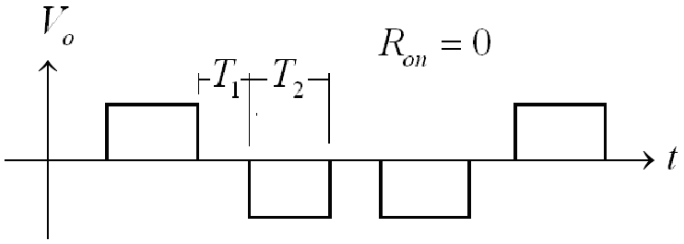


Fig.2. Output voltage of SC-DEM-Amplifier

In our design we want to minimize this charge to 10^{-5} of the whole charge. Therefore, the condition below should be held.

$$\sum_{i=1}^{k} R_{on,i} \cdot C \le T/10 \qquad (2)$$

Where *K* is the number of switches series with the capacitor (beside SC-DEM-Amplifier there are a chopper and some selectors). Also the frequency of the integrator should be far

from the frequency of the two main disturbing signals: the supply frequency, (50 Hz or 60 Hz) and the clock frequency of the micro controller (several MHz). A good compromise can be [6]:

$$T_1 = 10\,\mu s \text{ and } T_2 \geq 10\mu s \quad (3)$$

When the switch resistance are equal, with K= 3 and C_{off} = 2pF, we need

$$R_{on} \leq 150k\Omega \quad (4)$$

Figure 3 shows the on-resistance of the smallest switch with respect to V_{in} for the applied technology (AMI semiconductor CMOS0.7μm).

As we can see, as far as it concerns R_{on}, even the smallest switches can be good enough.

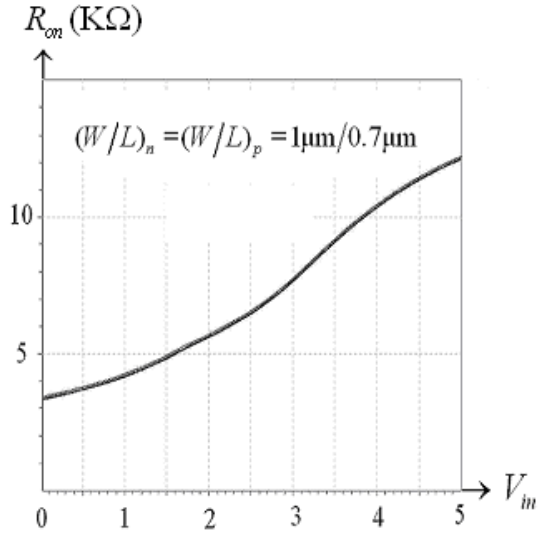


Fig 3. On-resistance of CMOS switch

Switch charge injection

During the falling edge of the clock signal, some parts of the channel- and overlap-capacitance charge are transferred to the sampling capacitor [4,5] and cause some error. Charges injected via the NMOS and PMOS switches, have opposite signs, so some parts of them will be compensated. Since the injected charge depends on V_{in}, we cannot fully compensate the charge injection by appropriate design. However, for some switches, for instance for the reset switch in Fig 1, this voltage is rather well defined (around $V_{dd}/2$), so we can design the ratio of $(W/L)_n/(W/L)_p$ for full compensation of the charge injection.

For other cases the input voltage can have any value between 0 V to V_{dd}, optimizing this ratio for $V_{dd}/2$ can be a good selection. The equivalent error voltage versus the channel width W_p for $V_{in} = V_{dd}/2$ is shown in Figure 4.

As it can be seen the optimum width W_p amounts to 2.2 μm.

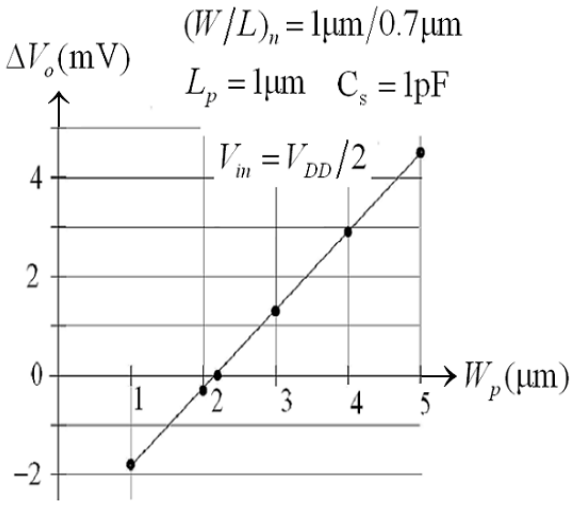
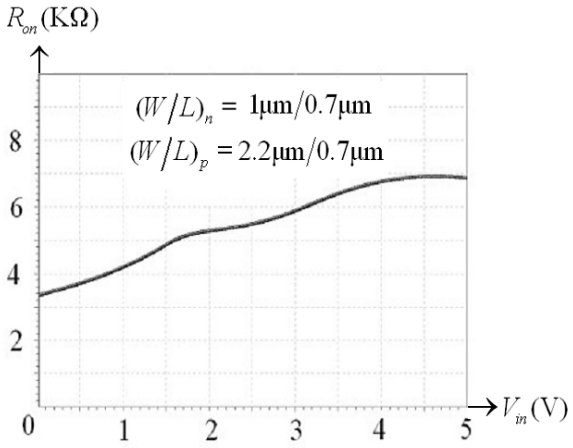
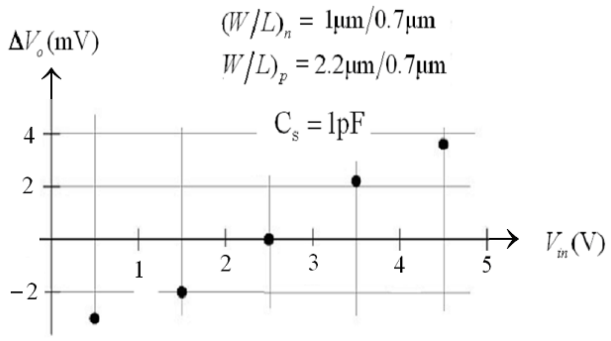


Fig4. Equivalent error voltage versus the channel width W_p

The on-resistance and switch-charge-injection error versus V_{in} for this optimum switch are shown in Figure 5. Fortunately, with this ratio the on resistance is more uniform.



(a)



(b)

Fig 5. On-resistance (a) and charge injection error (b) of optimum switch

Auto calibration

Figure 6 shows the implemented auto calibration. As it can be seen here we measure four different signals as follows:

In phase 1, the switches S1 and S3 are ON and the other switches are OFF.
(V_x measurement mode)

$$T_1 = T_x = K \cdot A \cdot V_x + T_{DEM\_offset} \qquad (5)$$

In phase 2, the switches S1 and S4 are ON and the other switches are OFF.
(DEM-OFFSET measurement mode)

$$T_2 = T_{DEM\_offset} \qquad (6)$$

In phase 3, the switches S2 and S5 are ON and the other switches are OFF.
(V_{ref} measurement mode)

$$T_3 = T_{ref} = K \cdot V_{ref} + T_{offset} \qquad (7)$$

In Phase 4, the switches S2 and S6 are ON and the other switches are OFF.
(V_{ref} measurement mode)

$$T_4 = T_{offset} \qquad (8)$$

Therefore:

$$M = \frac{T_1 - T_2}{T_3 - T_4} = \frac{A \cdot V_x}{V_{ref}} \qquad (9)$$

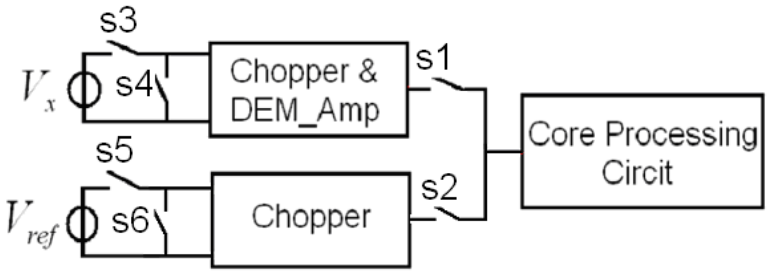


Fig6. The block diagram of designed chip

When $V_x = V_{ref}$, then $M = A$ is a measure for the gain of the DEM-Amp. We can calculate the average value and the standard deviation of the measured value of M. The first value represents the gain of the amplifier, and the second one the noise of the system.
For assessment of our amplifier we can measure the standard deviation of T_1 to T_4.
For instance the difference between standard deviation of T_1 and T_3 shows the amount of noise that is added by SC-DEM-Amplifier.

Conclusion

The switch sizes for a SC-DEM Amplifier have been optimized. A more efficient auto-calibration technique has been introduced. For experimental evaluation of the amplifier, the chip has been designed in a $0.7\,\mu m$ standard CMOS technology process. Measurement will be performed in the near future.

References

[1]. Paul C. de jong and Gerard C. M. Meijer " Absolute Voltage Amplification Using Dynamic Feedback Control". IEEE Transaction on instrumentation and measurement, vol.46, no. 4, August 1997.

[2]. Paul C. de jong , Gerard C. M. Meijer and Arthur H.M. van Roermund "A 300^{o}C Dynamic-Feedback Instrumentation Amplifier" IEEE Jornal of solid state circuit, vol. 33, no. 12, pp.1999-2009, December 1998.

[3]. G. Wang , Dutch Patent Application, No. 1014551, 2000.

[4]. Bing J. Sheu and Chenming Hu "Switched-Induced Error Voltage on a Switched Capacitor" IEEE Jornal of solid state circuit, vol. Sc19, no. 4, August 1984.

[5]. C. Eichenberger and W. Guggenbuhl "Charge Injection of Analog Switches" IEEE Proceedings-G, vol. 138, no 2, April 1991.

[6]. Frank van der Goes "Low-Cost Smart Sensor Interfacing" PhD thesis Delft University of Technology, The Netherlands, 1996.

[7]. G. Wang "CMOS Band Gap Reference and Temperature Sensors and their Applications" PhD thesis Delft University of Technology, The Netherlands, 2004.