MEASUREMENT CONVERTER FOR AVERAGING PULSE MODULATED PARAMETERS AND SIGNALS

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The paper introduces on a novel measuring converter for averaging pulse modulated parameters and signals with direct conversion and improved metrology characteristics. The proposed circuit is a Pulse-width demodulator (PWD) with improved metrology characteristics by the introduced new control approach. Simulations are presented to prove the validity of this approach by using the software package Cadence Pspice. *The conventional and the presented circuits are analyzed under the same operational conditions. The accuracy of the conversion is estimated. The carried out simulations and comparisons prove the validity of the presented control approach and show excellent performance as opposed to the conventional circuit.*

Keywords: Pulse-width demodulators, time amplitude converters (TAC)

1. INTRODUCTION

In power electronics, for the purpose of control and protection of power transistors pulse-width demodulators with direct conversion are often used. They must meet the following requirements: high speed, high stability, minimum pulsations in the output signal, good linearity. In practice such measurement converters are called pulse width demodulators (PWD) in Power Electronics applications, time amplitude converters (TAC) in Measuring Applications, or integrating DAC in digital circuits.

The current value of the width of the input pulses t_{xn} in the linear time-amplitude converters is related to the modulating signal $X(t)$ as follows:

$$txn = tx0 + \Delta txmax \,.\, X(t) \qquad (1)$$

where: tx0 is width of non-modulated pulses;

tx0 = tx0' + tx0";

tx0' is the width of non-modulated pulses at the beginning of the period;

tx0" is the width of non-modulated pulses at the end of the period, usually

tx0' = tx0" = 2÷5% of the period.

Δtxmax = T - tx0 is the maximum diapason of the width of the pulses.

The purpose of PWD is to restore the modulating signal $X(t)$, carrying the useful information.

In this paper a *modified PWD circuit with improved metrological parameters* is presented and compared with the conventional PWD.

2.CONVENTIONAL PWD CIRCUIT

The circuit conventional of conventional pulse-width demodulator is shown in fig.1, and the waveforms in fig.2.

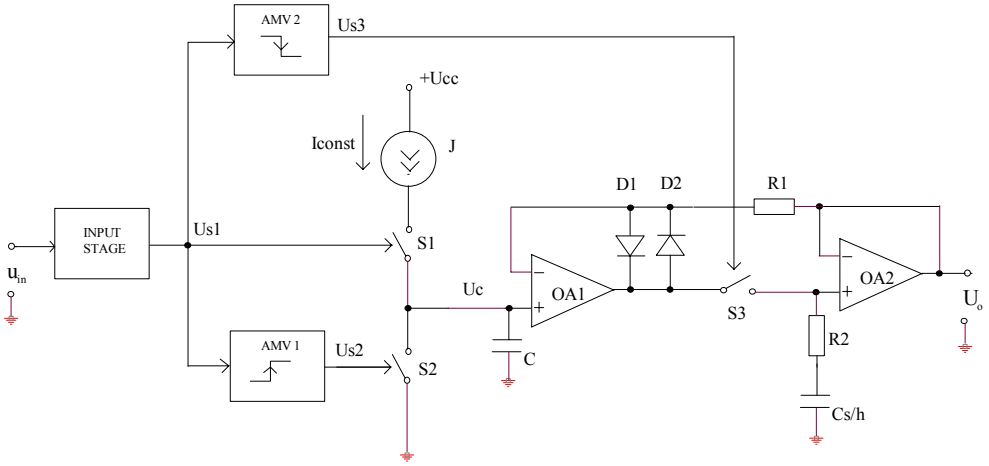

Fig.1. The circuit of conventional pulse-width demodulator

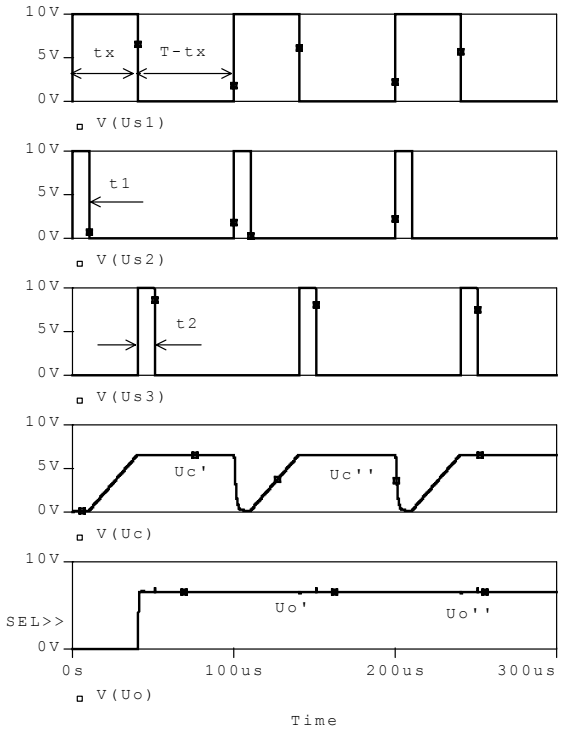

Fig.2. Operational waveforms of the conventional PWD

The switch S1 is controlled by the output logical signal Us1 of the input stage. With the closing of S1, at the same moment the switch S2 also closes for the reset time – t1 of the capacitor C. Then the constant current I_{const} is leaded away to the common ground together with the discharge current of the capacitor C. After the reset time - t1 is over, the analog switch S2 opens and the constant current through S1 starts to charge the capacitor C. At the end of tx, the switch S1 opens and the voltage of the capacitor is set to Uc', which is unchanged for the track time – t2 of the analog memory, realized with the elements OpAmp1, OpAmp2, D1, D2, S3 и Cs/h. The analog memory is realized according to the structure of the integrated analog memory LM398, where the resistor R1, limits the maximal output current of OpAmp2, and R2, D1 and D2 prevent OpAmp2 from saturation, when the analog switch S3 is open. The speed of the analog memory is determined mostly by the speed of OpAmp1 and OpAmp2. The amplifier OpAmp1 provides the necessary

current for the charge of Cs/h. The second OpAmp2, which is with MOS input transistors, reduces the discharge current of the capacitor [1]. For the time (T-t2), equal to the hold time, the voltage Ucs/h of the capacitor Cs/h decreases with $\Delta U_{Cs/h}$:

$$\Delta U_{Cs/h} = \frac{(T - t2)(I_{iOA2} + I_{leak})}{Cs/h} \qquad (2)$$

where I_{iOA2} is the input current of OpAmp2;

I_{leak} is the leakage current of self-discharge of the capacitor Cs/h and the resistance of the off state Roff of the analog switch S3, which is not infinity.

During the tracking time - t2, the capacitor Cs/h is charged from the output current of OpAmp1 – $I_{o,OA1}$ to the voltage $U_{Cs/h}$. The required tracking time can be found by:

$$t2 = \frac{C_{s/h}.U_{Cs/h}}{I_{o,OA1}} \qquad (3)$$

The capacitance of the memory capacitor Cs/h can be found form (2), and the minimal value of tracking time from (3).

Increasing the value of the memory capacitor Cs/h, leads to decreasing the voltage of the capacitor, but in this way the tracking time is increased. This method must be applied only when signals with large period are converted.

Till the next pulse for tracking, the analog memory keeps at its output voltage Uo´, which in the ideal case is equal to the voltage of the capacitor C, Uc´:

$$Uc' = \frac{1}{C}\int_{t1}^{tx} i_C(t)dt = \frac{I_{const}}{C}(tx - t1) \qquad (4)$$

Must be noted that the second part of equation (4) is a parameter in the conversion equitation, and should not be mixed with the "additive error".

Additional error in this case is caused by the instability of the parameters, related to the fact that $-I_{const}.t1/C \neq 0$ (deviation of these parameters from their nominal values), and also and the bias voltages of OpAmp1 and OpAmp2.

The multiplicative error depends on the instability of the parameters related to the conversion coefficient, according to equation (4): I_{const} and C.

It can be noticed, that it is necessary to ensure the stability of the parameters I_{const} и C, and also to take special actions to guarantee constant value of the reset time - t1, which will surely leads to complicating the circuit.

It is necessary to accomplish the next essential requirement: to ensure full discharge of the capacitor C, thus the inequality $t1 > 3\tau c$ should be kept (τc is the discharge time constant of the capacitor C) [3].

3. PROPOSED IMPROVED PWD CIRCUIT

The discussed conventional circuit, (fig.1), is modified and improved for getting better metrological parameters. A new way for controlling is proposed. The circuit is shown on fig.3 and the waveforms on fig.4.

When S1 is closed, the constant current I_{const} begins to flow and to charge the capacitor C.

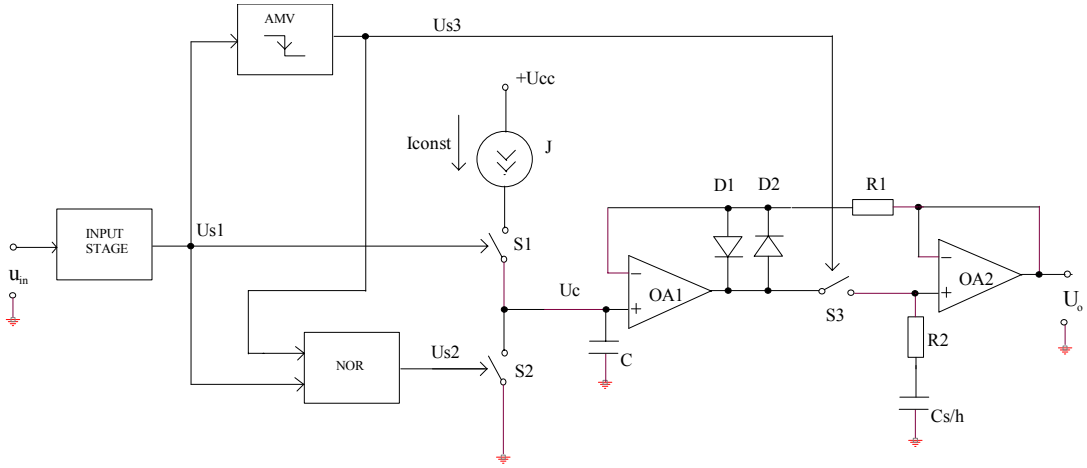

Fig.3. The Circuit of the proposed PWD

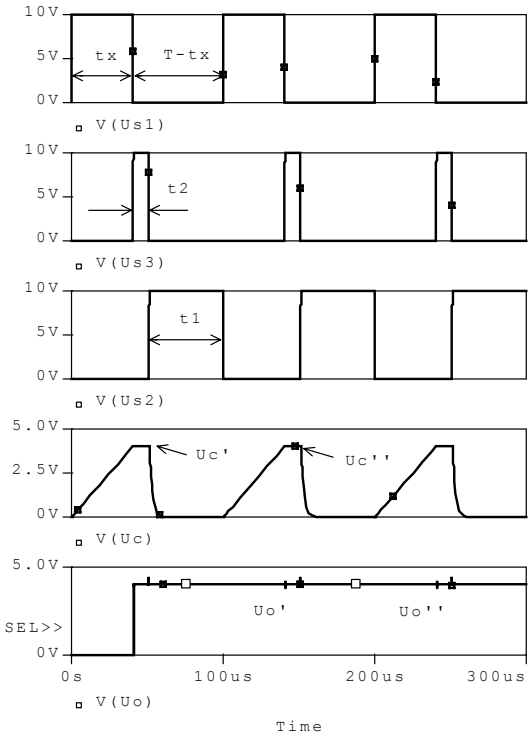

Fig.2. Operational waveforms of the proposed modified PWD

At the end of tx, the astable multivibrator, with its output signal Us3 defines the tracking time of the analog memory – t2. During this time the voltage of the capacitor C is unchanged and at the output of the analog memory the voltage Uo' is set. After t2 is over the logic element "or-not" forms the control signal Us2 with duration t1 and the reset of the capacitor C is initiated. The difference between this case of control, and the previous one, is that the constant current I_{const} does not flow through the switch S2. In this case there are better conditions for discharging of the capacitor C. Discharging the capacitor continues till the next front edge of Us1. The voltage Uc', of the capacitor C, after the time tx is:

$$Uc' = \frac{1}{C}\int_0^{tx} ic(t)dt = \frac{Iconst}{C}.tx \qquad (5)$$

Comparing equations (4) and (5) for the two circuits, one can see that in the equation (5) of the modified circuit shown on fig.3 the second part of equation (4) is

missing. In this case it is not necessary to take any special measures for stabilizing the reset time – t1, which is a significant advantage of the modified circuit.

4. ANALYSIS AND COMPARISON

The analysis of both circuits in time domain is carried out by *Cadence Pspice* at the following conditions:

- period of the signal :T=100μs;
- track time of the analog memory: t2=10μs;
- discharge time of the capacitor: t1=10μs;
- discharge time of the integrating capacitor C for the circuit of fig.1 -t1=10 μs; for the circuit of fig.3 - t1max = T-(txmin+t2) =70 μs and t1min = T-(txmax+t2) =10 μs;
- range for the time of conversion: tx=(20÷80)μs;
- rise and fall time of the control signals: 250ns;
- readings of the output signals: 500μs;
- C=100nF ; Cs\h=1nF; Iconst=10mA

The manufacturer models of OA-LM082; analog switch DG304; diods 1N4148 are used in the simulation of the circuits of fig.1 and fig.3.

Part of the simulation results are shown in fig.2 and fig.4.

Table 1. shows the data for Uo*meas,* measured during the simulation, and calculated according equation (6) relative error δx, The calculations are done with different width of tx of the input signal: tx=(20÷80)μs. The nominal values of Uo*nom* are calculated from equations (4) and (5) for each of the circuits.

$$\delta x = \frac{\Delta X}{Xnominal} = \frac{Xmeasurement - Xnominal}{Xnominal} \qquad (6)$$

Table 1 Comparison of the conventional and proposed improved PWD circuits

	Conventional PWD circuit, Fig.1			Proposed improved PWD circuit, Fig.3		
tx[μs]	Uo*meas,*[V]	Uo*nom*, [V]	δx [%]	Uo*meas,*[V]	Uo*nom,* [V]	δx [%]
20	1,228	1	22,8	2,045	2	2,25
30	2,241	2	12,05	3,050	3	1,67
40	3,251	3	8,37	4,055	4	1,38
50	4,264	4	6,60	5,059	5	1,18
60	5,274	5	5,48	6,060	6	1,00
70	6,287	6	4,78	7,068	7	0,97
79,2	-	-	-	8,035	7,925	1,39
80	7,300	7	4,29	-	-	-

Figure 5 shows a graph of the relative error with different duration of the input signal of both conventional and proposed improved circuit. A significantly smaller error is attained with the proposed circuit. The precision of the conversion is much better with smaller duty ratios.

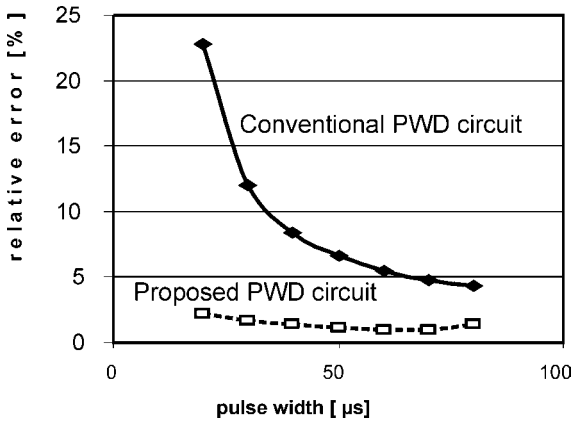

Fig.5. Relative error in conventional and proposed improved PWD circuits

5. CONCLUSION AND RECOMMENDATIONS

The proposed new PWD circuit with direct conversion with improved speed has the following advantages and improved metrological characteristics:

- Lower relative error;
- Better precision with smaller duty ratios;
- Converting signals with short periods.

In practical realization of the circuit the following requirements should be kept:

- The used amplifiers should be high speed precision operational amplifiers
- The constant current source should have long term and temperature stability;
- Resistors should be at least 1% with TKR = 50ppm, and the capacitors to have a polypropylene dielectric, which assures low dielectric absorption and low leakage current.
- Analog switches should have low value of Ron, high Roff, low own capacity, and good speed;
- The choose of Cs/h should be according to the next conditions – greater value assures smaller pulsations of the output voltage and better linearity of the circuit, but this reduces the бързодействието of the circuit.

6. ACKNOWLEDGEMENT

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7. REFERENCES

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