VISUALIZATION OF THE FRAMES FROM CMOS IMAGE SENSOR ON THE MONITOR IN REAL TIME

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In the present paper is described optoelectronic system for visualization of frames from a CMOS image sensor on the monitor. It uses features and advantages of the programmable logic and it based on a FPGA Spartan III. Hardware and software solutions are presented. Simultaneously with the data from the image sensor, the system can visualize addition information. This expands features of the system especially when it is uses for measurement or scientific applications. In this way there is no necessary to using additional device for visualization of the information. In the end of the paper experimental results are applied.

Keywords: CMOS image sensor, Image processing, RGB interface, Real-time applications, VHDL

1. Introduction

Optoelectronic systems are widely used in different fields of the industry and our everyday live. Their applications grew every day. The system for visualization of the frames from the CMOS image sensor was developed like an extension to the optoelectronic system for determination of the position of light spot

The block diagram of the realized system is shown in Figure 1.

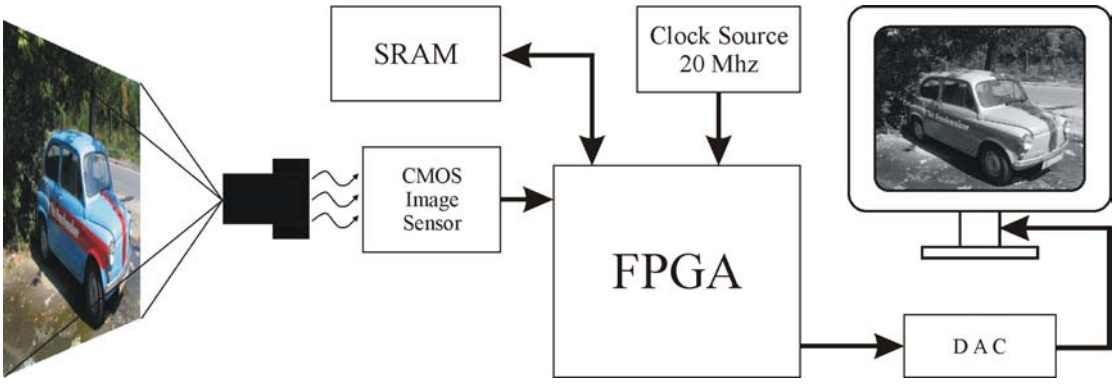

Figure 1 – Block diagram of the optoelectronic system

Algorithms for Image processing require high performance and calculation power from the proceeding system. To be ensured high performance of the proceeding system, it is based on FPGA Spartan III by XILINX. The software is written in VHDL.

The information is obtained directly from 2 MP (1600x1200) CMOS color image sensor OV2610. After that read and structured data are processed. Clock rate for the system is generated by external generator and it is 20 MHz. For proper synchronization there is only one clock source for entire optoelectronic system. For temporary storage of the current frame, additional fast SRAM is used. This is needed because it is necessary to be executed reformatting of the frames incoming from the image sensor. Output data are eight bit binary numbers. The analog signal for RGB video interface is produced by additional external Digital-to-Analog Converter. Realization of the RGB video interface based on a FPGA allows addition information to be visualized simultaneously with the frames obtained from the image sensor.

A grayscale SVGA (800x600) RGB video interface is realized. The frame rate is 60Hz. The output data are eight bit numbers, which ensure a picture with 256 grayscale levels.

On the paper are presented software and hardware realization of such Opto-electronic system working in the real time.

2. Problem statement

2.1. RGB video interface description

In the color video interface there is three signals: Red, Green and Blue. When these three signals are mixed, equivalent color is produced. In the monochrome frame there is only one signal, which defines the gray level of the corresponding pixel. If the volumes of the three basic colors are equal – again monochrome frame is produced.

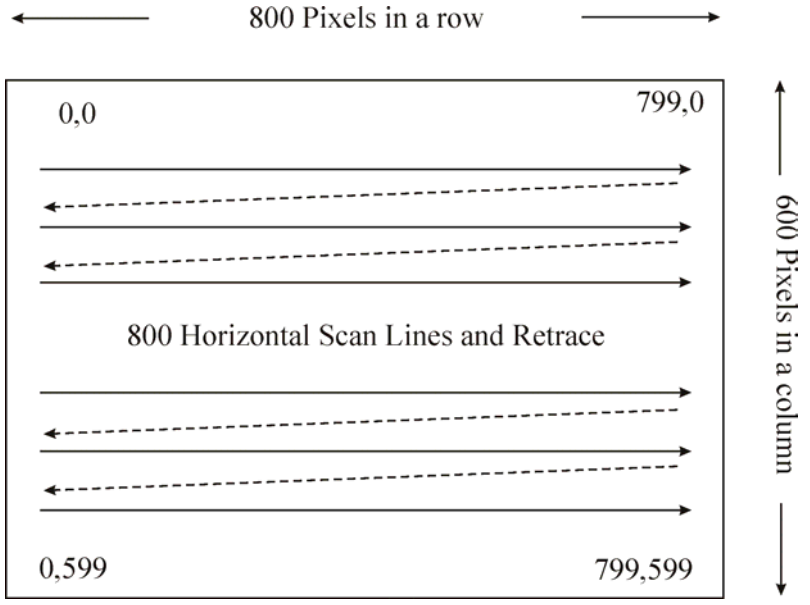

Figure 2 – Image restoration

The screen refresh process seen in Figure 2 begins in the top left corner and paints pixels from left to right. At the end of each row, the row increments and the column

address is reset to the first column. Each row is painted until all pixels have been displayed. Once the entire screen has been painted, the refresh process begins again.

The video signal paints or refreshes the image using the following process: The vertical sync signal tells the monitor to start displaying a new image of frame, and the monitor starts in the upper left corner with pixel 0,0. The horizontal sync signal tells the monitor to refresh another row of 800 pixels.

After 600 rows of pixels are refreshed with 600 horizontal sync signals, a vertical sync signal resets the monitor to the upper left corner and the process continues. During the time when pixel data is not being displayed and the current position is returning to the left column to start another horizontal scan, the RGB signals should all be set to the color black (all zeros) [1].

In Table 1 the main characteristics of the RGB video interface for various graphic standards are shown. The characteristics which are reached in the described optoelectronic system are marked.

Graphics standard	Horizontal resolution [pixels]	Vertical resolution [pixels]	Horizontal frequency [kHz]	Frame rate [Hz]	Pixel/Sample rate [MHz]
VGA	640	480	31,5	60	25,175
	640	480	37,7	72	31,5
	640	480	37,5	75	31,5
	640	480	43,3	85	36
SVGA	800	600	35,1	56	36
	800	600	37,9	60	40
	800	600	48,1	72	50
	800	600	46,9	75	49,5
	800	600	53,7	85	56,25
XGA	1024	768	48,4	60	65
	1024	768	56,5	70	75
	1024	768	60	75	78,75
	1024	768	64	80	85,5
	1024	768	68,3	85	94,5
SXGA	1280	1024	64	60	108
	1280	1024	80	75	135
	1280	1024	91,1	85	157
UXGA	1600	1200	75	60	162
	1600	1200	81,3	65	175,5
	1600	1200	87,5	70	189
	1600	1200	93,8	75	202,5
	1600	1200	106,3	85	229,5

Table 1 – Characteristics for various graphic standards

It is obviously that the pixel rate increase very fast with increase of the frame size and frame rate. This provokes huge requirements for the calculation power of the system.

2.2. CMOS image sensor description

Used CMOS image sensor is OV2610. It uses Bayer pattern sensor matrix with UXGA resolution (1600x1200) [2].

The sensor supports two resolutions: UXGA (1600x1200) and SVGA (800x600). The relation between generated frames and clock source rate are shown in Table 2.

PCLK (MHz)	24	12	6	3
Frame rate (fps)	10	5	2,5	1,25

Table 2 – Frame and Pixel rates

There is build in PLL in the image sensor, which generates all needed clocks from the external clock source.

3. Implementation

The software part of the project, which is implemented in the FPGA [3], is separated into different blocks shown in Figure 3.

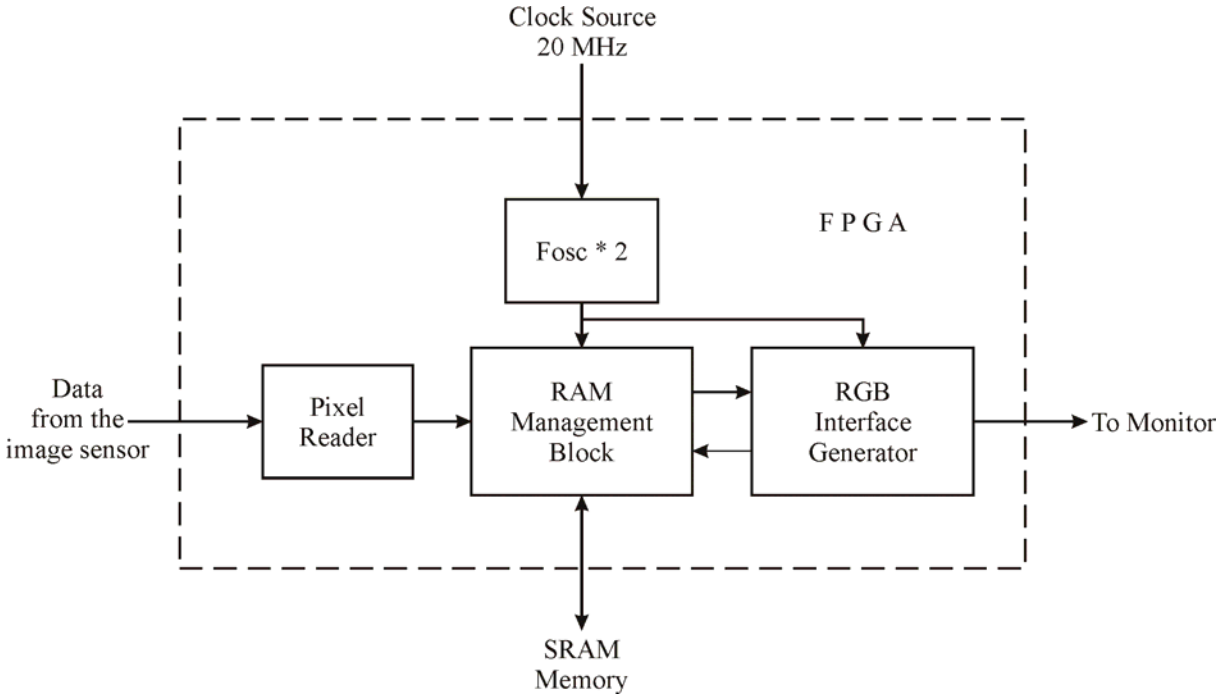

Figure 3 – Structure of the design implemented into FPGA

The Pixel Reader block reads the data from an image sensor and transforms RGB frames into monochromes. It also resizes the frame from UXGA (1600x1200) to SVGA (800x600).

Used FPGA has built in DCM (Digital Clock Manager). It provides flexible, complete control over clock frequency, phase shift and skew through the use of the DCM feature. The DCM is used for multiplication of the input clock with two. In this way 40MHz clock frequency is obtained.

The restrictions about RGB interface is because of the used SRAM memory. It minimum access time is 10ns. The synchronous Read/Write cycle with the memory is

realized. These cycles are executed by rising and falling edge of the clock signal. The communication with the SRAM is shown in Figure 4.

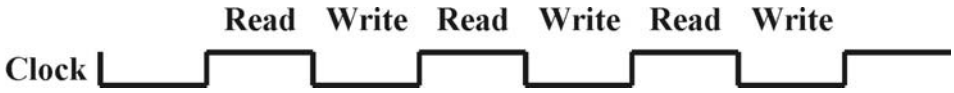

Figure 4 – Communication with SRAM

Clock period = 25ns (40MHz)
Read Cycle = 12,5ns
Write Cycle = 12,5ns

The access time with the SRAM allows realization of SVGA interface with 60Hz frame rate. The communication with the SRAM memory is executed by the Management Block.

RGB Interface Generator ensures right generation of the synchronization pulses and information shown on to the monitor. The other feature of this module is possibility for visualization of the additional data simultaneously with the image from the CMOS image sensor. For example this information can be grid scale or/and text. This is useful when the system is used for measurements.

The image sensor generates 10 frames per second but the RGB interface has frame rate 60Hz. This means that each 6 following frames are equal, but high frame rate ensures a stable image on the monitor.

4. Results

The output digital data is transformed to an analog signal with the external DAC (Digital to Analog Converter). 0V corresponds to a black color in the frame and 0,7V corresponds to a white color in the frame. Realized DAC works with 75 Ohm load impedance. Figures 5 and 6 are showing the pictures on the monitor in different cases.

Figure 5 – Visualization of scene

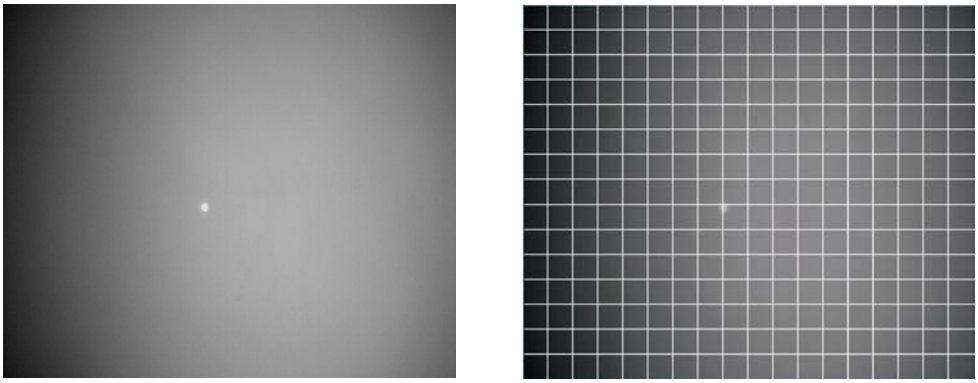

Figure 6 - Visualization of laser spot and grid scale for measurements

5. Conclusion

In the presented paper proposed optoelectronic system, which processes the data from the CMOS image sensor and create RGB interface for visualization on the monitor. The system is realized over the FPGA Spartan 3. The characteristics of the RGB interface and its realization are described.

6. References

[1] Hamblen J.O, *Rapid Prototyping of digital systems*, Kluwer Academic Publishers, Boston / Dordrecht / London, 2001.

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[3] Roth C. H., *Digital system design using VHDL*, PWS Publishing Company 1997.