VIRTUAL UNIVERSAL COUNTER

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This paper is aimed to introduce the basic concepts, techniques and the underlying principles that constitute the construction of virtual counter possessing full functionality of the conventional products. The introduced virtual universal counter is based on general-purpose counter/timer module of the multifunctional DAQ and graphical application development environment LabVIEW. The build in timing functions includes period measurement, pulse-width measurement, event counting, single-pulse generation, and pulse-train generation with programmable frequency and duty cycle. Unfortunately these functions can be used for TTL levels only. In this paper the design and development of simple counter's input circuitry is described. It is necessary to convert the input signal into a digital form compatible with the counter's counting register. In addition of conventional methods for period and frequency measurement, the implementation of reciprocal technique with the two build in DAQ 24 bits counters is introduced.

Keywords: Universal Counter, Virtual Instrumentation, Reciprocal Technique, Graphical Programming.

1. INTRODUCTION

Since many years, the conventional counter is used as a digital electronic device, which measures the frequency of an input signal. It may also have been designed to perform related basic measurements including the period of the input signal, ratio of the frequency of two input signals, time interval between two events and totalizing a specific group of events [1, 3]. The electronic counters have become increasingly powerful and versatile in the measurements they perform and have found widespread applications in the laboratories, production lines and service centers of the telecommunications, electronics, electronic components, aerospace, military, computer, education and other industries. The advent of the integrated circuit, the high speed MOS and VLSI devices, and lately the microprocessor, has brought about a proliferation of products to the counter market.

On the other hand virtual measurement technologies have entered the scientific and engineering realm within the last few years in parallel with the emergence of the personal computer as a low cost, widely available and generic computing platform. Although the modern trend is to construct even conventional instruments as sensors incorporated together with software, virtual instruments (VIs) can be distinguished because they make use of a general-purpose computing platform to provide the processing, which can also carry out a variety of other tasks by loading other software.

2. PLANNING THE COUNTER'S FUNCTIONALITY

The conventional counter is a digital electronic device that measures the frequency of an input signal. The reciprocal counter is a new class of counter, which always makes a period measurement on the input signal [2]. If frequency information is desired, it can be directly displayed by taking the reciprocal of the period measurement. The reciprocal technique is gaining much popularity as it offers two major and distinct features:

- The ±1 count quantization error is independent of the input signal frequency. Hence, for a noiseless input signal and assuming negligible trigger and time base error, the resolution of the reciprocal counter would also be independent of the input signal frequency.
- The period counting characteristic of the reciprocal technique provides the capability for control of the main gate in real time.

The basic block diagram of a reciprocal counter is essentially similar to the conventional counter except for the fact that the counting is done in separate registers for time and event counts. The contents of these registers are processed and their quotients computed to obtain either the desired period or frequency information, which are displayed directly. The simplified block diagram of a high-precision reciprocal counter is shown in figure 1. The Event Counter accumulates counts from the input signal while at the same time, the Time Counter accumulates counts from the internal clock for as long as the main gate is open. In a single period measurement, the main gate opens for precisely one period under the control of the input signal. During this time interval, the Event Counter would have accumulated one count while the Time Counter would have accumulated a number of clock pulses.

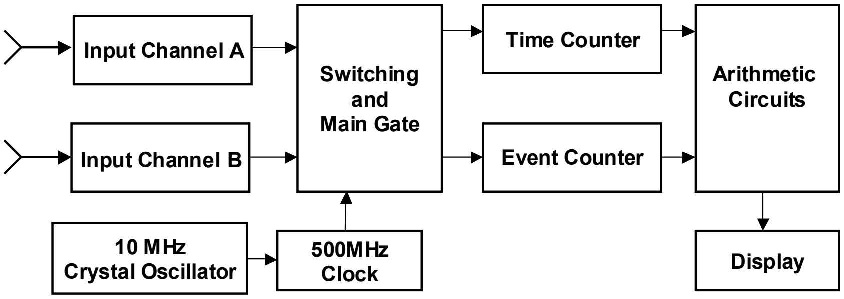

Fig. 1. Block diagram of a reciprocal counter

In period averaging, the main gate is open for more than one (*K*) cycle of the input signals. The Event and Time Counters accumulate and count pulses from the input signal and the internal clock, respectively, during this time while the gate is open. The number of accumulated clock pulses N is multiplied by the clock period T_{ref} to give the period of the input signal:

$$K.T_{in} = N.T_{ref} \text{ or } f_{in} = \frac{K.f_{ref}}{N}. \tag{1}$$

The expression for computing the quantization error is obtained by differentiate of (1) and is given by the equation:

$$\frac{\Delta f_{in}}{f_{in}} = \pm\frac{T_{ref}}{KT_{in}} = \pm\frac{f_{in}}{K.f_{ref}} \tag{2}$$

The essential part of modern multifunction DAQ is the counter/timer circuits, which is responsible for synchronization of all the system. In National Instruments production these circuits is realised as specialized chips called DAQ-STC [4].

The DAQ-STC contains nine modules, or function groups. These function groups include the analog input timing/control module, analog output timing/control module, general-purpose counter/timer module (GPCT), programmable function inputs module, RTSI trigger module, digital I/O module, interrupt control module, bus interface module, and the miscellaneous functions module.

The GPCT consists of two independent 24-bit up/down counters, each with associated load and save registers, and a control structure for implementing some common counting and timing I/O functions. These timing functions include period measurement, pulse width measurement, event counting, single-pulse generation, and pulse-train generation with programmable frequency and duty cycle (the percentage of the cycle that the pulse is high). Most functions can operate using only one general-purpose counter. There are two modes of operation for the measurement functions - single mode and buffered mode. In single mode, the functions obtain only one measurement. In buffered mode, the functions obtain a series of consecutive, gap-free measurements.

Figure 2 shows a simplified model of the counter. Each GPCT counter has a source input (SOURCE), a gate input (GATE), and an up/down control input (UP_DOWN). When the counter is enabled to count, rising edges on the SOURCE input cause the counter to increment or decrement. The GATE input acts as a general-purpose control signal and can operate as a counter trigger signal, a counter enable, a save signal, a reload signal, an interrupt, an output control signal, a load register select signal, and a counter disarm. The UP_DOWN input determines whether the counter counts up or down. The counter outputs are the signals labeled OUT and INTERRUPT. OUT is a counter TC-related signal, which can toggle on every counter TC or can output the counter TC signal directly. INTERRUPT is an interrupt signal routed inside the DAQ-STC to the interrupt control module. The counter has load registers to reload the counter with new count values. The save registers save the counter contents until they can be read by software.

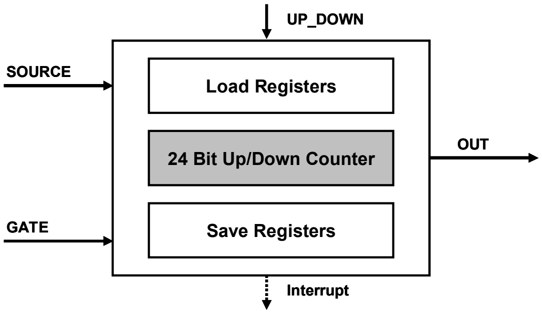

Fig. 2. Model of a GPCT counter

3. DESIGN OF HARDWARE CONFIGURATION

The proposed block diagram of virtual universal counter is shown on figure 3. The shaper circuit is appropriately connected to the DAQ and is used for converting the input signal into a digital form compatible with the counter's counting register.

The input coupling (AC or DC coupling) selection of the counter is cover by the digital inputs DIO7 and DIO3. The trigger level is controlled by the analog outputs

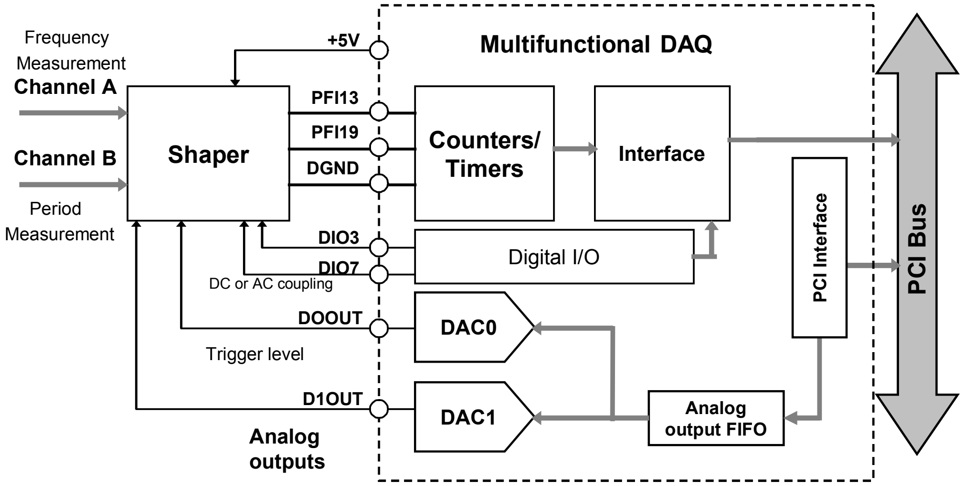

Fig. 3. Block diagram of virtual universal counter

D0OUT and D1OUT. The input (measured) signals appearing at the channels A and B of the shaper and then the conditioned signals are leads on the inputs PFI13 and PFI19 (SOURCE of the counter 1 and GATE f the counter 0). The voltage of the comparator's open collector is applied from the DAQ's output +5V (fig. 4).

There are many circuits of shapers for converting the arbitrary signals to TTL levels signals. In this case an adaptation of well-known circuit of comparator with hysteresis is used. The circuit is shown on the figure 4 [5].

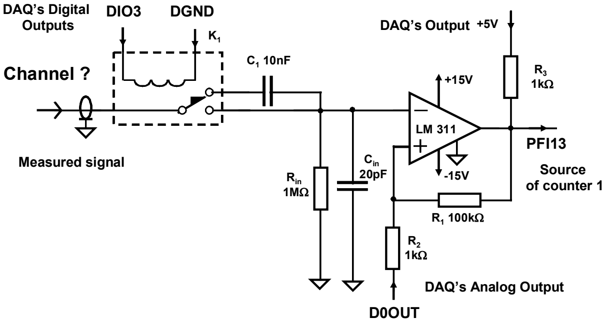

Fig. 4. The circuit of the shaper

4. DESIGN BY UML

Applying structural approach the design process can be divided in dynamic and structural modeling. The UML's activity chart diagrams can describe the dynamic behavior of the developed system. In order to accomplish the modeling of flow of behavior for reciprocal countering the UML activity diagram is most appropriate. The dynamic model is shown on figure 5. The correct sequence of software configuration of DAQ's counters for frequency and period measurement is: independently programming of the counters, synchronization, results reading and displaying.

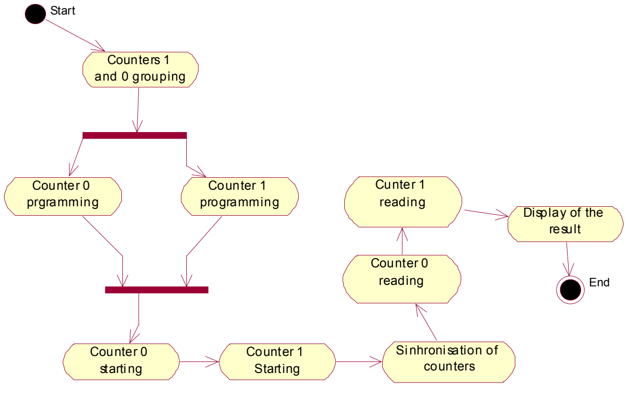

Fig. 5. The UML's activity diagram

In the case of graphical programming presented in this paper, for structural modeling most appropriate are component diagrams. Component diagram describe the organization of physical software components, including source code, existing LabVIEW function, created applications and executables is shown on figure 6. This diagram define that many virtual counter's component are build-in LabVIEW functions.

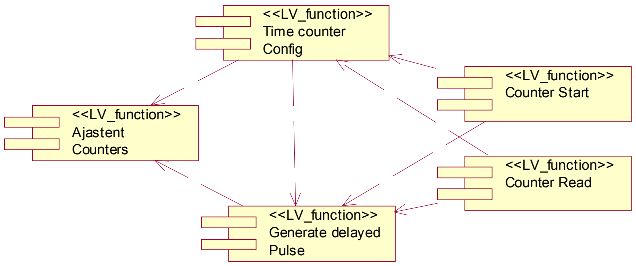

Fig. 6. The UML's component diagram

5. SOFTWARE CODING

The user interface or so-called front panel of virtual universal counter is shown on figure 7. On the left part of the figure can be seen the controls for AC or DC coupling of the input channels A and B. The controls for measurement method, internal clock selection or number of pulse cycles counting are located in the center of the panel. In the right of the figure the roll controlling trigger level are placed.

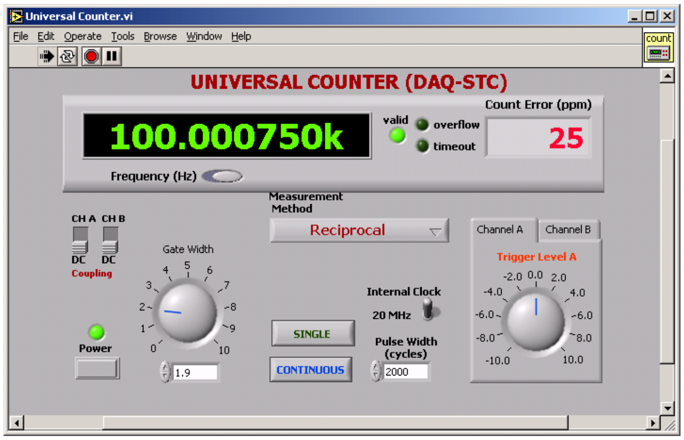

Fig. 7. Front panel of virtual universal counter

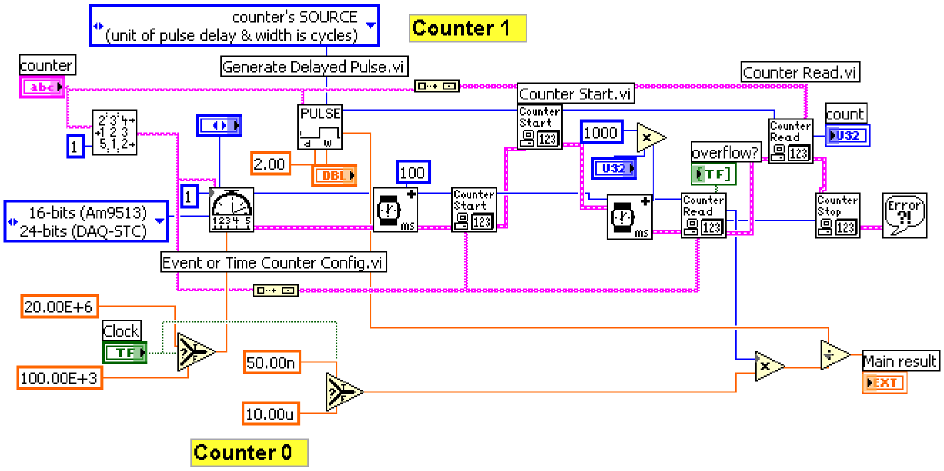

Fig. 8. The program code of the virtual reciprocal counter

The program code (block diagram) of the virtual reciprocal counter is shown on figure 8. The diagram is well corresponded of the component diagram (figure 5).

6. EXPERIMENTAL RESULTS

The results of the device characterisation are fulfilled in table 1. For referenced frequency generation the build in HP 4195A Network/Spectrum Analyzer frequency syntesizer is used. The measuring accuracy is calculated using the well-known equation: $\delta = \frac{f_{meas} - f_{in}}{f_{in}}.1.10^6, \text{ppm}$. In order to achieve quantization error ±1 count, the cycles K is calculated according equation (2).

Table 1

Generated frequency f_{in}, Hz	**Measured frequency f_{meas}, Hz**	**Cycles K**	**Measuring accuracy δ, ppm**
10	9,999270	2	73
100	99,99500	5	50
500	500,0035	25	7
1 k	1,000008 k	50	8
5 k	5,000035 k	250	7
10 k	10.00008 k	500	8
50 k	50.00040 k	2500	8
100 k	100.0009 k	5000	9
500 k	500.0030 k	25000	6
1 M	1.000008M	50000	8
2 M	2.000016M	100000	8
3 M	3.000024M	150000	8
4 M	4.000032M	200000	8
5 M	5.000038M	250000	8

7. CONCLUSION

The approach of design and implementation of virtual universal counter is considered in this presentation. Based on multifunction DAQ, graphical ADE and simple additional hardware, the realized counter posses full functionality of similar bench top measuring instrumentation. By using build in LabVIEW library functions and by creating additional software modules it is possible to achieve virtual instrument measuring time intervals in three independent techniques (frequency, period and reciprocal). This capability of the realized counter based on multifunction DAQ will be useful for educational purposes. The presented approach can be applied for specialized counter/timers DAQ to realize virtual counters with much more improved specifications, especially concerning the frequency range.

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